## CLAIMS

1. A THx2 threshold gate cell comprising:

a mode-independent PMOS configuration;

an NMOS configuration configured to operate in one of a TH12 mode and a TH22 mode, wherein x is a threshold of 1 for the TH12 mode and x is a threshold of 2 for the TH22 mode, and

further comprising an output network, wherein:

the mode-independent PMOS configuration comprises a reset NULL block comprising a pair of PMOS transistors in series; and

the NMOS configuration comprises a set DATA block comprising a pair of NMOS transistors.

2. The THx2 threshold gate cell of claim 1, wherein the mode-independent PMOS configuration and the NMOS configuration are configured to form a NAND gate.

3. The THx2 threshold gate cell of claim 1, further comprising a mask programmable gate array (MPGA).

4. The THx2 threshold gate cell of claim 3, wherein the NMOS configuration configured to operate in one of the TH12 mode and the TH22 mode based on an additional NMOS wiring configuration to eliminate an NMOS transistor in the TH12 mode.

5. The THx2 threshold gate cell of claim 4, wherein the set DATA block comprises the pair of NMOS transistors connected through the additional NMOS wiring configuration in parallel in the TH12 mode.

6. The THx2 threshold gate cell of claim 4, wherein the set DATA block comprises the pair of NMOS transistors connected through the additional NMOS wiring configuration in series in the TH22 mode.

7. The THx2 threshold gate cell of claim 1, wherein the set DATA block comprises the pair of NMOS transistors connected in parallel in the TH12 mode.

8. The THx2 threshold gate cell of claim 1, wherein the set DATA block comprises the pair of NMOS transistors connected in series in the TH22 mode.

9. The THx2 threshold gate cell of claim 1, wherein the output network comprises a pair of CMOS inverters.

10. A method of operating a THx2 threshold gate cell comprising:

accessing the THx2 threshold gate cell comprising a mode-independent PMOS configuration and an NMOS configuration configured to operate in one of a TH12 mode and a TH22 mode;

setting x to a threshold of 1 to operate in the TH12 mode; and

setting x to a threshold of 2 to operate in the TH22 mode, wherein:

the THx2 threshold gate cell is a mask programmable gate array (MPGA), the MPGA comprising an MPGA base cell and an output network;

setting x in THx2 to a threshold of 1 to operate in the TH12 mode comprises

(1) connecting a pair of NMOS transistors in parallel in the NMOS configuration to eliminate an NMOS transistor of the NMOS configuration in the TH12 mode for the MPGA; and

setting x in THx2 to a threshold of 2 to operate in the TH22 mode comprises

(1) connecting the pair of NMOS transistors in in series in the NMOS configuration for the MPGA.