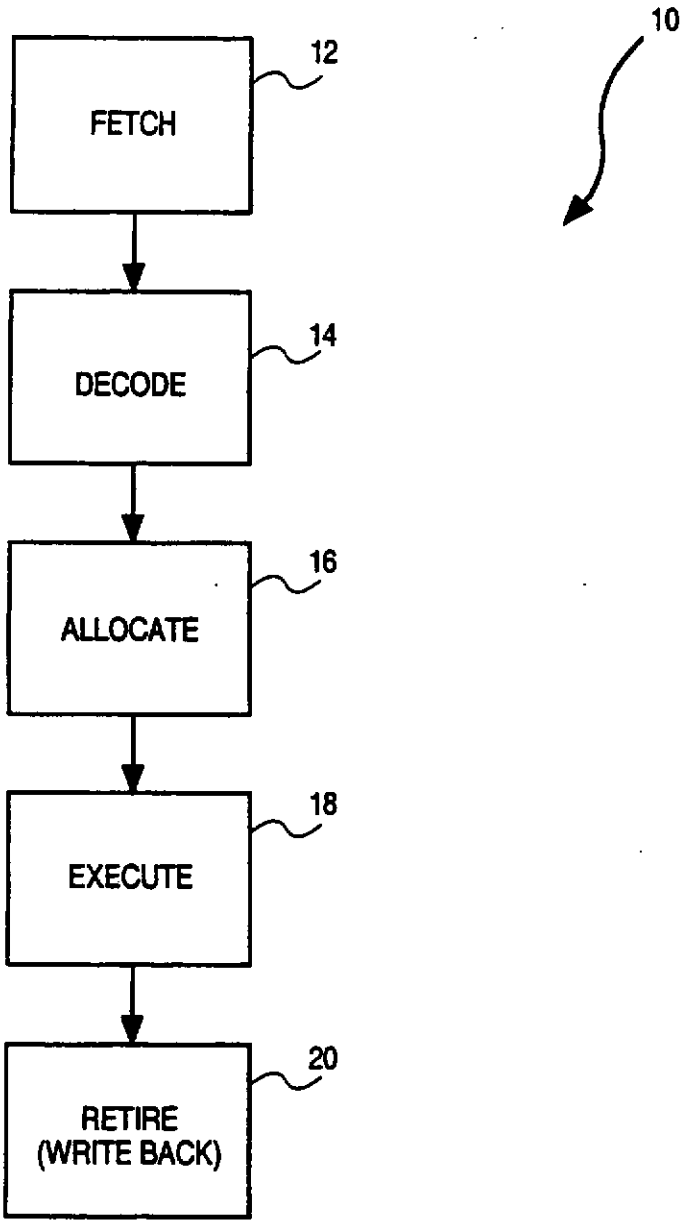

10
12
FETCH
14
DECODE
16
ALLOCATE
18
EXECUTE
20
RETIRE
(WRITE BACK)

FIG. 1

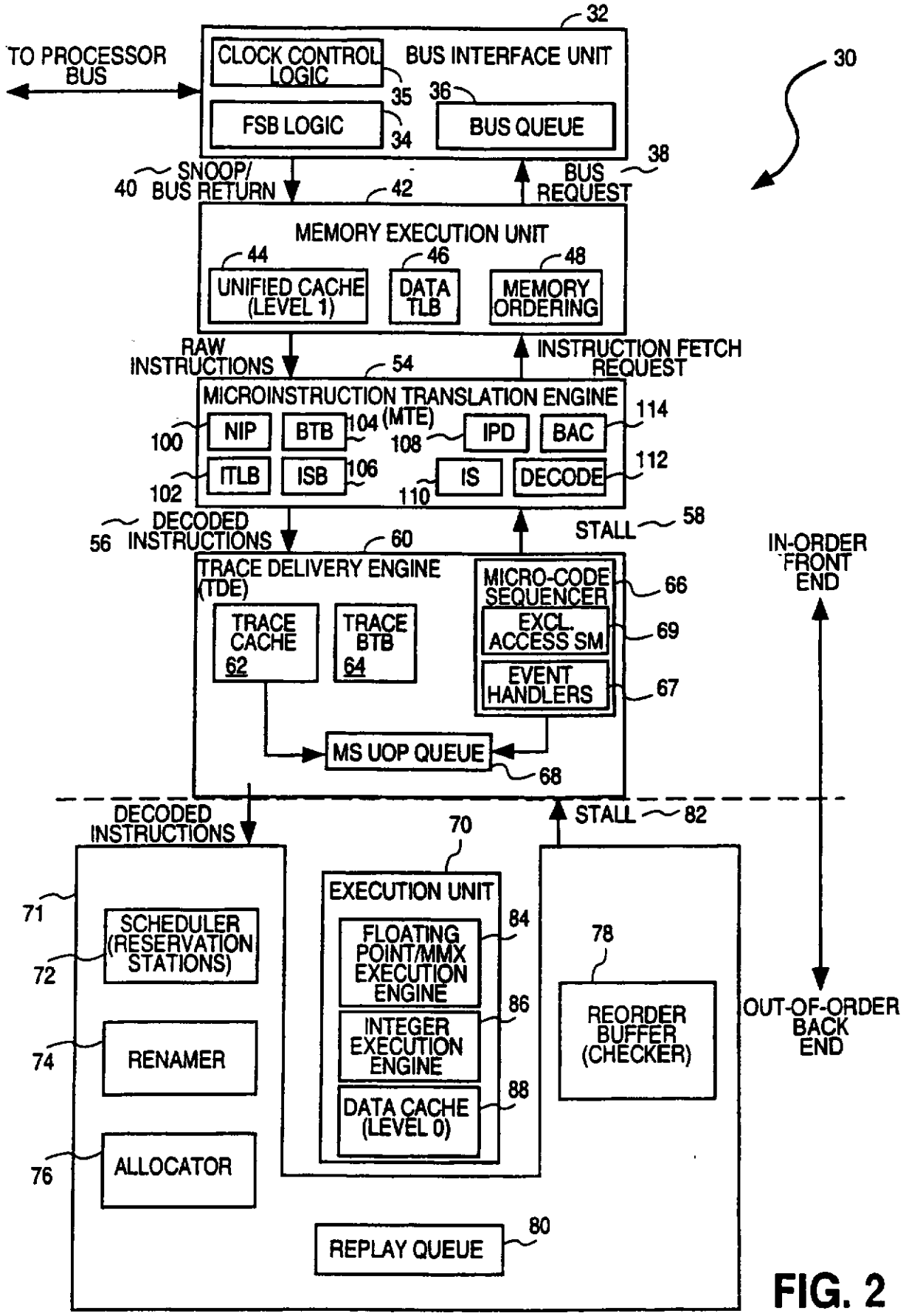

32
TO PROCESSOR BUS
CLOCK CONTROL LOGIC
BUS INTERFACE UNIT
35
36
FSB LOGIC
34
BUS QUEUE
30
38
40 SNOOP/ BUS RETURN
42
BUS REQUEST
MEMORY EXECUTION UNIT
44
46
48
UNIFIED CACHE (LEVEL 1)
DATA TLB
MEMORY ORDERING
RAW INSTRUCTIONS
54
INSTRUCTION FETCH REQUEST
MICROINSTRUCTION TRANSLATION ENGINE (MTE)
100
NIP
BTB
104
108
IPD
BAC
114
102
ITLB
ISB
106
110
IS
DECODE
112
56 DECODED INSTRUCTIONS
60
STALL
58
IN-ORDER FRONT END
TRACE DELIVERY ENGINE (TDE)
TRACE CACHE 62
TRACE BTB 64
MICRO-CODE SEQUENCER
66
EXCL. ACCESS SM
69
EVENT HANDLERS
67
MS UOP QUEUE
68
DECODED INSTRUCTIONS
STALL
82
70
71
EXECUTION UNIT
SCHEDULER (RESERVATION STATIONS)
84
78
72
FLOATING POINT/MMX EXECUTION ENGINE
74
RENAMER
86
INTEGER EXECUTION ENGINE
REORDER BUFFER (CHECKER)
OUT-OF-ORDER BACK END
88
DATA CACHE (LEVEL 0)
76
ALLOCATOR
80
REPLAY QUEUE

FIG. 2

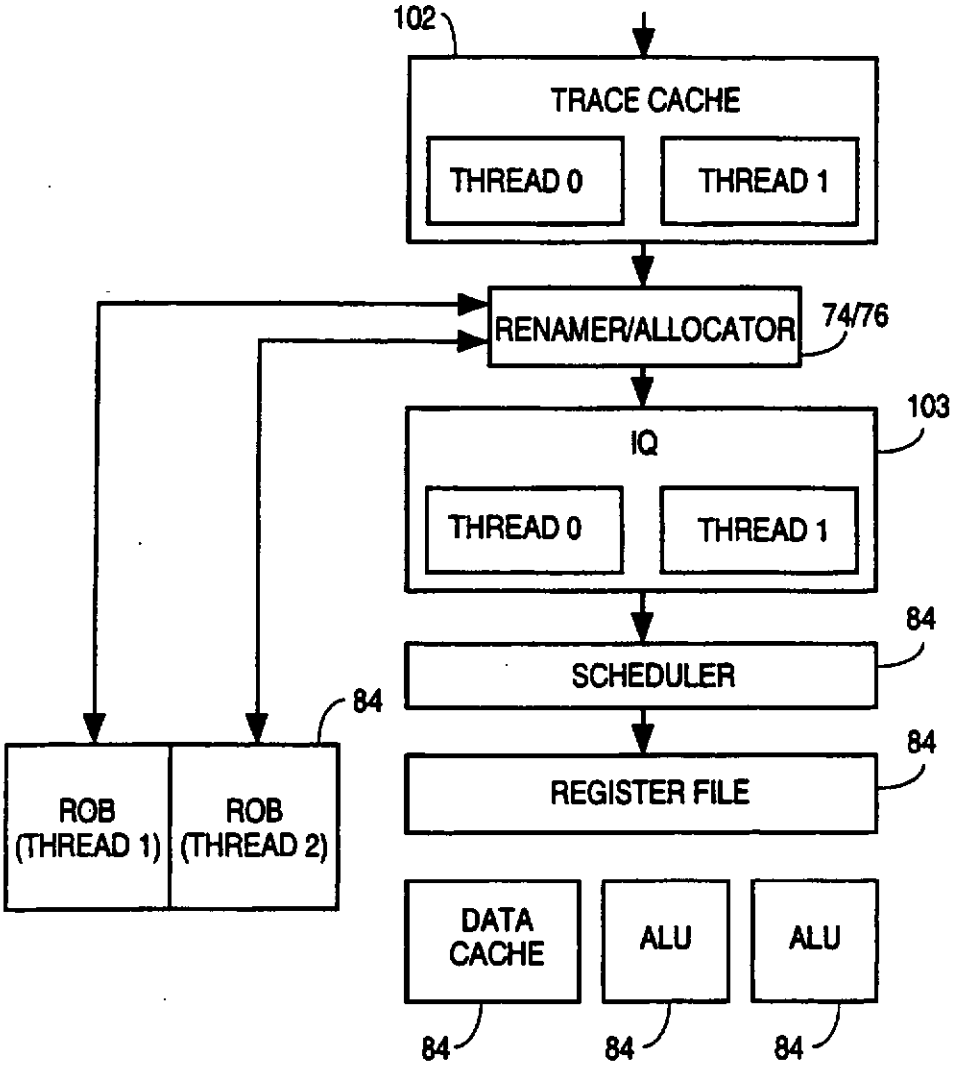

102
TRACE CACHE
THREAD 0
THREAD 1
RENAMER/ALLOCATOR
74/76
103
IQ
THREAD 0
THREAD 1
84
SCHEDULER
84
REGISTER FILE
84
ROB (THREAD 1)
ROB (THREAD 2)
DATA CACHE
ALU
ALU
84
84
84

FIG. 3

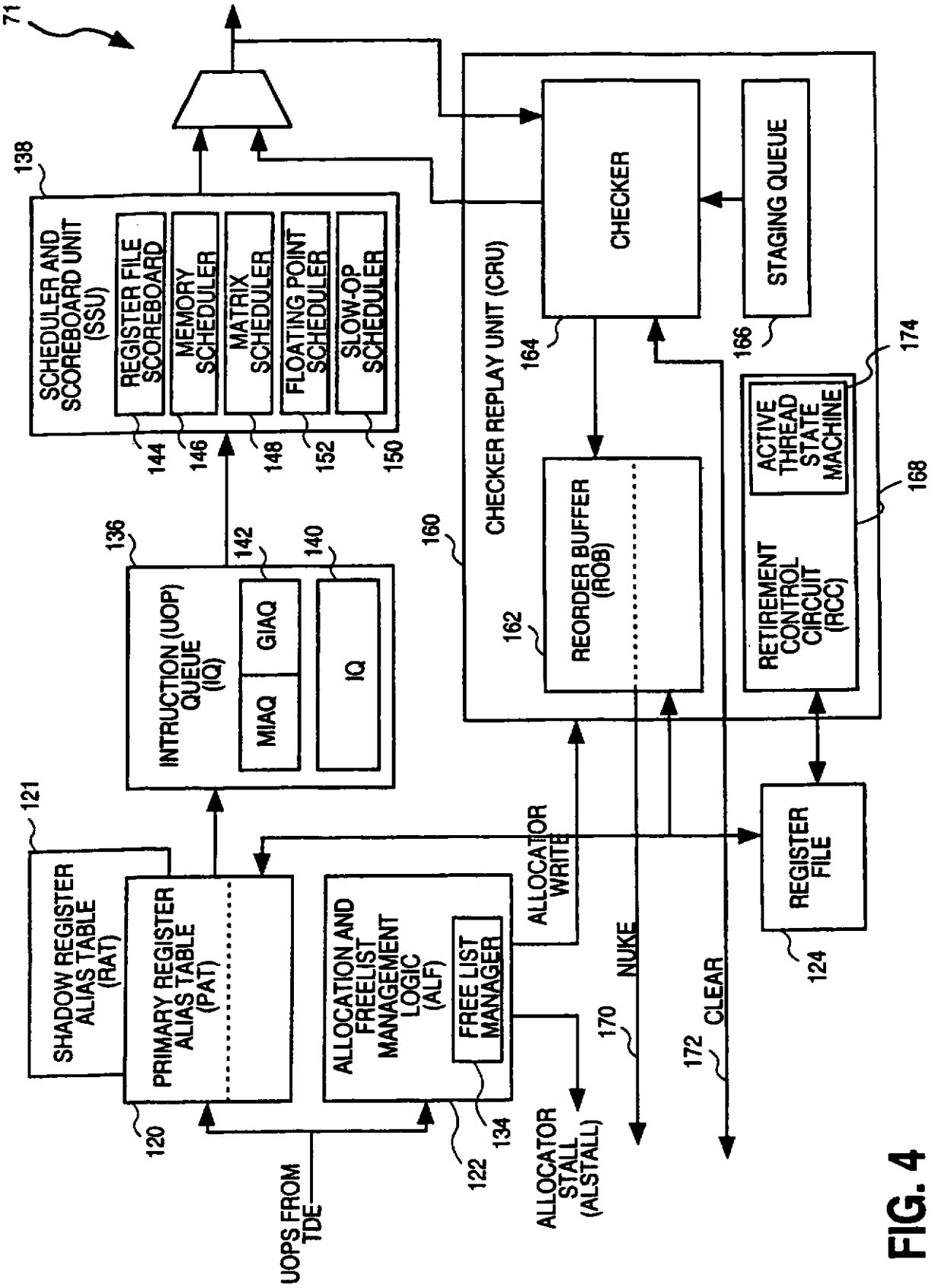

71
138
SCHEDULER AND SCOREBOARD UNIT (SSU)
REGISTER FILE SCOREBOARD
MEMORY SCHEDULER
MATRIX SCHEDULER
FLOATING POINT SCHEDULER
SLOW-OP SCHEDULER
144
146
148
152
150
136
142
140
INTRUCTION (UOP) QUEUE (IQ)
GIAQ
MIAQ
IQ
121
SHADOW REGISTER ALIAS TABLE (RAT)
PRIMARY REGISTER ALIAS TABLE (PAT)
120
ALLOCATION AND FREELIST MANAGEMENT LOGIC (ALF)
FREE LIST MANAGER
134
122
UOPS FROM TDE
ALLOCATOR STALL (ALSTALL)
ALLOCATOR WRITE
NUKE
170
CLEAR
172
160
CHECKER REPLAY UNIT (CRU)
CHECKER
164
STAGING QUEUE
166
REORDER BUFFER (ROB)
162
ACTIVE THREAD STATE MACHINE
174
RETIREMENT CONTROL CIRCUIT (RCC)
168
REGISTER FILE
124

FIG. 4

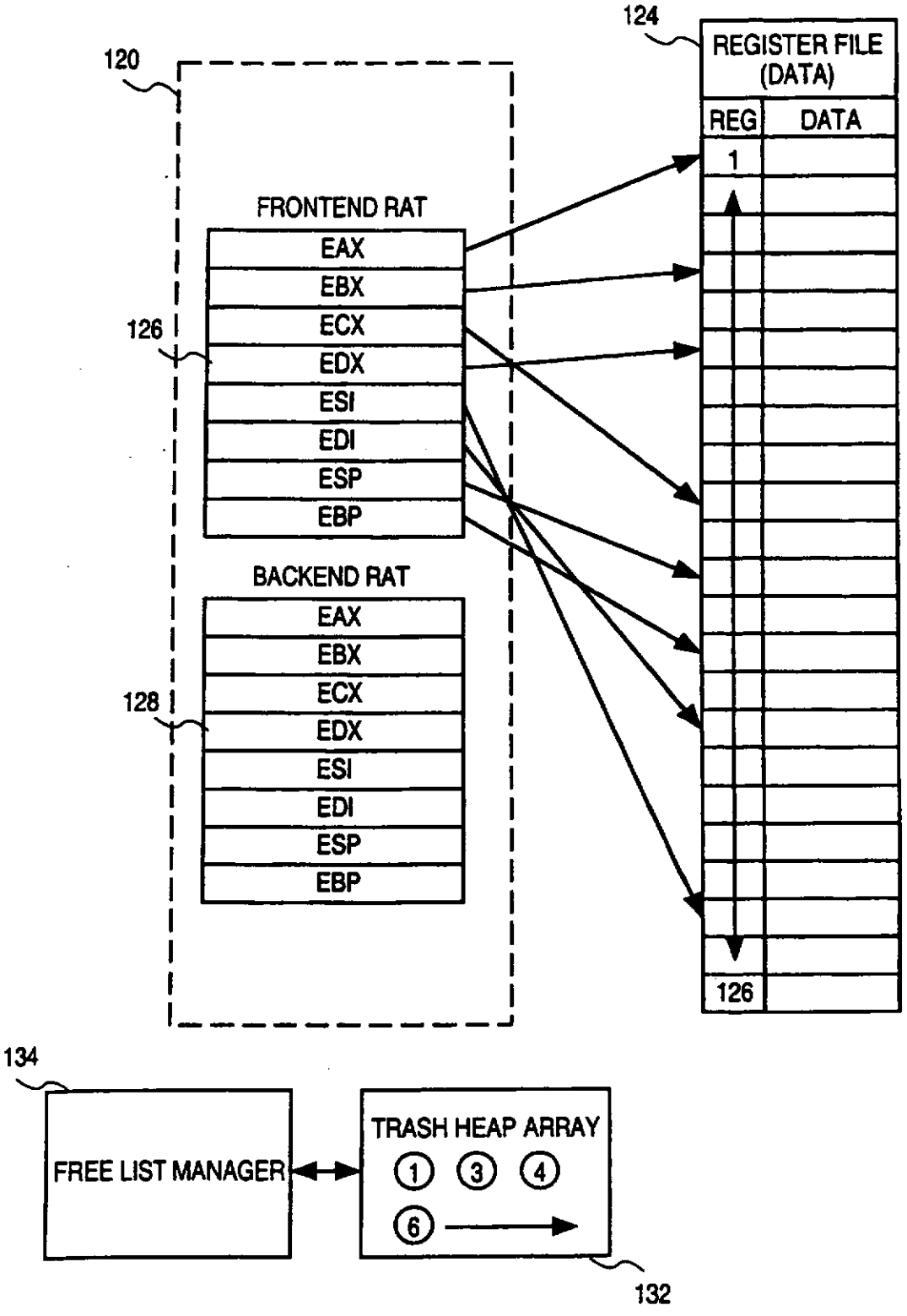
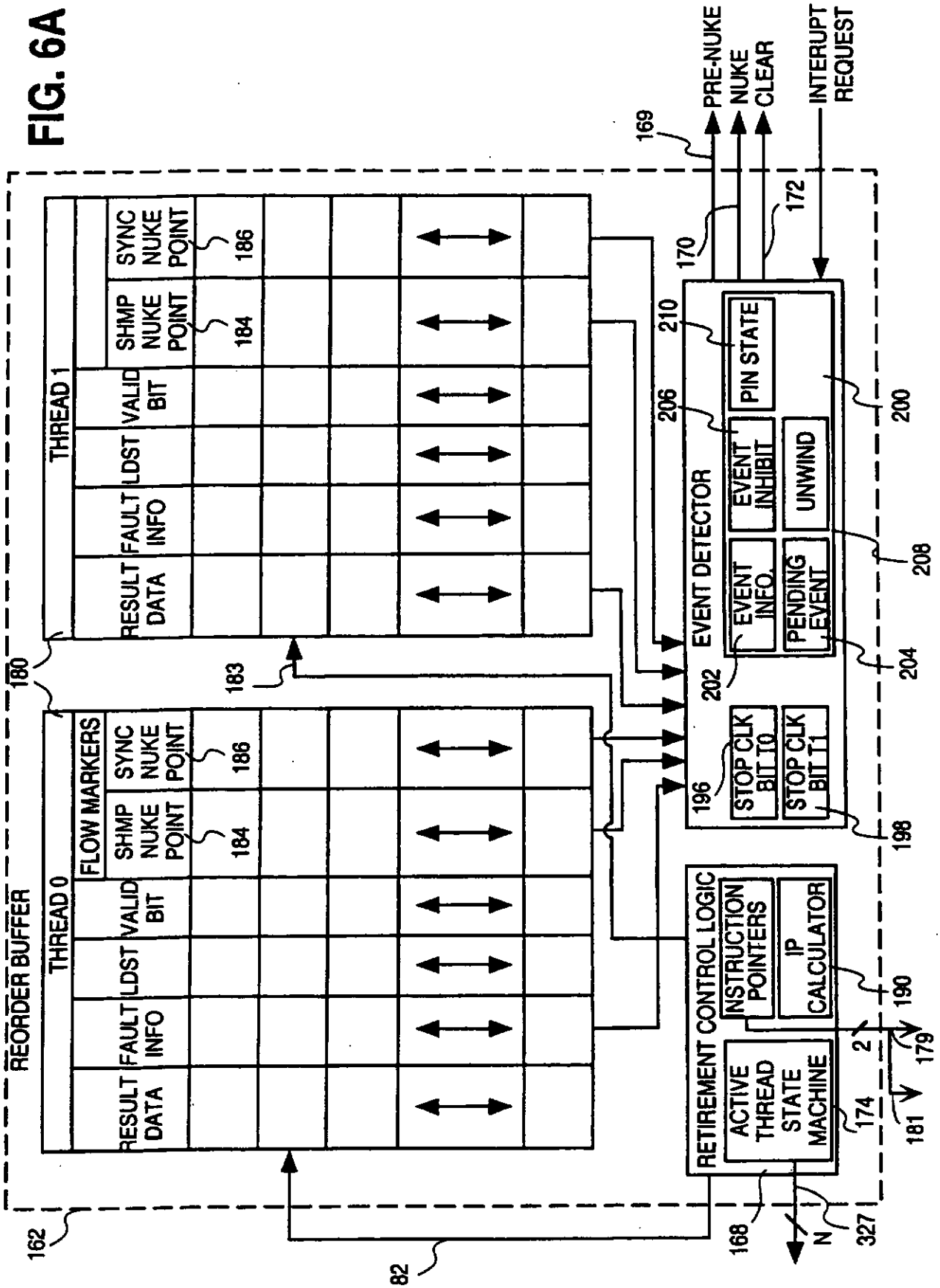

124
REGISTER FILE (DATA)
REG
DATA
1
126
120
FRONTEND RAT
EAX
EBX
ECX
EDX
ESI
EDI
ESP
EBP
126
BACKEND RAT
EAX
EBX
ECX
EDX
ESI
EDI
ESP
EBP
128
134
FREE LIST MANAGER
TRASH HEAP ARRAY
1
3
4
6
132

FIG. 5

FIG. 6A


REORDER BUFFER
162
THREAD 0
THREAD 1
RESULT DATA
FAULT INFO
LDST
VALID BIT
FLOW MARKERS
SHMP NUKE POINT
SYNC NUKE POINT
184
186
180
183
182
EVENT DETECTOR
202
EVENT INFO.
PENDING EVENT
204
208
EVENT INHIBIT
UNWIND
PIN STATE
206
210
200
STOP CLK BIT T0
STOP CLK BIT T1
196
198
RETIREMENT CONTROL LOGIC
ACTIVE THREAD STATE MACHINE
INSTRUCTION POINTERS
IP CALCULATOR
174
190
179
181
168
N
327
169
170
172
PRE-NUKE
NUKE CLEAR
INTERUPT REQUEST

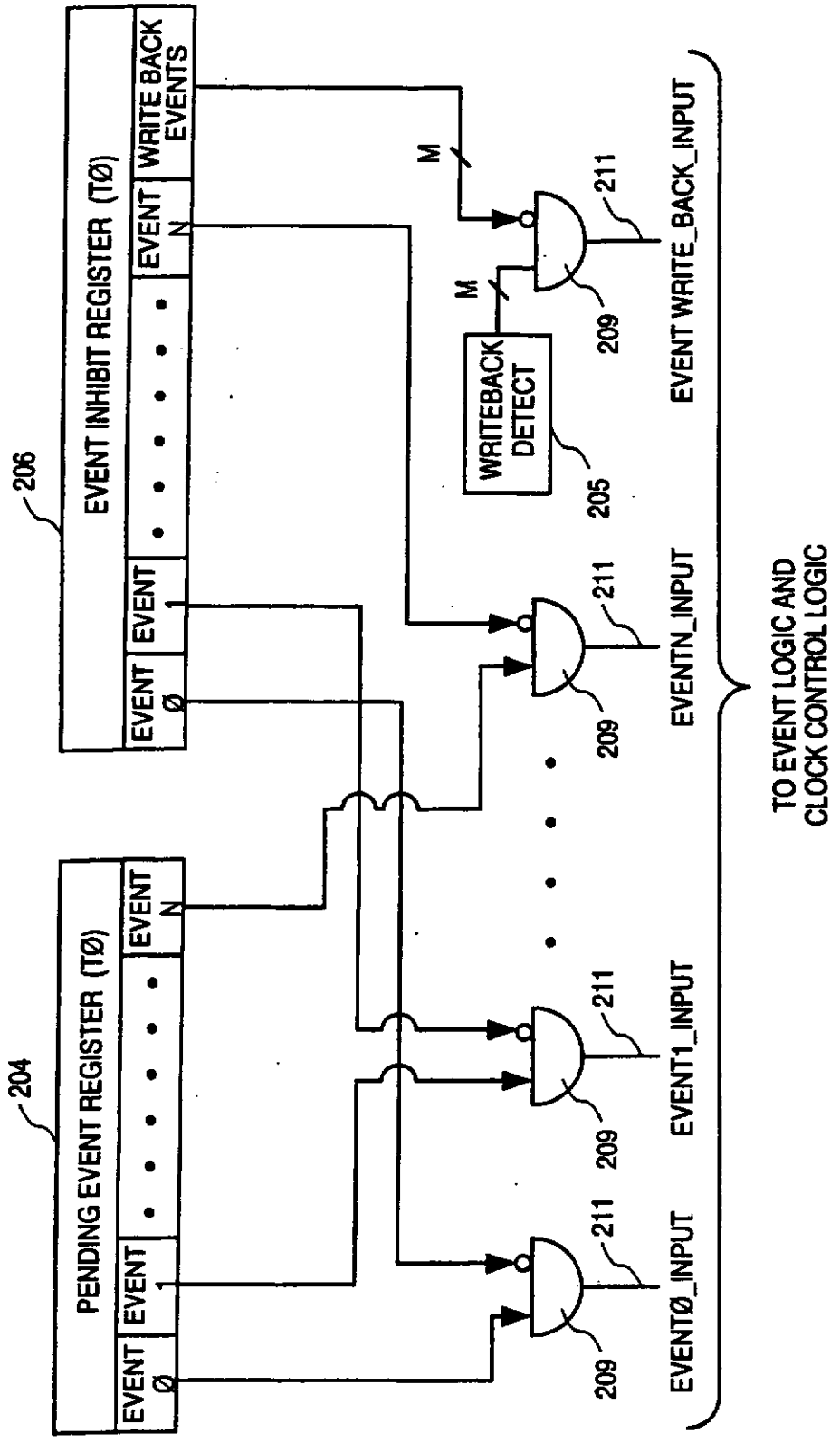

206
EVENT INHIBIT REGISTER (TØ)
EVENT Ø
EVENT 1
EVENT N
WRITE BACK EVENTS
M
M
WRITEBACK DETECT
205
209
211
EVENT WRITE_BACK_INPUT
204
PENDING EVENT REGISTER (TØ)
EVENT Ø
EVENT 1
EVENT N
EVENTØ_INPUT
EVENT1_INPUT
EVENTN_INPUT
TO EVENT LOGIC AND CLOCK CONTROL LOGIC

FIG. 6B

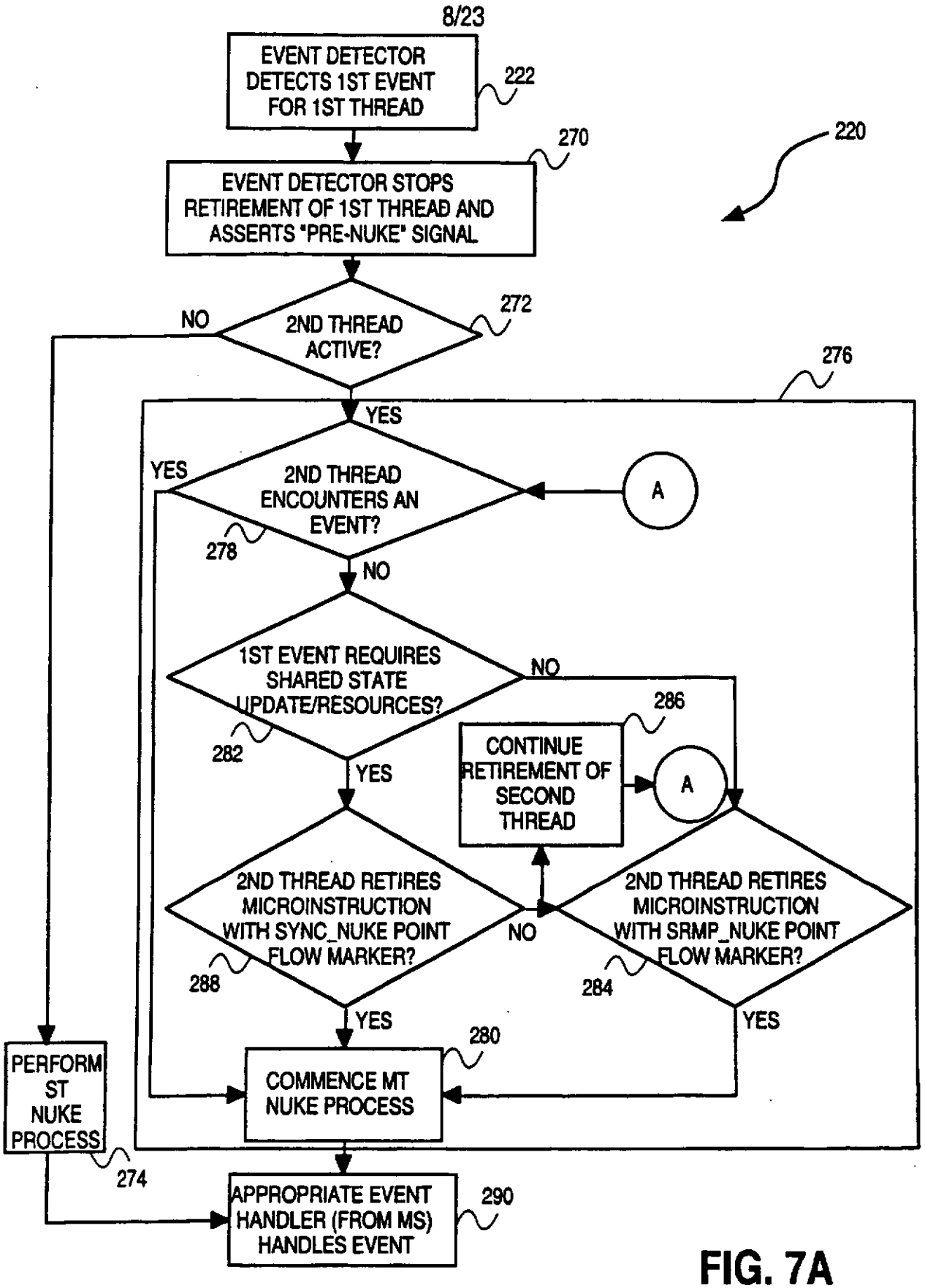

EVENT DETECTOR DETECTS 1ST EVENT FOR 1ST THREAD
222
220
270
EVENT DETECTOR STOPS RETIREMENT OF 1ST THREAD AND ASSERTS "PRE-NUKE" SIGNAL
NO
2ND THREAD ACTIVE?
272
276
YES
YES
2ND THREAD ENCOUNTERS AN EVENT?
A
278
NO
1ST EVENT REQUIRES SHARED STATE UPDATE/RESOURCES?
NO
286
282
YES
CONTINUE RETIREMENT OF SECOND THREAD
A
2ND THREAD RETIRES MICROINSTRUCTION WITH SYNC_NUKE POINT FLOW MARKER?
NO
2ND THREAD RETIRES MICROINSTRUCTION WITH SRMP_NUKE POINT FLOW MARKER?
288
284
YES
YES
280
PERFORM ST NUKE PROCESS
COMMENCE MT NUKE PROCESS
274
APPROPRIATE EVENT HANDLER (FROM MS) HANDLES EVENT
290

FIG. 7A

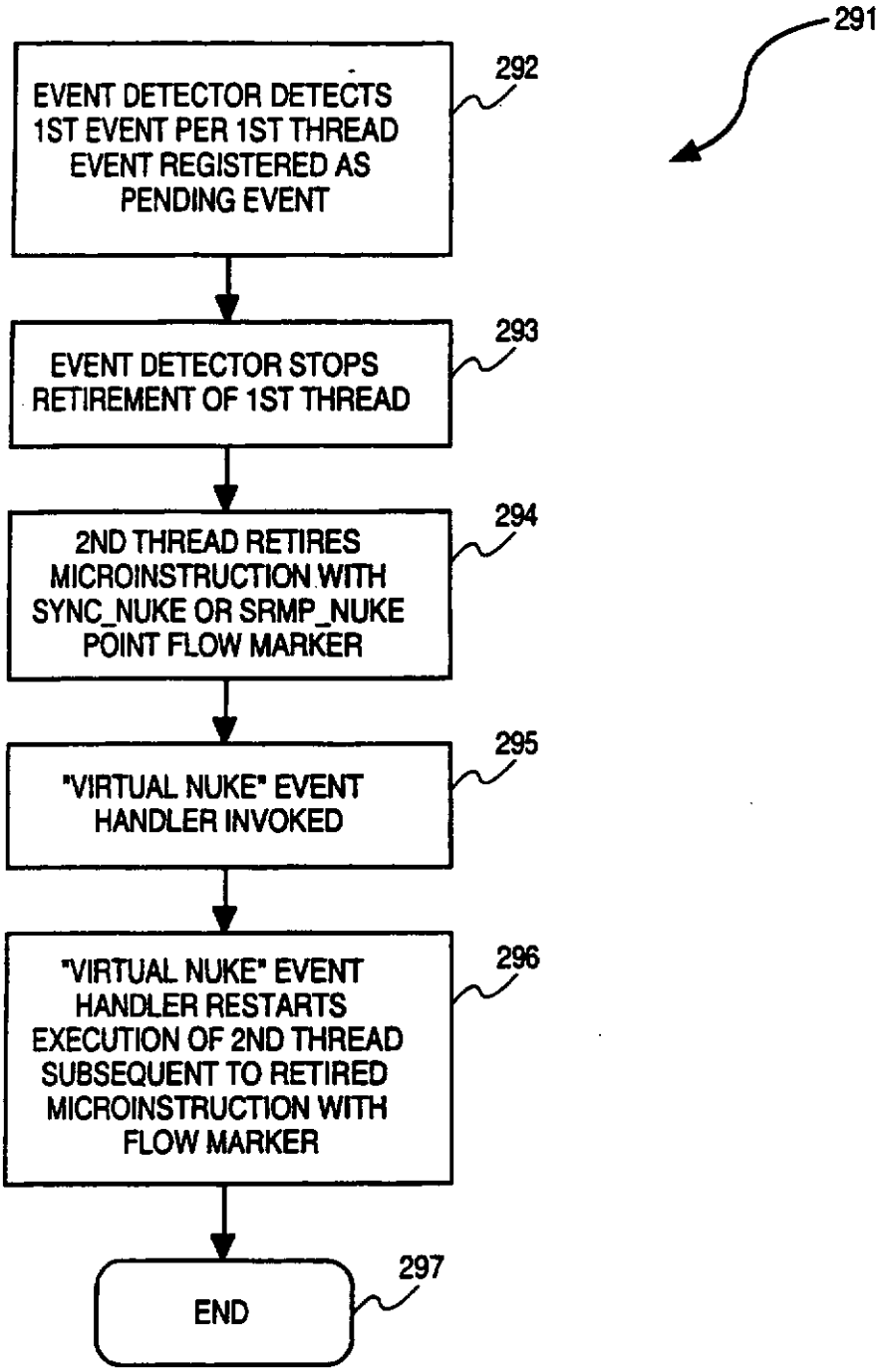

291
EVENT DETECTOR DETECTS 1ST EVENT PER 1ST THREAD EVENT REGISTERED AS PENDING EVENT
292
EVENT DETECTOR STOPS RETIREMENT OF 1ST THREAD
293
2ND THREAD RETIRES MICROINSTRUCTION WITH SYNC_NUKE OR SRMP_NUKE POINT FLOW MARKER
294
"VIRTUAL NUKE" EVENT HANDLER INVOKED
295
"VIRTUAL NUKE" EVENT HANDLER RESTARTS EXECUTION OF 2ND THREAD SUBSEQUENT TO RETIRED MICROINSTRUCTION WITH FLOW MARKER
296
END
297

FIG. 7B

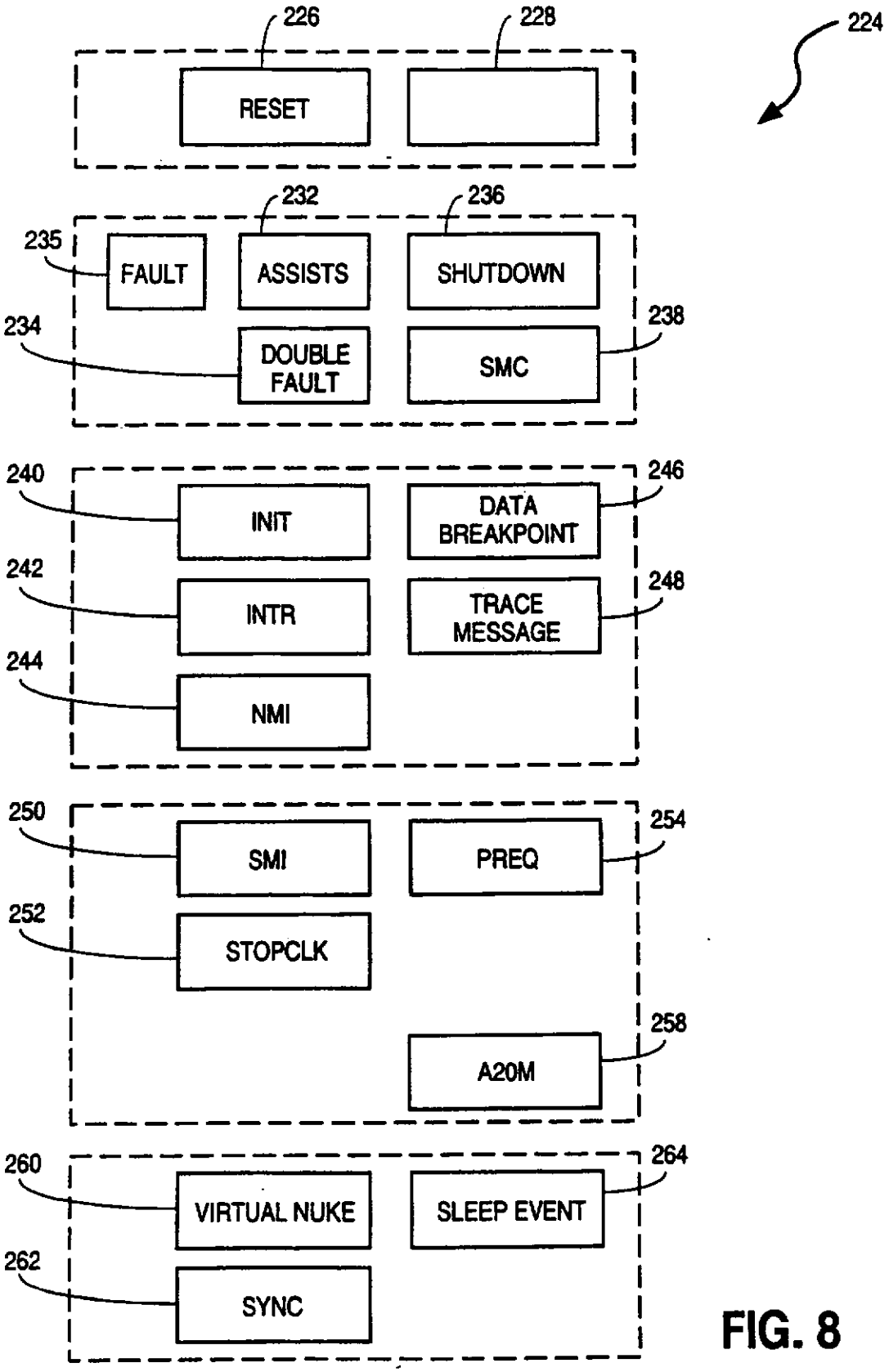

224
226
228
RESET
232
236
235
FAULT
ASSISTS
SHUTDOWN
238
234
DOUBLE FAULT
SMC
240
246
INIT
DATA BREAKPOINT
242
248
INTR
TRACE MESSAGE
244
NMI
250
254
SMI
PREQ
252
STOPCLK
258
A20M
260
264
VIRTUAL NUKE
SLEEP EVENT
262
SYNC

FIG. 8

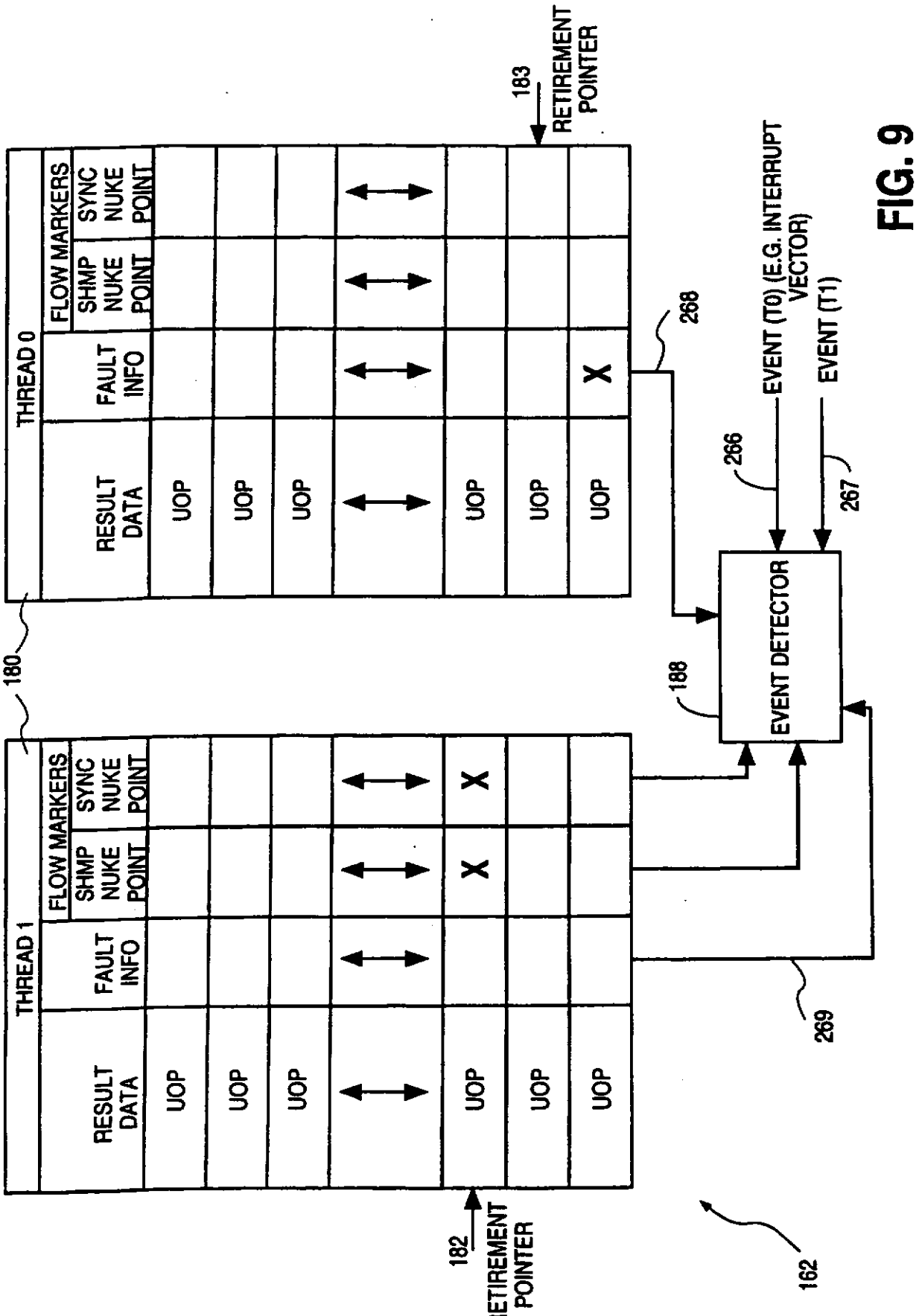

THREAD 0
RESULT DATA
FAULT INFO
FLOW MARKERS
SHMP NUKE POINT
SYNC NUKE POINT
UOP
183
RETIREMENT POINTER
180
THREAD 1
182
RETIREMENT POINTER
268
269
188
EVENT DETECTOR
266
267
EVENT (T0) (E.G. INTERRUPT VECTOR)
EVENT (T1)
162

FIG. 9

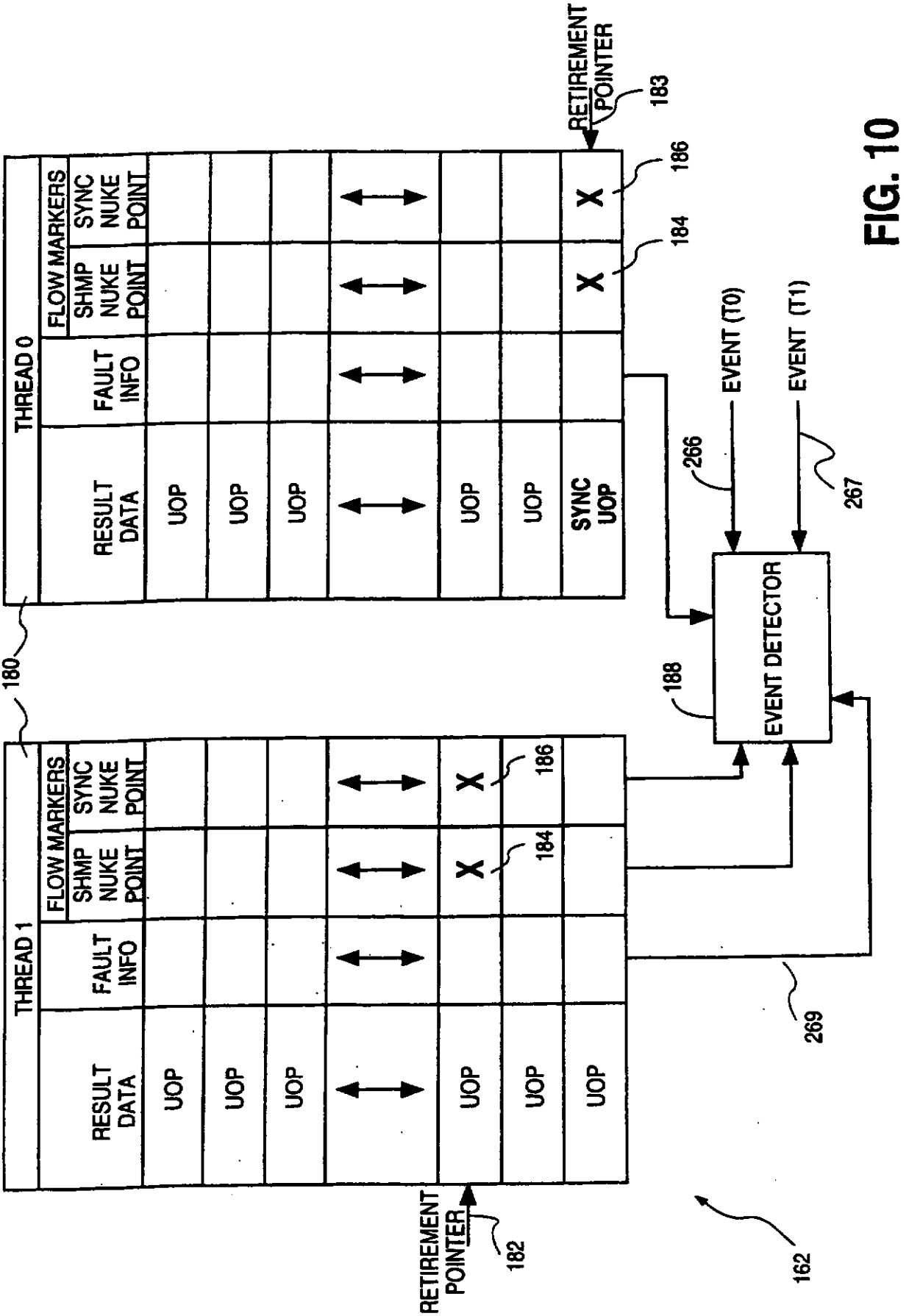

THREAD 0
RESULT DATA
FAULT INFO
FLOW MARKERS
SHMP NUKE POINT
SYNC NUKE POINT
UOP
SYNC UOP
RETIREMENT POINTER
183
186
184
180
THREAD 1
RETIREMENT POINTER
182
EVENT (T0)
EVENT (T1)
266
267
EVENT DETECTOR
188
269
162

FIG. 10

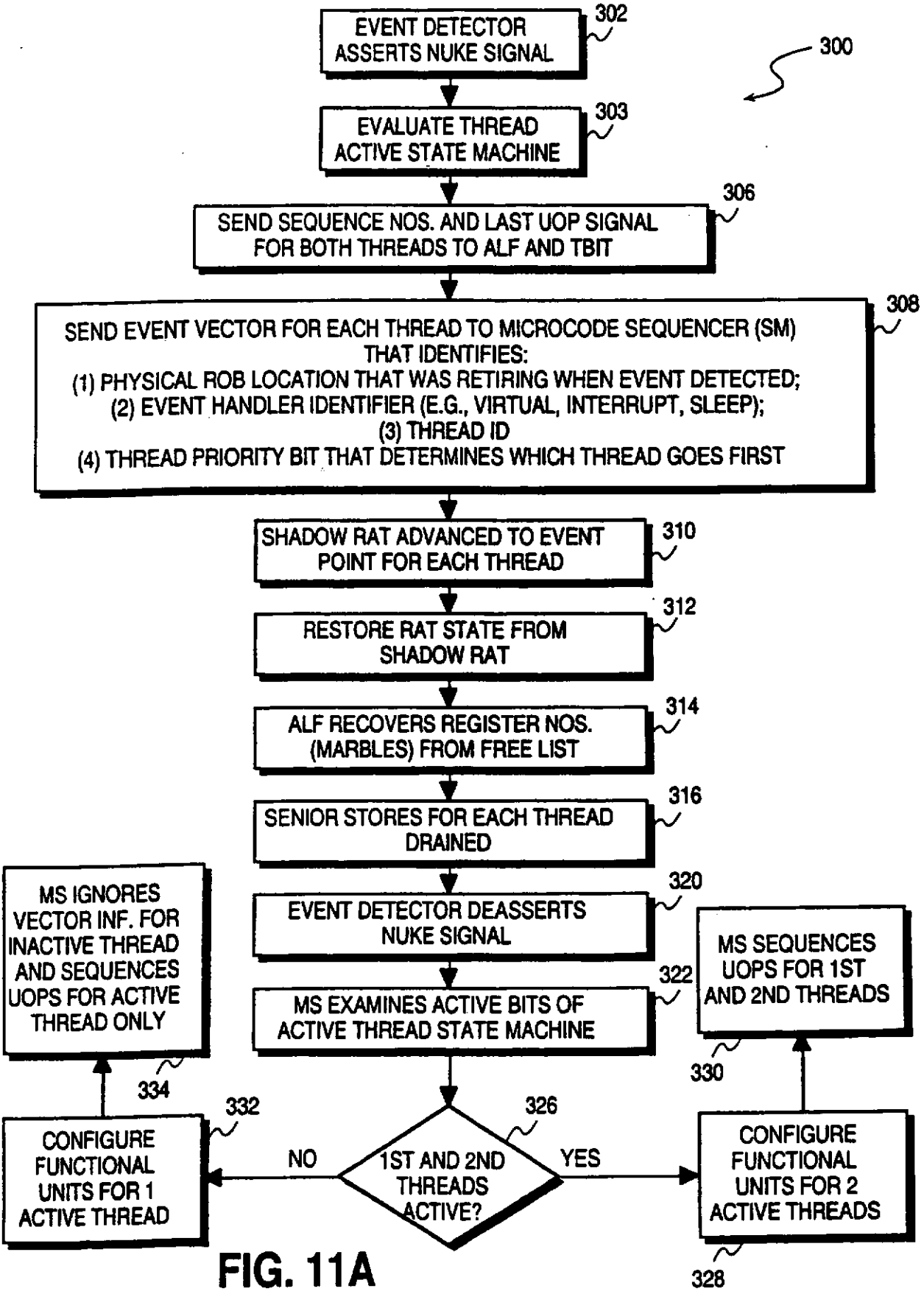

EVENT DETECTOR ASSERTS NUKE SIGNAL
302
300
EVALUATE THREAD ACTIVE STATE MACHINE
303
SEND SEQUENCE NOS. AND LAST UOP SIGNAL FOR BOTH THREADS TO ALF AND TBIT
306
SEND EVENT VECTOR FOR EACH THREAD TO MICROCODE SEQUENCER (SM) THAT IDENTIFIES:
(1) PHYSICAL ROB LOCATION THAT WAS RETIRING WHEN EVENT DETECTED;
(2) EVENT HANDLER IDENTIFIER (E.G., VIRTUAL, INTERRUPT, SLEEP);
(3) THREAD ID
(4) THREAD PRIORITY BIT THAT DETERMINES WHICH THREAD GOES FIRST
308
SHADOW RAT ADVANCED TO EVENT POINT FOR EACH THREAD
310
RESTORE RAT STATE FROM SHADOW RAT
312
ALF RECOVERS REGISTER NOS. (MARBLES) FROM FREE LIST
314
SENIOR STORES FOR EACH THREAD DRAINED
316
EVENT DETECTOR DEASSERTS NUKE SIGNAL
320
MS EXAMINES ACTIVE BITS OF ACTIVE THREAD STATE MACHINE
322
1ST AND 2ND THREADS ACTIVE?
326
NO
YES
MS IGNORES VECTOR INF. FOR INACTIVE THREAD AND SEQUENCES UOPS FOR ACTIVE THREAD ONLY
334
CONFIGURE FUNCTIONAL UNITS FOR 1 ACTIVE THREAD
332
MS SEQUENCES UOPS FOR 1ST AND 2ND THREADS
330
CONFIGURE FUNCTIONAL UNITS FOR 2 ACTIVE THREADS
328

FIG. 11A

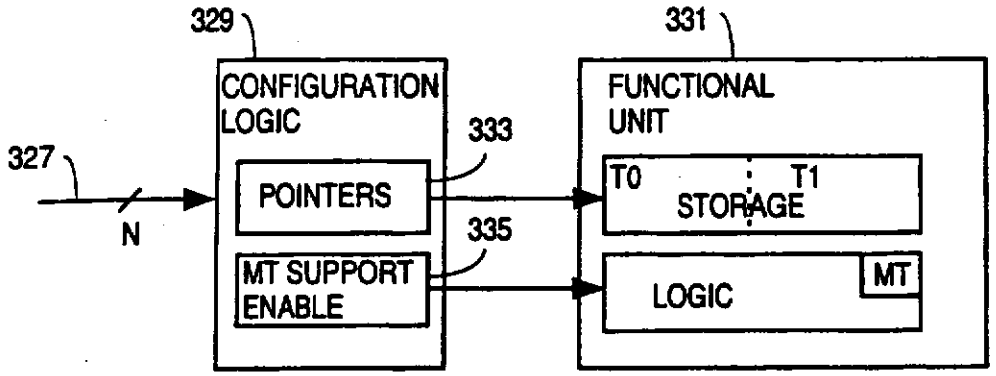

329
331
CONFIGURATION LOGIC
FUNCTIONAL UNIT
327
N
333
335
POINTERS
MT SUPPORT ENABLE
T0
T1
STORAGE
LOGIC
MT

FIG. 11B

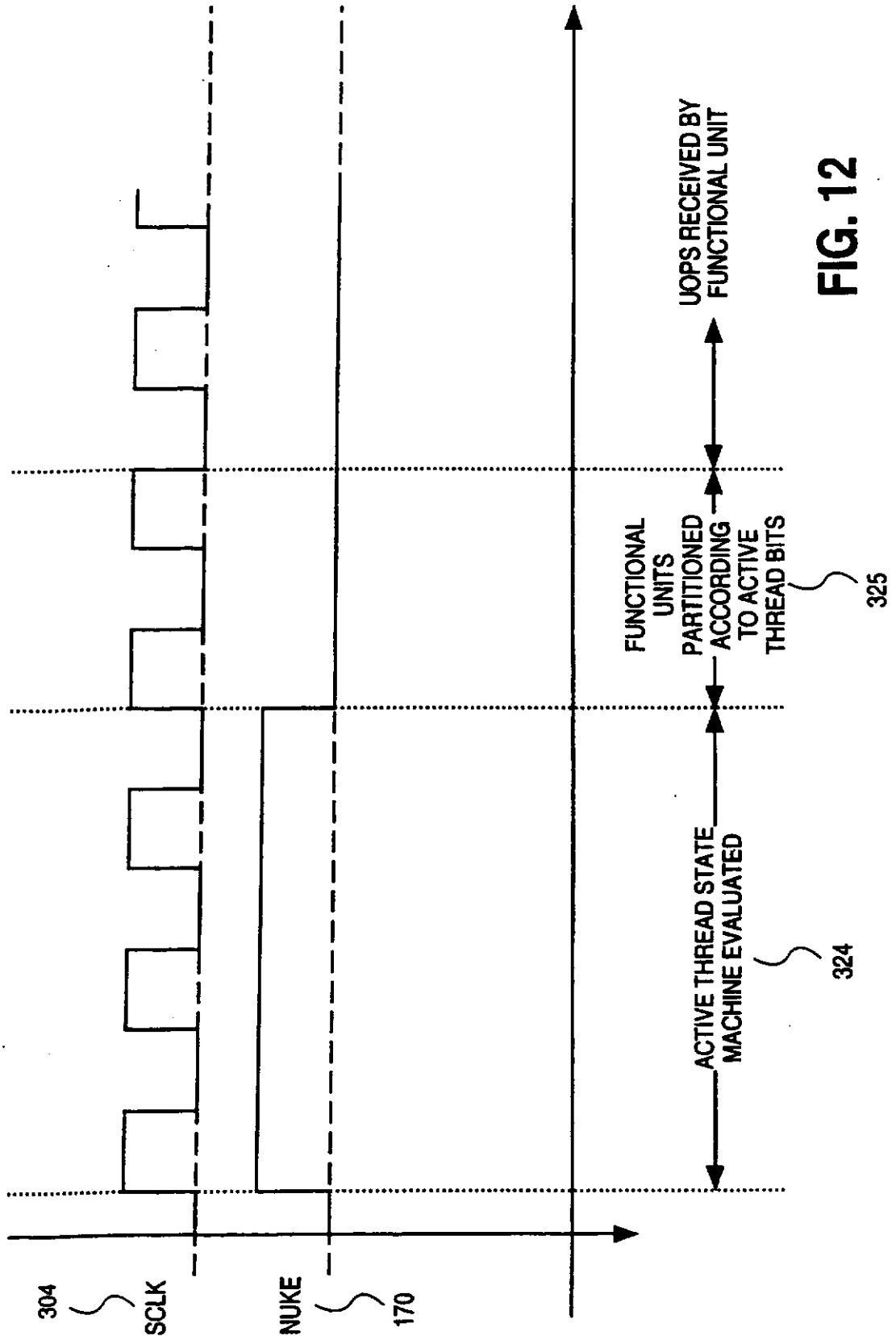

304
SCLK
NUKE
170
ACTIVE THREAD STATE MACHINE EVALUATED
324
FUNCTIONAL UNITS PARTITIONED ACCORDING TO ACTIVE THREAD BITS
325
UOPS RECEIVED BY FUNCTIONAL UNIT

FIG. 12

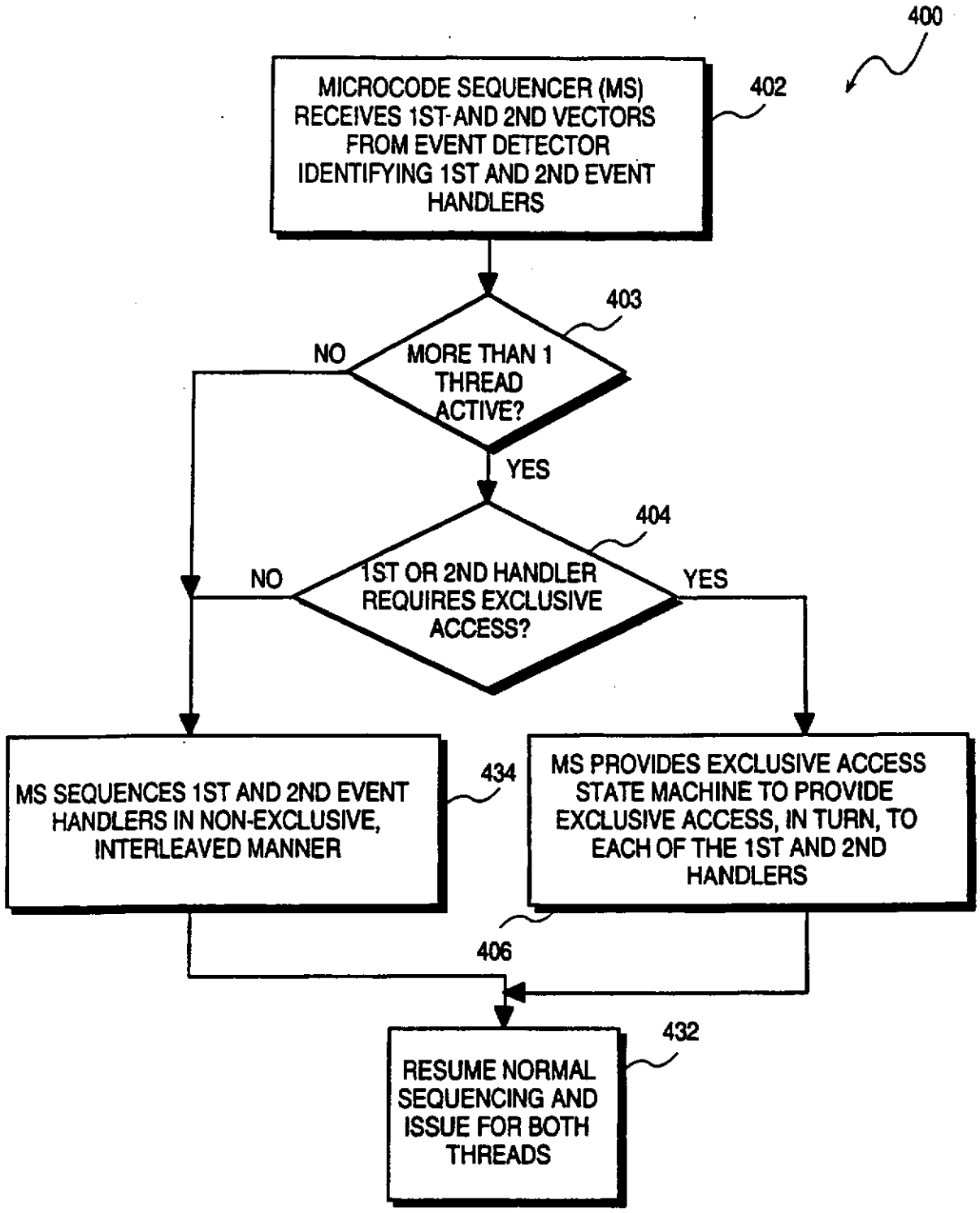

400
MICROCODE SEQUENCER (MS) RECEIVES 1ST-AND 2ND VECTORS FROM EVENT DETECTOR IDENTIFYING 1ST AND 2ND EVENT HANDLERS
402
403
MORE THAN 1 THREAD ACTIVE?
NO
YES
404
1ST OR 2ND HANDLER REQUIRES EXCLUSIVE ACCESS?
NO
YES
MS SEQUENCES 1ST AND 2ND EVENT HANDLERS IN NON-EXCLUSIVE, INTERLEAVED MANNER
434
MS PROVIDES EXCLUSIVE ACCESS STATE MACHINE TO PROVIDE EXCLUSIVE ACCESS, IN TURN, TO EACH OF THE 1ST AND 2ND HANDLERS
406
RESUME NORMAL SEQUENCING AND ISSUE FOR BOTH THREADS
432

FIG. 13

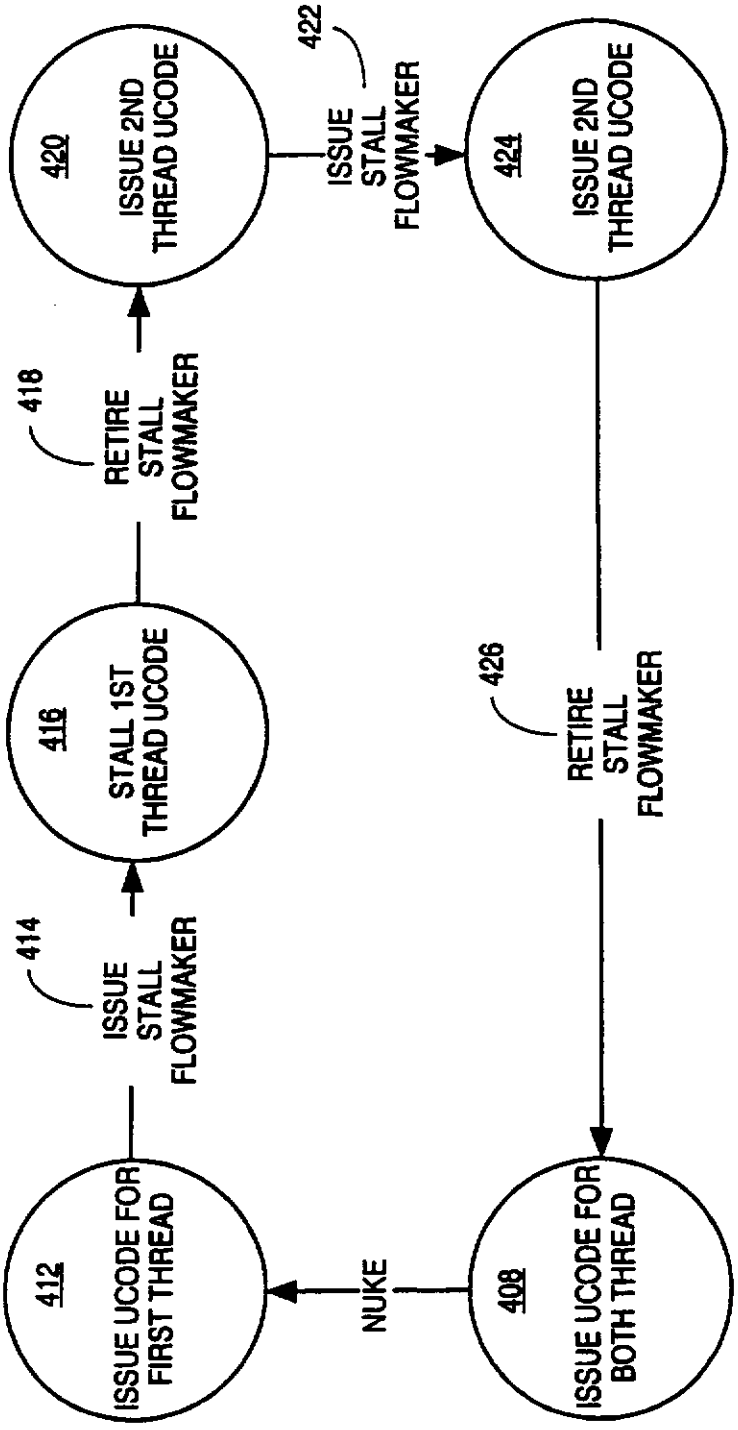

408
ISSUE UCODE FOR BOTH THREAD
NUKE
412
ISSUE UCODE FOR FIRST THREAD
414
ISSUE STALL FLOWMAKER
416
STALL 1ST THREAD UCODE
418
RETIRE STALL FLOWMAKER
420
ISSUE 2ND THREAD UCODE
422
ISSUE STALL FLOWMAKER
424
ISSUE 2ND THREAD UCODE
426
RETIRE STALL FLOWMAKER

FIG. 14

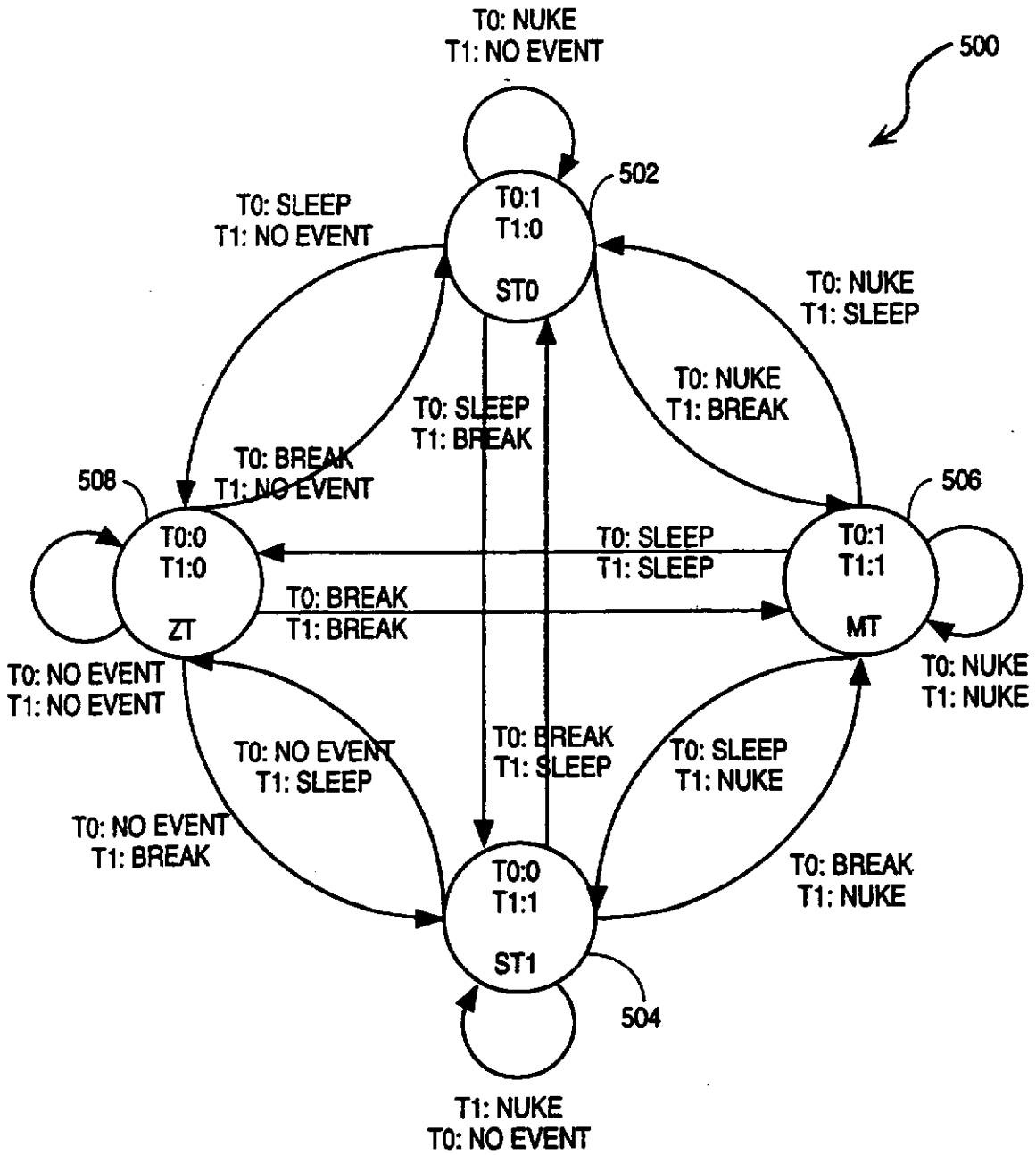

T0: NUKE
T1: NO EVENT
500
502
T0:1
T1:0
ST0
T0: SLEEP
T1: NO EVENT
T0: NUKE
T1: SLEEP
T0: NUKE
T1: BREAK
T0: SLEEP
T1: BREAK
T0: BREAK
T1: NO EVENT
508
506
T0:0
T1:0
ZT
T0: SLEEP
T1: SLEEP
T0:1
T1:1
MT
T0: BREAK
T1: BREAK
T0: NO EVENT
T1: NO EVENT
T0: NUKE
T1: NUKE
T0: NO EVENT
T1: SLEEP
T0: BREAK
T1: SLEEP
T0: SLEEP
T1: NUKE
T0: NO EVENT
T1: BREAK
T0: BREAK
T1: NUKE
T0:0
T1:1
ST1
504
T1: NUKE
T0: NO EVENT

FIG. 15

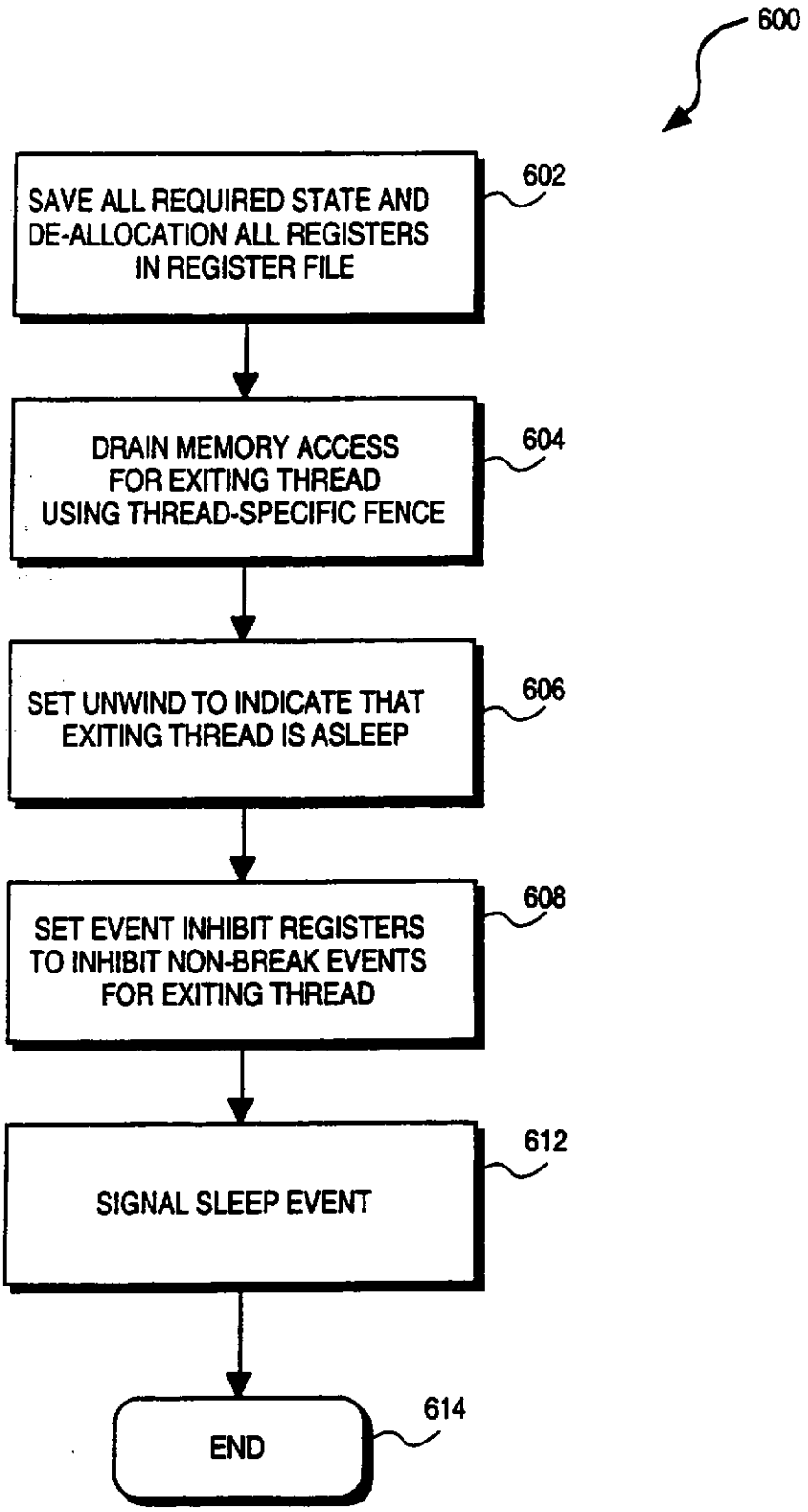

600
SAVE ALL REQUIRED STATE AND DE-ALLOCATION ALL REGISTERS IN REGISTER FILE
602
DRAIN MEMORY ACCESS FOR EXITING THREAD USING THREAD-SPECIFIC FENCE
604
SET UNWIND TO INDICATE THAT EXITING THREAD IS ASLEEP
606
SET EVENT INHIBIT REGISTERS TO INHIBIT NON-BREAK EVENTS FOR EXITING THREAD
608
SIGNAL SLEEP EVENT
612
END
614

FIG. 16A

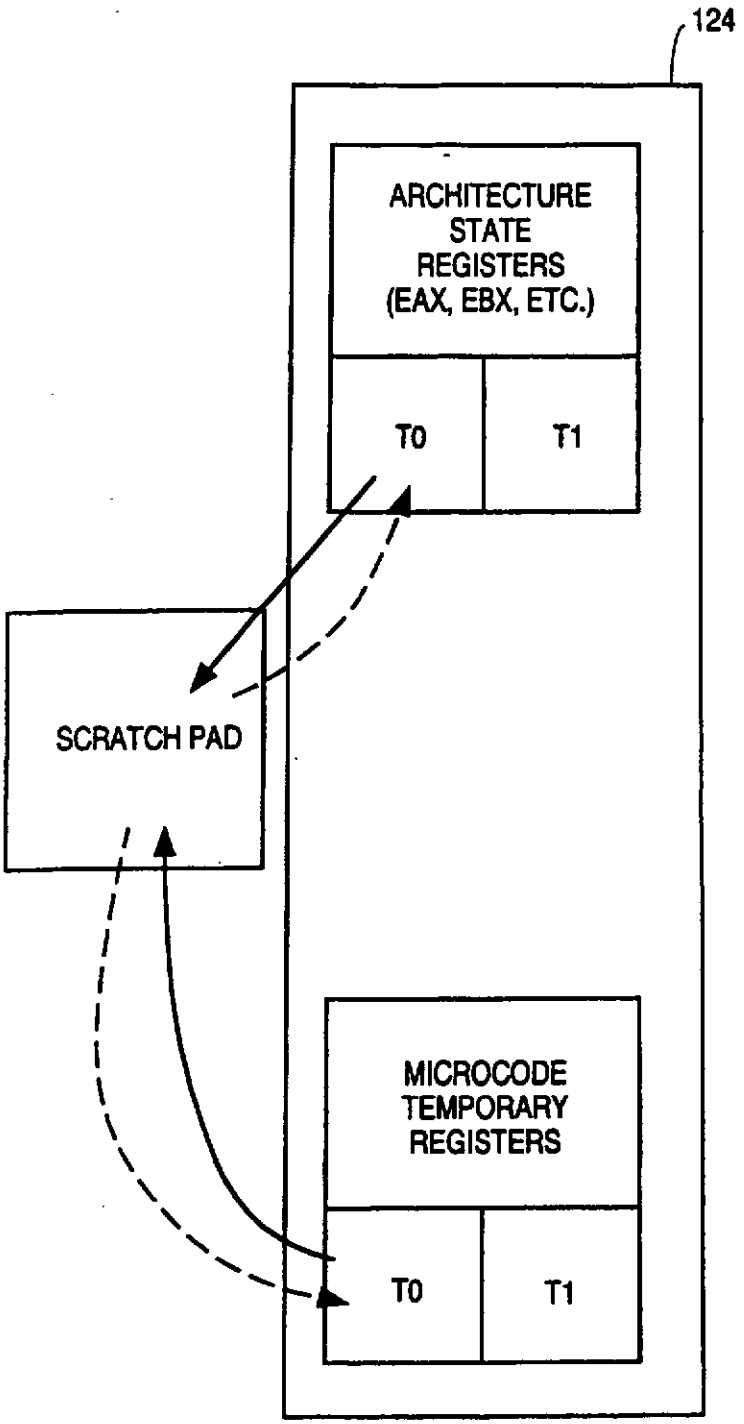

124
ARCHITECTURE STATE REGISTERS (EAX, EBX, ETC.)
T0
T1
SCRATCH PAD
MICROCODE TEMPORARY REGISTERS
T0
T1

FIG. 16B

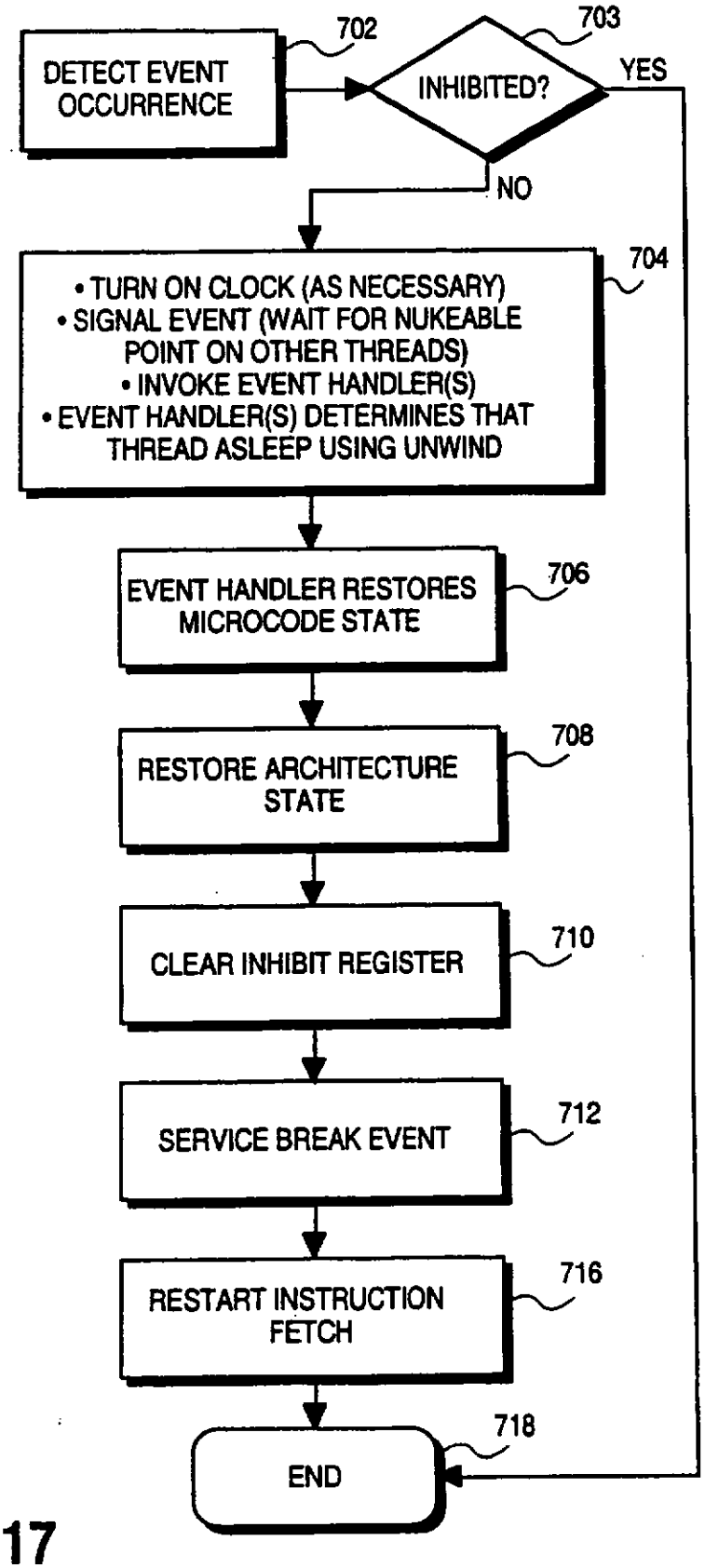

DETECT EVENT OCCURRENCE
702
INHIBITED?
703
YES
NO
• TURN ON CLOCK (AS NECESSARY)
• SIGNAL EVENT (WAIT FOR NUKEABLE POINT ON OTHER THREADS)
• INVOKE EVENT HANDLER(S)
• EVENT HANDLER(S) DETERMINES THAT THREAD ASLEEP USING UNWIND
704
EVENT HANDLER RESTORES MICROCODE STATE
706
RESTORE ARCHITECTURE STATE
708
CLEAR INHIBIT REGISTER
710
SERVICE BREAK EVENT
712
RESTART INSTRUCTION FETCH
716
END
718

FIG. 17

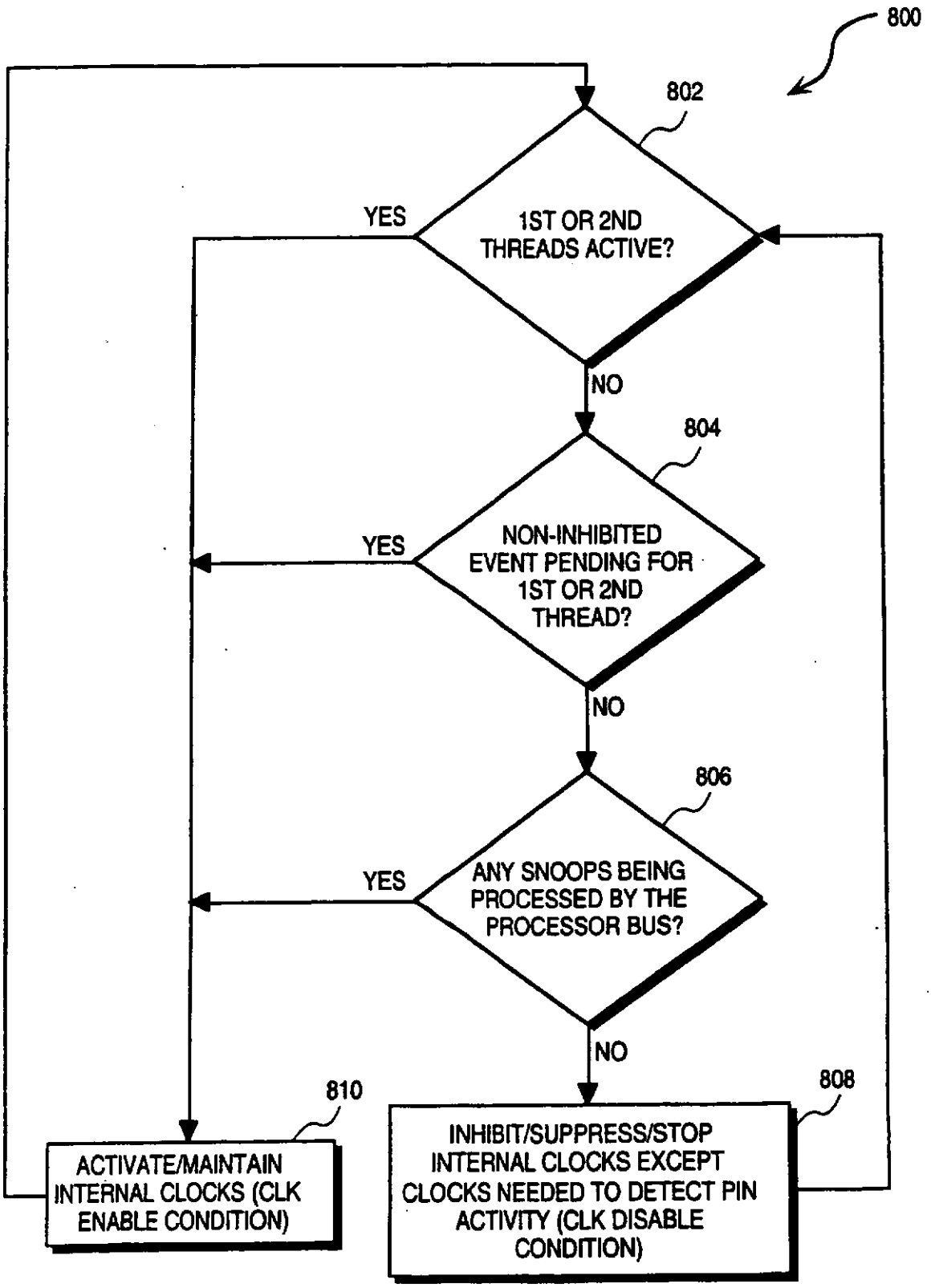

800
802
1ST OR 2ND THREADS ACTIVE?
YES
NO
804
NON-INHIBITED EVENT PENDING FOR 1ST OR 2ND THREAD?
YES
NO
806
ANY SNOOPS BEING PROCESSED BY THE PROCESSOR BUS?
YES
NO
808
INHIBIT/SUPPRESS/STOP INTERNAL CLOCKS EXCEPT CLOCKS NEEDED TO DETECT PIN ACTIVITY (CLK DISABLE CONDITION)
810
ACTIVATE/MAINTAIN INTERNAL CLOCKS (CLK ENABLE CONDITION)

FIG. 18

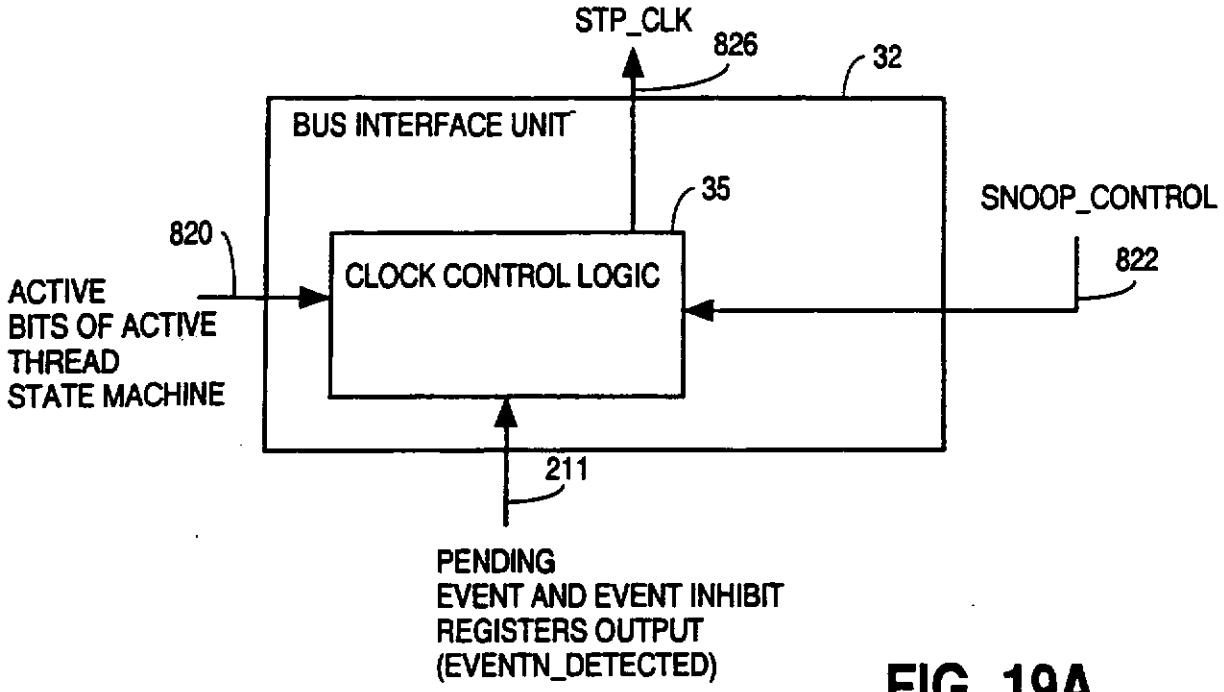


FIG. 19A

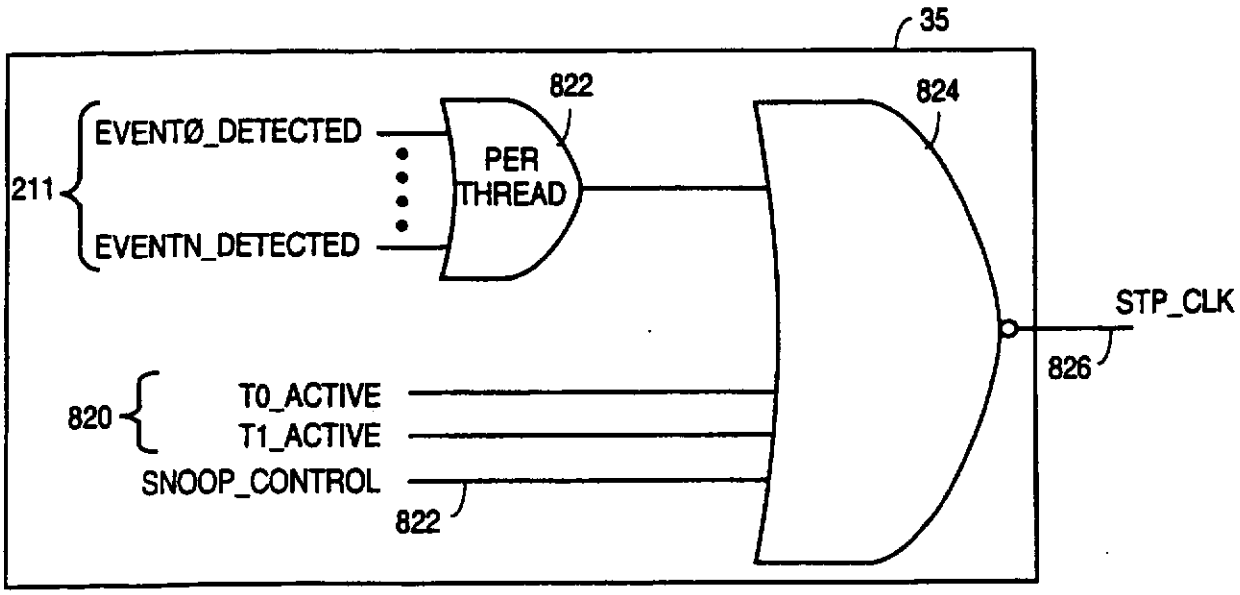


FIG. 19B