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(71) Applicant: **NEOLOGIC LTD.** [IL/IL]; 12 HaPekan Street,
4062955 Tel-Mond (IL).

(72) Inventors: **MESSICA, Avi**; 12 HaPekan Street, 4062955
Tel-Mond (IL). **LESHEM, Ziv**; 26 Ha-Mizmor Street,
3751056 Pardes Hana-Karkur (IL).

(74) Agent: **CHECHIK, Haim** et al.; LUZZATTO & LUZ-
ZATTO, P.O. BOX 5352, 8415202 Beer Sheva (IL).

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(54) Title: AN EFFICIENT BINARY MULTIPLIER WITH REDUCED AREA AND POWER CONSUMPTION

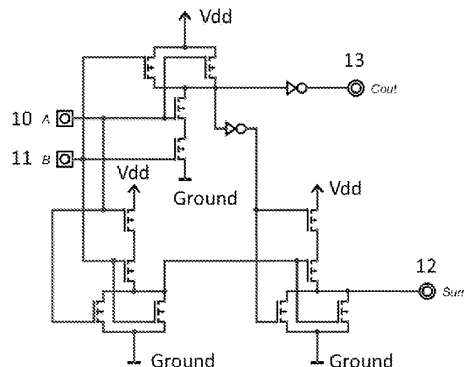


Fig. 3

(57) Abstract: A signed or unsigned multiplier for the multiplication of binary numbers, comprising a combination of logic cells consisting of standard cells or circuits in any multiplication architecture, which are modified, such that the modified logic cells partially replace CMOS circuits as mix-and-match implementation, or fully replace CMOS circuits as drop in implementation, in any architecture of the signed or unsigned multiplier.



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