

PATENT SPECIFICATION

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(54) A FIELD EFFECT MEMORY DEVICE

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention is directed to storage circuits which use transistors and more particularly to such storage circuits using storage type field effect transistors.

Semiconductor active devices, such as field effect transistors, are of great interest for use as memory elements. Circuits using such devices are fast, inexpensive, require little power, occupy a small amount of space, and may be integrated to form large arrays. However, in such circuits known up to this time, there is room for improvement in a number of areas. For example, conventional storage circuits commercially available and using semiconductor devices generally have a minimum of four or five semiconductor active elements (such as the above-mentioned transistors or the like) for each bit of information stored. If the number of semiconductor active devices per bit could be reduced, the number of storage cells in a given area of space would be increased correspondingly.

A number of proposals have been made to provide a storage circuit which uses only one transistor for each stored bit. Such proposed circuits usually include a transistor of the so-called storage type, a storage type transistor being defined as one where the main conduction path (which extends between two so-called main terminals) is settable to either of a minimum of two conductive states, and where the transistor thereafter maintains that state (in the absence of external influences) even though, for example, externally-supplied voltages may be removed from the electrodes of the transistor. One such storage type transistor is the so-called ferroelectric type, which includes a semiconductor body whose conduction path is altered by polarizing ferroelectric

material. The ferroelectric material is disposed in proximity to the transistor electrodes in order to alter the surface charged on a portion of that body which is adjacent the conductive path. However, in practice such ferroelectric transistors have proved extremely difficult to manufacture and have been unstable, and have not been proposed for use in storage circuits.

Storage circuits pertinent to the present invention are shown and described in our Belgian patent specification 722,411 which was granted October 16, 1968. Each storage circuit in the disclosure of this Belgian patent uses one storage transistor of the field effect type and further requires at least one additional, conventionally-operated field effect transistor which is used for selectively admitting operating voltage to the current path defined by the main electrodes of the storage transistor. The circuit shown in this Belgian specification further requires the use of an additional load impedance for the storage transistor, across which voltage is observed during a reading operation for the purpose of determining the state in which the storage transistor previously has been set. In addition to requiring the application of voltage at many levels, this particular storage circuit, when operated in its read mode develops an output signal which not only is a function of the state of the storage device, but also depends (inter alia) on the impedance of the above-mentioned additional conventional field effect transistor. As a consequence, output parameters of the circuit may vary from one storage circuit to the next.

It is an object of the present invention to provide a new and improved semiconductor active device storage circuit, which uses a single storage type field effect transistor to store one bit of binary information.

The present invention includes a storage type field effect transistor having a source electrode and a drain electrode (which are the above-mentioned "main electrodes") as well as a gate electrode. Such a transistor has a path which extends between the source and drain electrodes for controllably conducting current

from an external source of operating voltage. The transistor, which may be of the type shown and claimed in the aforementioned Belgian patent, exhibits bistable characteristics, i.e., (a) in response to the application between its gate and source electrodes of a first voltage greater than a first given value and a polarity which tends to increase conductivity in the source drain path, the transistor is set to a state in which it exhibits a first threshold value; while (b) in response to the application between its gate and source electrodes of a second voltage of greater than a second given value and of polarity which tends to decrease conductivity of the source drain path, the transistor is set to a state in which it exhibits a second threshold value different from the first value. In such a circuit the transistor is adapted to receive between its source and drain electrodes (for example, by way of an inactive device in the circuit which serves as a load impedance) operating voltage from an external source. The transistor also is adapted to receive between the source and gate electrodes: (a) during a writing operation a signal of amplitude selected to be equal to one of the first and second voltages, and (b) during a reading operation a signal of amplitude intermediate to the first and second given values.

The storage transistor is the sole active element in the circuit, and during a reading operation of the circuit the circuit output is determined solely by the impedance of the source drain path of the storage transistor.

A circuit using the present invention offers the advantage of requiring a minimum space for each circuit. Additionally, the performance of the circuit is improved because the dependence on the impedance of the single device allows output signal parameters to be controlled more easily. Further, the present invention allows the storage circuit to be served over a minimum number of lines (such as those extending to the source and drain electrodes) in the presence of control signals delivered (at a minimum number of voltage levels) over lines extending to the source electrode and gate electrodes of the single transistor.

In the detailed description of circuits embodying the present invention, reference is made to the drawings which are attached to and form a part of the present specification, and in which:

FIGURE 1 is a cross-sectional view of one embodiment of an N-channel depletion semiconductor device which may be used to practice the invention;

FIGURE 2 is a plot of capacitance versus applied voltage illustrating the bistable character of the device of FIGURE 1;

FIGURE 3 is a circuit diagram showing schematically an N-channel device used as a variable threshold detector;

FIGURES 4(a) and 4(b) are plots of the

V—I characteristics of the device of Fig. 3 when pulsed into the low and high threshold states;

FIGURE 5 is a schematic diagram showing the FIGURE 3 device used as a single element memory device; and

FIGURE 6 is a schematic diagram showing a series means to set and read-out the memory element of FIGURE 5.

FIGURE 1 shows a depletion type insulated-gate field-effect transistor 10 suitable for practicing the invention. The transistor 10 includes a body 12 of the semiconductive material of given conductivity type, such as p-type silicon, which has an upper surface 14. Adjacent to the surface 14 are spaced regions 15 and 16 of conductivity type opposite to that of body 12, which constitute source and drain regions, respectively, for the transistor 10. The distance between regions 15 and 16 defines the width of the conduction channel. Contacts 18 and 20 are formed on the surface 14 in ohmic contact with the regions 15 and 16.

Overlying the channel space between the regions 15 and 16 is a structure which comprises the gate and charge storing elements of the transistor 10. The first layer adjacent to the surface 14 in the space between the regions 15 and 16 is a thin layer 22 of insulating material, such as silicon dioxide.

Deposited on this layer 22 of silicon dioxide is a layer 24 of material which can accept charge carriers and confine them to localized sites adjacent the interface between the layers 22 and 24. In this example, the layer 24 is a layer of silicon nitride which is itself an insulator. On the silicon nitride layer 24 is a metallic electrode 26. Leads 28, 30 and 32, schematically shown, enable the application of external potentials to electrodes 18, 20 and 26. The conduction channel 34 existing for depletion type transistors with zero gate voltage applied, is shown by means of the dashed line 35 and is N-type produced from the P-type substrate by the oxidation step or otherwise.

The transistor 10 may be fabricated by known techniques. For example, the source and drain regions 15 and 16 may be formed by selectively masking the surface 14 and diffusing conductivity modifying substances through spaced portions of the surface 14 into the body 12. The silicon dioxide layer may be formed by thermally oxidizing the surface of the body 12 or by the pyrolytic decomposition of an organic siloxane compound such as tetraethoxysilane on the surface 14. The silicon nitride layer may be deposited by heating body 12 in an atmosphere of silane SiH_4 , and ammonia.

The insulating layer 24 is indicated as silicon nitride, but, equivalents having the same or similar properties may be substituted as circumstances may suggest or render expedi-

ent, without departing from the scope of the invention. Also, though transistor 10 is shown as a depletion type semiconductor, an enhancement device, whether of P-type or N-type silicon, having an insulator layer such as layer 24 is also suitable for practicing the invention.

The memory action of transistor 10 can be demonstrated by measuring the capacitance of the parallel plate system wherein the gate region 26 acts as one plate and the source 15 and drain 16 regions are connected to the semiconductor body 12 which acts as the other plate thereof and in which the insulating and charge storing layers act as the dielectric thereof. When the gate potential is varied, this capacitance changes in the manner illustrated in FIGURE 2, i.e., with a pronounced hysteresis loop. If the applied voltage is made sufficiently negative, the capacitance will switch to a higher value and will remain in that state after the removal of the negative voltage. If the potential applied to the gate is made sufficiently positive, the capacitance is switched to the lower value and will remain in that state after the removal of the positive voltage.

Referring to FIGURE 2, it should be noted that if the gate-to-source voltage is varied about the reference point (V_{REF}) by an amount whose amplitudes is less than plus or minus one half the amount ΔV , which may, for example, be 10 volts, the state of the transistor will be undisturbed indicating a mode of operation, which will be nondestructive of the information stored in the device.

The phenomenon just described is manifested by the device exhibiting a bivalued threshold voltage when operated as a transistor. In addition to the above described change in capacitance if the voltage applied to the gate is made sufficiently more positive than the voltage at the source electrode, the threshold voltage (V_T) will switch to a high value of threshold voltage (V_{TH}) and if the applied voltage is made sufficiently negative with respect to the source and drain electrodes, the threshold voltage is switched to a low value of threshold voltage (V_{TL}).

The circuit of FIGURE 3 is a logic gate whose threshold may be varied thereby controlling the passage of input signals. Transistor 50 is an N-channel device as indicated by the arrow on its source electrode. Its gate electrode is connected to terminal 52, its drain electrode is connected to terminal 54 and its source electrode is connected to reference terminal 56. A resistor 58 is connected between terminal 54 and junction point 60 and a source of potential 62 of magnitude V_{CC} is connected between junction point 60 and terminal 56. Terminal 54 serves as the voltage output of the circuit while the signal across resistor 58 is indicative of the current flowing in the circuit. Potential source 62 is shown as a

battery but it may instead be either pulsed, a half wave rectified, or a full rectified power source.

A source of positive potential 64 of magnitude V_1 may be connected by means of switch 66 to the gate 52 and a source of negative potential 68 of magnitude V_2 may be connected by means of switch 70 to gate electrode 52. The gate terminal 52 is also connected to one terminal of capacitor 72, the other terminal of the capacitor being connected to signal generator 74. Switch 76, connected across capacitor 72, may be used to shunt out the capacitor and to directly couple the signal generator 74 to the gate of transistor 50. Note that while for purposes of the present explanation, the switches are shown to be mechanical switches, in practice they may be electronic devices such as field-effect transistors or bipolar devices.

The amplitudes V_1 and V_2 of potential sources 64 and 68 are made sufficiently large to permit the threshold of transistor 50 to be set to either its low or high state. By way of example, for this particular case, V_1 and V_2 may each be chosen to be equal to 22.5 volts (plus in one case, minus in the other).

For depletion type transistor 50, the closure of switch 66 applies a positive 22.5 volts potential to the gate electrode setting its threshold voltage to V_{TH} , which is approximately equal to -4 volts, as indicated by the voltage-current ($V-I$) characteristics shown in FIGURE 4(a). Note that with a gate voltage (V_G) of zero volts, the drain current (I_D) for a drain-to-source voltage (V_{DS}) greater than 4 volts is approximately 5 milliamperes. Note also that the knee of the constant current curve for $V_G=0$ corresponds to a value of 4 volts along the X axis (said axis representing the value of drain-to-source (V_{DS}) voltage). Since the knee of the curve occurs at a point at which V_{DS} is equal to the difference between the gate and threshold voltage ($V_G - V_T$) and since V_G is equal to zero, then obviously V_T is equal to approximately -4 volts. When switch 66 is opened this value of V_{TH} exhibited by transistor 50 is maintained so long as any potential applied to the gate electrode does not reverse bias the gate-to-source region by an amount exceeding the reference value, which in the case given by way of example is approximately (-)3 volts about a negative bias of (-)7 volts.

Closing switch 70, while switch 66 is open applies a negative 22.5 volts potential to the gate of transistor 50. Applying this large reverse bias between the gate and the source and drain electrodes of the device sets the transistor into its low threshold state (V_{TL}), as indicated in FIGURE 4(b). FIGURE 4(b) is essentially the same as FIGURE 4(a) except that the threshold level has been decreased by approximately 6 volts. Note that in FIGURE 4(b) the curve traced for the condition when

V_G equals 0, indicates that a current of 10 milliamperes is obtained along the flat portion of the curve and with the knee of the curve corresponding to the drain-to-source potential of 10 volts. The potential at which the knee occurs, as explained before, indicates that the threshold voltage of transistor 50 is now -10 volts. Thus, by applying a negative potential between the gate and source electrode, the threshold voltage has been changed from -4 volts to -10 volts. This value of threshold will be maintained even though switch 70 is open and so long as any potential applied to the gate electrode does not forward bias the gate-to-source region by an amount exceeding the value of the indicated reference voltage, which in the case given, by way of example, is approximately (+) 3 volts about a negative bias of (-) 7 volts.

Thus, with transistor 50 in the V_{TL} state any signal above -10 volts will cause conduction and result in an output signal. However, with transistor 50 set to the V_{TH} state, transistor 50 will be cut off to all signals not exceeding -4 volts in amplitude. The threshold voltage is thus used to discriminate between signals of varying amplitudes. An important feature of the circuit of the present invention is that all potentials may be removed from the transistor and it will remain in the state in which it was last placed. This is of great value in memory arrays as loss of power or other computer system malfunction of similar nature does not destroy the stored information.

FIGURE 5 shows a flip-flop or memory circuit comprising a transistor 80 which, for this example, will be assumed to be an N-channel device of the enhancement type having a silicon nitride layer as described in FIGURE 1. The gate electrode of transistor 80 is shown connected to one side of two signal generators 82 and 84, whose internal impedances are sufficiently high to prevent one generator from shorting the other and, the other end of said signal generators is connected to a terminal 100 shown as reference or ground potential. A third signal generator 86 is shown connected between terminal 100 and the source electrode of transistor 80. The drain of transistor 80 is shown connected to a resistor 88 at a terminal 90, which also serves as the output terminal. The other end of resistor 88 is connected to the positive terminal of potential source 92 of amplitude V_{CC} , the negative terminal of potential source 92 being connected to terminal 100.

As shown in FIGURE 5, the amplitude of the signal from signal sources 84 and 86 is bivalued being either zero volts or 22.5 volts. With generators 86 and 82 at ground potential, a 22.5 volt pulse from generator 84 forward biases the gate-to-source region of transistor 80 setting the transistor to its high voltage V_{TH} state, which for example, may be equal to

+10 volts. A read pulse from generator 82 having a value greater than V_{TL} but less than V_{TH} applied to the gate of transistor 80 will not be sufficient to overcome the value of threshold voltage and no signal will be observed at terminal 90. Depending on the definition of the logic levels this condition may, for example, correspond to the set condition of a flip-flop or the storing of a logic "1" or a logic "0" in a memory cell since the output voltage is maintained at $+V_{CC}$ and there is no conduction of current in the drain source path of transistor 80.

With signal generators 82 and 84 now returned to ground potential, signal generator 86 may be triggered to provide a positive pulse of 22.5 volts amplitude to the source electrode. This pulse provides a reverse bias to the source-gate region, which is analogous to the condition described in FIGURE 3 when switch 70 was closed. This causes transistor 80 to be set in the low threshold condition which, for example, may be equal to +4 volts. Now a read signal from generator 82 having a value greater than V_{TL} but less than V_{TH} will cause current to flow between the drain and source of transistor 80 resulting in a voltage other than V_{CC} at terminal 90. In keeping with the definition of logic level stated above, this state of the transistor may correspond to the reset condition of a flip-flop since the transistor is returned to the low threshold voltage state. Note that, as shown in FIGURE 6, the parallel combination of generators 83 and 84 may be replaced by a dc source, whose maximum amplitude meets the requirements set for the maximum amplitude of pulse generator 82 placed in series with a pulse generator such as generator 84.

Although the device of FIGURE 1 and the circuits of FIGURES 3 and 5 employ N-type conductivity transistors, it should be appreciated that P-type devices may also be employed by adaptation of the FIGURE 3 circuit, by appropriate changes in the connections of the bias sources and the levels of the input signals.

WHAT WE CLAIM IS:—

1. A storage circuit comprising:
 - a field effect transistor having a source electrode, a gate electrode and a drain electrode, with a path extending between the source and drain electrodes;
 - where the transistor is of the storage type which: (a) responds to a first voltage applied between the gate and source electrodes where the first voltage is greater than a first given value and of polarity tending to make the source drain path more conductive by exhibiting a first threshold value, and (b) responds to a second voltage applied between the gate and source electrodes where the second voltage is greater than a second given value and of polarity tending to make the source drain



V_G equals 0, indicates that a current of 10 milliamperes is obtained along the flat portion of the curve and with the knee of the curve corresponding to the drain-to-source potential of 10 volts. The potential at which the knee occurs, as explained before, indicates that the threshold voltage of transistor 50 is now -10 volts. Thus, by applying a negative potential between the gate and source electrode, the threshold voltage has been changed from -4 volts to -10 volts. This value of threshold will be maintained even though switch 70 is open and so long as any potential applied to the gate electrode does not forward bias the gate-to-source region by an amount exceeding the value of the indicated reference voltage, which in the case given, by way of example, is approximately (+) 3 volts about a negative bias of (-) 7 volts.

Thus, with transistor 50 in the V_{TL} state any signal above -10 volts will cause conduction and result in an output signal. However, with transistor 50 set to the V_{TH} state, transistor 50 will be cut off to all signals not exceeding -4 volts in amplitude. The threshold voltage is thus used to discriminate between signals of varying amplitudes. An important feature of the circuit of the present invention is that all potentials may be removed from the transistor and it will remain in the state in which it was last placed. This is of great value in memory arrays as loss of power or other computer system malfunction of similar nature does not destroy the stored information.

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+10 volts. A read pulse from generator 82 having a value greater than V_{TL} but less than V_{TH} applied to the gate of transistor 80 will not be sufficient to overcome the value of threshold voltage and no signal will be observed at terminal 90. Depending on the definition of the logic levels this condition may, for example, correspond to the set condition of a flip-flop or the storing of a logic "1" or a logic "0" in a memory cell since the output voltage is maintained at $+V_{CC}$ and there is no conduction of current in the drain source path of transistor 80.

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WHAT WE CLAIM IS:—

1. A storage circuit comprising:
a field effect transistor having a source electrode, a gate electrode and a drain electrode, with a path extending between the source and drain electrodes;
where the transistor is of the storage type which: (a) responds to a first voltage applied between the gate and source electrodes where the first voltage is greater than a first given value and of polarity tending to make the source drain path more conductive by exhibiting a first threshold value, and (b) responds to a second voltage applied between the gate and source electrodes where the second voltage is greater than a second given value and of polarity tending to make the source drain



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path less conductive by exhibiting a second threshold value which is different from the first threshold value;

where the transistor is adapted to receive operating voltage between the source and drain electrodes;

and where the transistor is adapted to receive between the gate and source electrodes: (a) during a writing operation to signal of amplitude selected to be equal to one of the first and second voltages, and (b) during a reading operation a signal of amplitude intermediate the first and second threshold values; wherein:

the transistor is the sole active element in the storage circuit;

and during a reading operation the circuit output is determined solely by the impedance of the source drain path of the sole transistor.

2. A storage circuit of the type set forth in claim 1, further adapted in quiescent state to receive between the gate and source elec-

trodes of the transistor a voltage of value sufficient to bias the source drain path of the transistor into substantial non-conduction.

3. A storage circuit of the type set forth in either of claims 1 and 2, and which is adapted to receive during a reading operation a signal of magnitude sufficient to bias the source-drain path of the transistor into conduction when set to exhibit the second threshold value and into non-conduction when set to exhibit the first threshold value.

4. A storage circuit substantially as hereinbefore described in conjunction with Figure 3, Figure 5, or Figures 5 and 6 of the accompanying drawings.

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