

Description

The present invention relates generally to digital signal processing circuits, and particularly to a novel signal stretcher for a digital control signal.

In certain systems employing digital signal processing circuits, a need often arises for some form of control system, subject to actuation in an appropriate period of real time as determined by a sensing circuit, which recognizes the existence of a condition requiring control actuation via a monitoring of the digital signals being processed. Difficulties, associated, for example, with the monitoring functions, may, in some instances, suggest the wisdom of a widening of the control actuation period relative to the width of the period of condition recognition provided by the sensing circuit, thus calling for some form of control signal stretching.

The present invention is concerned with the provision of a structure which may serve such a digital control signal stretching function, dependent, however, upon the input signal meeting a minimum-duration criterion for predetermined input signal parameters.

Pursuant to the principles of the present invention, a duration-sensitive signal stretcher comprises: delay means having a plurality of successive signal takeoff points; an "AND" gate having a plurality of inputs equal in number to said takeoff points; a plurality of signal paths, each linking a respectively different one of said takeoff points to a respectively different one of said inputs; a plurality of delay devices; and a succession of two-input "OR" gates. In the signal stretcher, the input of the delay means is coupled to a source of clocked control information signals exhibiting one or the other of two alternative signal levels, and the amount of delay between successive ones of said takeoff points is the same. Each of said plurality of delay devices imparts the same predetermined amount of delay. One input of each of said succession of "OR" gates is rendered responsive to the output of said "AND" gate. The output of each of said succession of "OR" gates, with the exception of the last of said succession, is coupled via a respective one of said plurality of delay devices to the other input of the next succeeding one of said succession of "OR" gates, while the output of the last of said succession of "OR" gates is coupled to a control signal output. The sum of the delays imparted by said plurality of delay devices exceeds the amount of delay between the first and last of said successive signal takeoff points.

Pursuant to an illustrative embodiment of the present invention, wherein control signal information, of insufficient duration to meet a minimum-duration criterion for stretching, is nevertheless permitted to pass (in unstretched form) to the control

signal output terminal, the other input of the first of said succession of "OR" gates is rendered signal responsive by the inclusion of means (independent of said delay means and said "AND" gate) for coupling the output of the signal source thereto. A different mode of operation, however, is also feasible, wherein the minimum-duration criterion for stretching also constitutes the criterion for information passage to the control signal output terminal. Reference may be made to co-filed European Patent application EP-A-0199539 corresponding to the US Patent US-A-4,634,984 of L.A. Harwood, et al., entitled "Digital Signal Gate" for an example of a structure operating in the latter mode. Where such a mode of operation is intended, it is desirable that the other input of the first of the succession of "OR" gates is rendered non-responsive to the input signals, as shown in said copending Harwood, et al. application.

In the sole figure of the accompanying drawing, a duration-sensitive stretcher for digital control signals, pursuant to an embodiment of the present invention, is schematically illustrated.

In the system of the drawing, the output of a clocked control signal source 20 appears at terminal CI as a one-bit stream of control information, exhibiting either a quiescent "0" level or an active "1" level during each successive clocking interval. The signal at terminal CI is applied to the input of a series of five similar delay devices (L-1, L-2, L-3, L-4, L-5) connected in cascade. Illustratively, each of these delay devices comprises a data-type flip-flop imparting a signal-delay (τ) corresponding to a period at the signal clocking frequency (f_{CL}).

The cascade connection of the delay devices (L-1, L-2...L-5) forms a delay means which exhibits a delay of a τ amount between succeeding ones of a trio of signal takeoff points (located successively at the respective outputs of delay devices L-3, L-4 and L-5). An "AND" gate 30 is provided with three inputs, each linked by a signal path to a respectively different one of the aforementioned signal takeoff points.

The output of "AND" gate 30 is coupled to one input of each of a succession of nine two-input "OR" gates (O-1, O-2, O-3...O-9). The output of the last "OR" gate (O-9) of the succession is coupled to a control signal output terminal CO. The output of each of the remainder of this succession of "OR" gates is coupled to the other input of the next succeeding "OR" gate in the succession via a respectively different one of a plurality of similar delay devices (D-1, D-2, D-3...D-8). Illustratively, each of these delay devices also comprises a data-type flip-flop imparting a signal delay (τ) corresponding to a period at the signal clocking frequency (f_{CL}).

The illustrated structure is completed by a sig-

nal path providing a direct coupling of the signals at terminal CI to the said other input of the first (0-1) of said succession of "OR" gates.

It will be appreciated that, in the system of the drawing, the structure interposed between control signal source terminal CI and control signal output terminal CO serves a duration-sensitive signal stretching function, subjecting control information which satisfies a duration criterion to a stretching action, while passing in unstretched form control information which fails to satisfy such a criterion. In the specific arrangement shown, the duration criterion is such as to require exhibition of a "1" level at terminal CI for at least three successive clicking intervals in order for output control period stretching to occur.

To aid in an understanding of the operation of the illustrated signal stretching structure, several input signal examples will be considered below.

Example 1: Terminal CI departs from a quiescent "0" level for only two successive clocking intervals; i.e., the input signal duration of two successive clocking intervals is below the duration criterion (three successive clocking intervals) required for stretching action to occur. The pair of successive "1" outputs of source 20 are clocked along a first signal path comprising delay devices D-1, D-2, etc. in cascade, ultimately appearing at control signal output terminal CO as an output control pulse of an unstretched, (two-clocking-interval) duration. Throughout the period of control information passage to output terminal CO, "AND" gate 30 remains inactive, failing to output a "1" because of the lack of simultaneous appearances of "1" levels at all three of its inputs. While a "1" level appears at one or two of the "AND" gate inputs during certain clocking intervals, as the signals from terminal CI traverse a second signal path formed by devices L-1, L-2, etc. in cascade, the insufficient duration (two successive clocking intervals) of the input signal elevation of terminal CI to a "1" level assures that "AND" gate 30 will not be activated to output a "1" level.

Example 2: Terminal CI departs from a quiescent "0" level for three successive clocking intervals, i.e., the input signal duration equals the duration criterion (three successive clocking intervals) required for stretching action to occur. In this instance, as the signals from terminal CI traverse the aforementioned second signal path, a clocking interval is reached when all three inputs of "AND" gate 30 are simultaneously elevated to a "1" level, wherefore "AND" gate 30 outputs a "1". Because of this "AND" gate activity during such a clocking interval, a "1" level simultaneously appears at the control signal output terminal CO and at the inputs of all eight of the delay devices D-1, D-2...D-8. Accordingly, a "1" will be outputted at terminal CO

for the aforesaid clocking interval and for eight successive clocking intervals subsequent thereto. Thus, an input signal with a control period duration of three clocking intervals is converted to an output signal with a control period duration of nine clocking intervals.

Example 3: Terminal CI departs from a quiescent "0" level for five successive clocking intervals; i.e. the input signal duration exceeds the duration criterion (three successive clocking intervals) required for stretching action to occur. In this instance, a "1" level simultaneously appears at the control signal output terminal CO and at the inputs of all eight of the delay devices D-1, D-2...D-8 in three successive clocking intervals. As in Example 2 above, a stretching of a duration of six clocking intervals is a consequence, wherefore an output signal with a control period duration of eleven clocking intervals is the result.

The duration-sensitive stretching techniques of the present invention may, if desired, be associated with a duration-sensitive signal gate, as described in the aforementioned copending patent application of Harwood, et al. In the structure therein disclosed, input signals meeting the duration criterion appear in stretched form at the control signal output terminal; however, input signals which fail to satisfy the duration criterion are blocked from passage to the control signal output terminal (rather than passed thereto in unstretched form, as achieved in the herein described embodiment).

In the invention embodiment illustrated herein, testing of the input signal for the duration criterion is based on the monitoring of immediately successive samples of the input signal (at the "AND" gate inputs). The aforementioned copending Harwood, et al. patent application illustrates an alternative technique wherein testing for the duration criterion is based on the monitoring of alternate samples of the input signal (via use of delays of 2 τ between the successive signal takeoff points providing inputs for the "AND" gate).

It will be appreciated that the number of signal takeoff points, and the delays therebetween, are selectable parameters for tailoring the duration criterion to particular system requirements. It will also be recognized that the degree to which the sum of the delays provided by delay devices D-1, D-2, etc. exceeds the delay between the first and the last of the aforementioned signal takeoff points is a selectable parameter determinative of the magnitude of stretching action to be attained.

Claims

1. A duration sensitive signal stretcher, for use with a clocked source (20) of control information signals exhibiting one or the other of two



alternative signal levels characterized by:

delay means (L-1 L-5) having a plurality of successive signal takeoff points; the amount of delay (τ) between successive ones of said takeoff points being the same; the input (C1) of said delay means being responsive to the output (C1) of said signal source;

a plurality of signal paths, each connected to a respectively different one of said signal takeoff points;

an "AND" gate (30) having a plurality of inputs equal in number to said plurality of signal paths, each of said signal paths terminating at a respectively different one of said plurality of inputs of said "AND" gate;

a plurality of delay devices (D-1 to D-8), each imparting the same predetermined amount of delay (τ); and

a succession of two-input "OR" gates (0-1 to 0-9), with one input of each rendered responsive to the output of said "AND" gate; with the output of each of said succession of "OR" gates, with the exception of the last (0-9) of said succession, is coupled via a respective one of said plurality of delay devices to the other input of the next succeeding one of said succession of "OR" gates; and with the output of said last of said succession of "OR" gates coupled to a control signal output (CO);

wherein the sum of the delays imparted by said plurality of delay devices (D-1 to D-8) exceeds the amount of delay between the first and last of said successive signal takeoff points.

2. A duration-sensitive signal stretcher in accordance with claim 1 wherein said predetermined amount of delay imparted by each of said plurality of delay devices (D-1 to D-8) corresponds to a period at the clocking frequency for said signals.
3. A duration-sensitive signal stretcher in accordance with claim 1 or 2 wherein the amount of delay between successive ones of said signal takeoff points corresponds to a period at the clocking frequency for said signals.
4. A duration-sensitive signal stretcher in accordance with claim 1, 2 or 3, also including means, independent of said delay means (L-1 to L-5) and said "AND" gate (30), for coupling the output of said signal source (20) to the other input of the first (0-1) of said succession of two-input "OR" gates.
5. A duration-sensitive signal stretcher in accordance with claim 4 wherein delivery of signals

from said source (20) to the first of said plurality of successive signal takeoff points is delayed relative to delivery of signals from said source to said other input of the first (0-1) of said succession of two-input "OR" gates (0-1 to 0-9).

Revendications

1. Circuit d'allongement pour signaux sensibles à la durée devant être utilisé avec une source rythmée (20) de signaux d'information de commande montrant l'un ou l'autre de deux niveaux de signaux alternés, caractérisé par :

- des moyens de retard (L-1, L-5) comportant une pluralité de points de prélèvements successifs de signaux ; la valeur du retard (τ) entre les points de prélèvements successifs étant la même ; l'entrée (C1) desdits moyens de retard agissant en réponse à la sortie (C1) de ladite source de signaux ;
- une pluralité de trajectoires de signaux, chacune connectée à un point respectivement différent desdits points de prélèvements de signaux ;
- une porte ET (30) comportant une pluralité d'entrées dont le nombre est égal à celui de ladite pluralité de trajectoires de signaux, chacune desdites trajectoires de signaux se terminant sur une entrée respectivement différente de ladite pluralité d'entrées de la porte ET ;
- une pluralité de dispositifs de retard (D-1 à D-8), chacun impliquant la même valeur prédéterminée de retard (τ) et,
- une succession de portes OU, à deux entrées (0-1 à 0-9), avec une entrée de chaque porte agissant en réponse à la sortie de ladite porte ET ; avec la sortie de chaque porte de ladite succession de portes "OU", à l'exception de la dernière (0-9) de ladite succession, couplée, via un dispositif à retard respectif de ladite pluralité de dispositifs à retard, à l'autre entrée de l'une des portes OU suivantes de ladite succession de portes OU et, avec la sortie de ladite dernière porte "OU" de ladite succession de portes "OU" couplée à une sortie de signaux de commande (CO) ;

dans lequel la somme des retards impartis par ladite pluralité de dispositifs de retard (D-1 à D-8) dépasse la valeur du retard entre le premier et le dernier desdits points de prélèvement de signaux successifs.

2. Circuit d'allongement pour signaux sensibles à



la durée selon la revendication 1, dans lequel ladite valeur prédéterminée de retard imparti pour chacun desdits dispositifs de ladite pluralité de dispositifs de retard (D-1 à D-8) correspond à une période à la fréquence d'horloge pour lesdits signaux.

3. Circuit d'allongement pour signaux sensibles à la durée selon la revendication 1 ou 2 dans lequel la valeur du retard entre les points successifs de prélèvement desdits signaux correspond à une période à la fréquence d'horloge pour lesdits signaux.

4. Circuit d'allongement pour signaux sensibles à la durée selon les revendications 1, 2 ou 3 comportant également des moyens, indépendants desdits moyens de retard (L-1 à L-5) et de ladite porte ET (30), pour coupler la sortie de ladite source de signaux (20) à l'autre entrée de la première porte (0-1) de ladite succession des portes "OU" à deux entrées.

5. Circuit d'allongement pour signaux sensibles à la durée selon la revendication 4 dans lequel la délivrance des signaux à partir de ladite source (20) au premier point de ladite pluralité de points de prélèvements successifs de signaux est retardée par rapport à la délivrance des signaux de ladite source vers ladite autre entrée de la première porte OU (0-1) de ladite succession des portes OU (0-1 à 0-9) à deux entrées.

Patentansprüche

1. Zeitdauer-sensitive Dehnschaltung für Signale zum Einsatz mit einer getakteten Quelle (20) von Steuerinformationssignalen, die einen oder den anderen von zwei alternativen Signalpegeln aufweisen, gekennzeichnet durch,

Verzögerungsmittel (L-1 bis L-5) mit einer Mehrzahl aufeinanderfolgender Signal-Abnahmepunkte; wobei die Dauer der Verzögerung (τ) zwischen aufeinanderfolgenden der Abnahmepunkte gleich ist; wobei der Eingang (C1) der Verzögerungsmittel auf das Ausgangssignal (C1) der Signalquelle anspricht;

eine Mehrzahl von Signalwegen, die jeweils mit einem jeweils anderen der Signal-Abnahmepunkte verbunden ist;

ein UND-Gatter (30) mit einer Mehrzahl von Eingängen gleicher Anzahl, wie der Anzahl von Signalwegen, wobei jeder der Signalwege an jeweils einen anderen der Mehrzahl von Eingängen des UND-Gatters endet;

eine Mehrzahl von Verzögerungsgliedern (D-1 bis D-8), die jeweils die gleiche, vorbe-

stimmte Verzögerungsdauer (τ) bewirken; und eine Folge von zwei Eingänge aufweisenden ODER-Gattern (0-1 bis 0-9), wobei jeweils ein Eingang derart geschaltet ist, daß er auf den Ausgang des UND-Gatters reagiert; wobei der Ausgang von jedem der Folge von ODER-Gattern mit Ausnahme des Letzten (0-9) der Folge über jeweils eins der Mehrzahl von Verzögerungsgliedern an den anderen Eingang des nachfolgenden der Folge von ODER-Gattern angeschlossen ist; und wobei der Ausgang des Letzten der Folge von ODER-Gattern an einem Steuersignalausgang (co) angeschlossen ist;

bei der die Summe der durch die Mehrzahl der Verzögerungsglieder (D-1 bis D-8) bewirkten Verzögerungen die Verzögerungsdauer zwischen dem Ersten und Letzten der aufeinanderfolgenden Signal-Abnahmepunkte übersteigt.

2. Zeitdauer-sensitive Dehnschaltung für Signale nach Anspruch 1, bei der die von jedem der Mehrzahl von Verzögerungsgliedern (D-1 bis D-8) bewirkte vorgegebene Verzögerungsdauer einer Periode der Taktfrequenz der Signale entspricht.

3. Zeitdauer-sensitive Dehnschaltung für Signale nach Anspruch 1 oder 2, bei der die Verzögerungsdauer zwischen aufeinanderfolgenden Signal-Abnahmepunkten einer Periode der Taktfrequenz der Signale entspricht.

4. Zeitdauer-sensitive Dehnschaltung für Signale nach Anspruch 1, 2 oder 3, die unabhängig von den Verzögerungsmitteln (L-1 bis L-5) und UND-Gatter (30) auch Mittel zum Verbinden des Ausganges der Signalquelle (20) mit dem anderen Eingang des Ersten (0-1) der Folge von zwei Eingänge aufweisenden ODER-Gattern enthält.

5. Zeitdauer-sensitive Dehnschaltung für Signale nach Anspruch 4, bei der die Signalabgabe von der Quelle (20) an den Ersten von der Mehrzahl von aufeinanderfolgenden Signal-Abnahmepunkten zur Signalabgabe der Quelle an den anderen Eingang des Ersten (0-1) der Folge von zwei Eingänge aufweisenden ODER-Gattern (0-1 bis 0-9) relativ verzögert wird.

