

ABSTRACT

A memory device includes a peripheral circuit region including a first substrate and circuit elements on the first substrate, the circuit elements including a row decoder; a cell array region including wordlines, stacked on a second substrate on the peripheral circuit region, and channel structures extending in a direction perpendicular to an upper surface of the second substrate and penetrating through the wordlines; and a cell contact region including cell contacts connected to the wordlines and on both sides of the cell array region in a first direction parallel to the upper surface of the second substrate, the cell contacts including a first cell contact region and a second cell contact region, the first and second cell contact regions having different lengths to each other in the first direction. Each of the first and second cell contact regions includes first pads having different lengths to each other in the first direction and second pads different from the first pads, and the cell contacts are connected to the wordlines in the first pads. The number of the second pads included in the first cell contact region is greater than the number of the second pads included in the second cell contact region.

FIG. 6A