"METHOD OF MANUFACTURING AN AMORPHOUS-SILICON THIN-FILM TRANSISTOR"

This invention concerns a method of manufacturing an amorphous-silicon thin-film transistor.

According to the present invention, there is provided a method of manufacturing an amorphous-silicon thin-film transistor comprising forming a gate electrode on an insulating substrate; forming a gate insulating layer on the gate electrode and on the insulating substrate; forming an amorphous-silicon layer on the gate insulating layer; forming a protective insulating layer on the amorphous-silicon layer; imparting a pattern, corresponding to that of the gate electrode, to the protective insulating layer so as to expose a corresponding portion of the amorphous-silicon layer; forming on the protective insulating layer, and on the said corresponding portion of the amorphous-silicon layer, an impurities-containing silicon layer containing impurities serving as a donor or as an acceptor; and forming a source electrode and a drain electrode which partly overlap the protective insulating layer, the impurities-containing silicon layer and the amorphous-silicon layer being selectively removed using the source and the drain electrode as a mask.

Preferably, the said pattern is imparted to the protective insulating layer by applying photo-resist thereto; developing the photo-resist by irradiating the surface of the insulating substrate opposite to that provided with the gate electrode so as to impart the said pattern to the photo-resist; and employing the developed photo-resist as a mask while etching the protective insulating layer.

In one form of the present invention, a metal layer is formed directly on the impurities-containing silicon layer; a pattern corresponding to the source electrode and the drain electrode is imparted to the metal layer; the impurities-containing silicon layer and the amorphous-silicon layer are selectively removed using the patterned metal layer as a mask; a transparent conductive layer is formed directly on the metal layer; and the transparent conductive layer is selectively removed to form source wiring connected to the source electrode and a pixel electrode connected to the drain electrode.

Preferably, the thicknesses of the gate insulating layer, the amorphous-silicon layer and the protective insulating layer are substantially 300 nanometers, 50 nanometers and 300 nanometers respectively.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a set of sectional views illustrating how an amorphous-silicon thin-film transistor for an active matrix type liquid crystal display is formed in accordance with an embodiment of the present invention;

Figure 2 is an electrical circuit diagram showing the construction of an active matrix type liquid crystal display;

Figure 3 is a set of sectional views illustrating how an amorphous-silicon thin-film transistor for an active matrix type liquid crystal display is formed in accordance with a known method; and

Figure 4 is an electrical circuit diagram showing a pixel portion of an active matrix type liquid crystal display.

A thin liquid crystal matrix image display is known in which an MIS-type thin-film transistor using

amorphous-silicon is provided for each pixel as a switching element. Such a display is known as an active matrix type liquid crystal display.

Figure 2 shows an example of the construction of the above-described active matrix type liquid crystal display. When, for example, a scanning line Y1 is selected from among a group of scanning lines 9, the gates of corresponding thin-film transistors 11 connected thereto are simultaneously turned on, and, through the sources of these thin-film transistors which have been thus turned on, a signal voltage corresponding to certain image information is transmitted from each of a group of signal lines 10 to the drain of each transistor. Connected to each drain is a pixel electrode (not shown), images being displayed by varying the light transmittance of a liquid crystal layer 12 by reason of the voltage difference between this pixel electrode and an opposed electrode 13 formed on a substrate on the opposite side with respect to the liquid crystal layer 12. After the above-mentioned gates are turned off, the voltage difference between the above-mentioned pixel electrode and the opposed electrode 13 is retained until the scanning line Y1 is selected next time, so that the liquid crystal corresponding to each pixel is static-driven, thus achieving a high-contrast image display.

Japanese Laid-Open Patent Specification No. 58-212177 discloses a method of manufacturing thin-film transistors in which a gate insulating layer, an amorphous silicon layer and a protective insulating layer are successively formed in order to secure reliability and reproducibility of the manufacturing process, etc.

Figure 3 illustrates the above-mentioned known

manufacturing process. First, a gate electrode 15 is formed on an insulating substrate 14 of glass or the like. Then, a gate insulating layer 16, an amorphous-silicon layer 17, and a protective insulating layer 18 are successively formed, as shown at (a). Subsequently, ultraviolet rays are applied from above, with photo-resist in a predetermined configuration on the protective insulating layer 18 being used as a mask, thereby producing openings in the protective insulating layer 18 so as to expose the amorphous-silicon layer 17 in such a manner that the protective insulating layer 18 partly overlaps the gate 15 as shown at (b). An impurities-containing silicon layer 19 which contains impurities serving as the donor or the acceptor is then formed. The impurities-containing silicon layer 19, the protective insulating layer 18, and the amorphous-silicon layer 17 are selectively removed, thereby forming an island structure including said openings, as shown at (c). Subsequently, a transparent conductive layer 20 is formed, and is selectively removed, thereby forming a source electrode drain pattern, a source wiring pattern, and a pixel electrode pattern. The impurities-containing silicon layer 19 is then selectively removed using the patterns of the transparent conductive layer 20 as a mask, as shown at (d).

If the minimum circuit wiring distance is L, it may be desirable to arrange that an overlapping area with a width 2L is formed both in the section between the gate and the drain and in that between the gate and the source. As a result, overlapping capacitance is generated in these areas, which involves the following problems in the case of the method illustrated in Figure 3.

Figure 4 shows the construction of one pixel portion of an active matrix type liquid crystal display using the thin-film transistor shown in Figure 3, focusing in particular on the overlap capacitance in the thin-film transistor. The reference numeral 21 denotes a thin-film transistor; 22 denotes a pixel capacitance formed between a pixel electrode (not shown) and an opposed electrode (not shown) with liquid crystal material (not shown) between them; 23 denotes the overlap capacitance between the gate and the drain of the transistor 21; and 24 denotes the overlap capacitance between the gate and the source.

First, the influence of the overlap capacitance 23 will be explained. A signal voltage corresponding to the pixel signal is charged on the pixel capacitance 22 while the thin-film transistor 21 is ON. When a predetermined ON-period has elapsed, the thin-film transistor 21 is turned OFF. In other words, the gate voltage of the thin-film transistor 21 is changed from "1" to "0". If at this time the overlap capacitance 23 did not exist, the voltage of the above-mentioned pixel electrode would remain the same. As it is, the voltage of the above-mentioned pixel electrode becomes lower than the normal value when the above-mentioned gate is turned off by the coupling effect. This leads to deterioration in the black or white level of the image display, i.e. degradation of the contrast ratio, thus affecting the image display quality.

Next, the influence of the overlap capacitance 24 will be explained. It is necessary for the pixel data to charge the above-mentioned pixel electrodes through the signal lines 10 while the above-mentioned gates are ON. When seen from the signal source, however, the overlap capacitance 24 relating to the thin-film

transistors 21 connected to one signal line 10 is increased, so that, when the capacitance value is large, it is difficult to charge the above-mentioned pixel electrodes up to the predetermined voltage. When, in particular, the number of pixels is augmented and the number of scanning lines 9 increased, the overlap capacitance 24 will increase and the ON period of the above-mentioned gates will decrease, thereby aggravating the above-described undesirable condition. Thus, when the said gates are turned OFF before the said pixel electrodes are sufficiently charged, i.e. before the voltage value of the said pixel electrodes has reached the normal value, the black or white level of the image display is deteriorated, i.e. the contrast ratio is degraded, as in the above case, thus affecting the image display quality.

As described above, the greater the capacitance value of the overlap capacitances 23, 24, the greater is the deterioration of the image display quality.

It is accordingly an object of the present invention to provide a method of manufacturing an amorphous-silicon thin-film transistor which makes it possible to decrease the overlap capacitance between the gate and the drain and that between the gate and the source and to obtain a high-quality image with a high contrast ratio.

An embodiment of the present invention will now be described with reference to Figure 1.

First a gate electrode 2 of a metal such as Cr is formed on an insulating substrate 1 made of glass or the like. Then, a gate insulating layer 3 of silicon nitride or silicon oxide is formed on the gate electrode 2 and on the insulating substrate 1. Thereafter, an amorphous-silicon layer 4, and a protective insulating

layer 5 of silicon nitride or silicon oxide are successively formed one on top of the other by, for example, the plasma CVD (chemical vapour deposition) method, as shown at (a). Subsequently, a positive-type photo-resist (not shown) is applied to the protective insulating layer 5, and, after pre-baking, the back surface of the insulating substrate 1 is irradiated with ultraviolet rays. Since the above-mentioned ultraviolet rays are not transmitted through the gate electrode 2, development of the said photo-resist results in the photo-resist remaining on the protective insulating layer 5 in a configuration conforming to the gate electrode 2. Etching of the protective insulating layer 5 is conducted using a buffer hydrofluoric acid solution, the photo-resist thus remaining serving as the mask. This results in a configuration conforming to the gate electrode 2 being imparted to the protective insulating layer 5, as shown in Figure 1(b), while exposing the corresponding portion of the amorphous-silicon layer 4. Since the amorphous-silicon layer 4 absorbs the said ultraviolet rays applied to the back surface of the insulating substrate 1, the irradiation ratio of the said ultraviolet rays to the said photo-resist is decreased. When, however, the film thickness of the amorphous-silicon layer 4 is 30 nanometers or so, several to several tens of percent of the said ultraviolet rays are transmitted, so that an excessive deterioration in the irradiation efficiency of the said ultraviolet rays applied to the above photoresist does not occur. On the contrary, it is advantageous in many ways. For example, it is not necessary to use a mask aligner or the like since the patterning is effected in a suitable manner. Further, a number of substrates can be exposed simultaneously.

After forming the protective insulating layer 5 in a pattern conforming to that of the gate electrode 2, an impurities-containing silicon layer 6 and a metal layer 8 are successively formed one on top of the other. A pattern corresponding to the source electrode and the drain electrode which partly overlap the protective insulating layer 5 is imparted to the metal layer 8, and the impurities-containing silicon layer 6 and the amorphous-silicon layer 4 are selectively removed using the patterned metal layer 8 as a mask, thereby forming an island structure, as shown at (c). Subsequently, a transparent conductive layer 7 is formed directly on the metal layer 8, and is selectively removed, thereby forming a source wiring connected to the source electrode and a pixel electrode connected to the drain electrode as shown at (d).

The manufacturing method illustrated in Figure 1 makes it possible to manufacture an amorphous-silicon transistor which has an overlapping width L (as opposed to the 2L of Figure 3) between the gate and the drain and between the gate and the source.

As described above, the overlapping area between the gate and the drain and that between the gate and the source in these embodiments has the minimum width L. In addition, the protective insulating layer 5 extends over the entire overlapping areas, in contrast to the arrangement shown in Figure 3, so that it is possible to reduce the overlap capacitance by half as compared with the prior art.

Further, by arranging that the thicknesses of the gate insulating layer 3, the amorphous-silicon layer 4, and the protective insulating layer 5 are substantially 300 nanometers, 50 nanometers, and 300 nanometers respectively, for example, the overlap capacitance can

be reduced to one third of that in the prior art.

In the embodiment of Figure 1, the protective insulating layer 5 is formed in such a manner that it conforms to the gate electrode 2 so that the width of the overlapping areas L between the gate and the drain and between the gate and the source can be smaller than in the prior art, the overlap capacitance thereof being reduced by half or more. Consequently, the method makes it possible to manufacture an amorphous-silicon transistor by means of which a high-quality image with a high contrast ratio can be obtained.

Further, the method illustrated in Figure 1 does not need alignment using a mask when patterning the protective insulating layer 5, so that inadequacies due to alignment are decreased, which results in a substantial improvement in the yield.

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CLAIMS

1. A method of manufacturing an amorphous-silicon thin-film transistor comprising forming a gate electrode on an insulating substrate; forming a gate insulating layer on the gate electrode and on the insulating substrate; forming an amorphous-silicon layer on the gate insulating layer; forming a protective insulating layer on the amorphous-silicon layer; imparting a pattern, corresponding to that of the gate electrode, to the protective insulating layer so as to expose a corresponding portion of the amorphous-silicon layer; forming on the protective insulating layer, and on the said corresponding portion of the amorphous-silicon layer, an impurities-containing silicon layer containing impurities serving as a donor or as an acceptor; and forming a source electrode and a drain electrode which partly overlap the protective insulating layer, the impurities-containing silicon layer and the amorphous-silicon layer being selectively removed using the source and the drain electrode as a mask.

2. A method as claimed in claim 1 in which the said pattern is imparted to the protective insulating layer by applying photo-resist thereto; developing the photo-resist by irradiating the surface of the insulating substrate opposite to that provided with the gate electrode so as to impart the said pattern to the photo-resist; and employing the developed photo-resist as a mask while etching the protective insulating layer.

3. A method as claimed in claim 1 or 2 in which a metal layer is formed directly on the impurities-containing silicon layer; a pattern corresponding to the source electrode and the drain electrode is imparted to the metal layer; the impurities-containing silicon layer and the amorphous-silicon layer are selectively removed using the patterned metal layer as a mask; a transparent conductive layer is formed directly on the metal layer; and the transparent conductive layer is selectively removed to form source wiring connected to the source electrode and a pixel electrode connected to the drain electrode.

4. A method as claimed in any preceding claim in which the thicknesses of the gate insulating layer, the amorphous-silicon layer and the protective insulating layer are substantially 300 nanometers, 50 nanometers and 300 nanometers respectively.

5. A method of manufacturing an amorphous-silicon thin-film transistor substantially as hereinbefore described with reference to Figure 1 of the accompanying drawings.

6. An amorphous-silicon thin film transistor substantially as hereinbefore described with reference to and as shown in Figure 1(d) of the accompanying drawings.