

The invention relates to a FM detector for demodulating signals, in particular audio signals, according to the preamble of claim 1. A FM detector of this kind is known from IEEE Transactions on Consumer Electronics, Vol. 34, No. 3 August 1988, IEEE; New York, US; Y. Yamamoto et al.: "A New Audio Processor for EIAJ MTS", pp. 625-633

These FM detectors are preferably used for applications in which frequency-modulated signals have to be converted into low-frequency audio signals. This is particularly the case in television or radio receivers.

As in the case of many other circuit parts in a television or radio receiver, it is desirable to dispose FM detectors in a space-saving manner. Although known FM detectors are already partly integrated in a module, they have to be provided with external components such as, for example, ceramic filters or LC circuits in order to have a good signal-to-noise ratio or prevent thermal drift of the charge carrier. In addition, expensive adjustment and tuning of the FM detectors and external components is frequently necessary.

The object of the invention is to develop an integrated FM detector of the described type such that it can be easily controlled and the expenditure on external components for adjusting the internal operating conditions and on the manual adjustment of the external components is reduced.

This object is solved according to the invention in that the external components are represented by an internal regulating or control circuit which is disposed in the module. Advantageous developments of the invention are described in the subclaims and the following description.

An embodiment of the invention is explained in detail in the following with reference to the drawings, in which:

Figure 1 is a basic circuit diagram of a FM detector

according to the invention,  
 Figure 2 is a schematic oscillator circuit diagram with  
 associated timing diagrams,  
 Figure 3 is a circuit diagram of a fully integrated FM  
 detector,  
 Figure 4 is a precise circuit diagram of a FM detector  
 according to Figure 3,  
 Figure 5 is an adjustment network with FM detectors  
 according to the preceding figures.

Figure 1 shows a basic circuit design of a FM detector (= FM  
 demodulator). The circuit essentially consists of a phase-  
 locked loop with a current-controlled oscillator 1 and a  
 four-quadrant/analogue multiplier 2 as phase detector. The  
 oscillator 1 consists of a current-controlled charging  
 capacitor 3 and a Schmitt trigger 4. The free-running  
 frequency of the oscillator is  $f_0 = (2 \Delta V C_2 / I_m)^{-1}$ .  
 $\Delta V$  is the voltage difference between the voltage  $V_u$  and  $V_o$  of  
 the charging capacitor,  $C_2$  the capacitance of the charging  
 capacitor 3.  $V_u$  and  $V_o$  are the switching potentials of the  
 Schmitt trigger.  $V_u$  is the low potential,  $V_o$  the high  
 potential. The operating mode of the Schmitt trigger is  
 known (see Tietze/Schenk "Halbleiter-Schaltungstechnik", pages  
 182 and 222 ff). In the steady state the charging capacitor  
 is charged by the mean direct current  $I_m$ . According to the  
 state of the Schmitt trigger and thus the oscillator voltage  
 $V_{osz}$ , the switch 5 is set either to 0 or to  $-2I_m$  and  $I_m$  is  
 superimposed on the current in question ( $-2I_m$  or 0). The  
 resulting current  $I_e$  ( $=I_m$  or  $-I_m$ ) thus charges or discharges  
 the charging capacitor. The switch 6 is at 0 after the  
 oscillator frequency has locked onto the input frequency  
 (i.e. in the steady state). Otherwise, the switch 6 is  
 switched to  $I_d$  or  $-I_d$  in order to lock the oscillator  
 frequency onto the input frequency. In this case the current  
 $I_d$  or  $-I_d$  serves as a d.c. compensating current and also has  
 $I_m$  or  $I_m$  superimposed on it. The charging capacitor and thus  
 the oscillator can therefore lock onto the input frequency  
 $f_{in}$  of the input signal in the range  $f_0 - \Delta f$  to  $f_0 + \Delta f$ .  
 $\Delta f/f_0 = I_d/I_m$  serves as output signal here. A phase shift of

90° occurs at the output of the Schmitt trigger and thus at the output of the oscillator for an unmodulated input frequency  $f_{in} = f_0$ . An additional phase shift of  $\Delta\varphi$  proportional to  $f_{in} - f_0$  occurs in the case of a frequency-modulated input signal. The phase detector 2 now mixes the oscillator signal from the output of the Schmitt trigger having the oscillator voltage  $V_{osz}$  (and the oscillator frequency  $f_{osz}$ ) with the input signal having the input voltage  $V_{in}$  (and the input frequency  $f_{in}$ ) and provides a pulse-width modulated signal at the output of the phase detector. This pulse-width modulated signal may, for example, be converted by a low-pass filter (not shown) which is connected downstream into a low-frequency audio signal.

Figure 2 shows a schematic oscillator circuit diagram with the associated timing diagram. The transistors  $Q_6 - Q_8$  form a Schmitt trigger which controls a differential amplifier designed as a switch. A delta voltage is thus produced, as shown in the timing diagram of Figure 2.

Particular attention is paid to the noise performance in this oscillator. The bandwidth of the Schmitt trigger must be limited in order to achieve a good noise performance. A filter capacitor  $C_{filt}$  is provided for this purpose. The time constant is as high as possible, but low enough to prevent a high frequency deviation ( $T = 0,13 \times T_{periode}$ ). The noise performance of the FM detector is inadequate without this filtering.

As already shown in Figure 1, the oscillator 1 is the nucleus of the FM detector. The control current  $I_0$  (in Figure 3) is modulated by the input signal. If its frequency is close to the free-running frequency of the oscillator  $f_z$ , it is synchronised and exhibits the time response as shown in the timing diagram in Figure 3. If the incoming input signal has the same frequency as the free-running frequency of the oscillator, there is a phase rotation of 90°. A deviation from the free-running frequency results in a linear phase deviation (see Figure 3). Simulation and

measurement of a production module demonstrated a good performance (signal-to-noise ratio 70 dB, distortion less than 2%, side bands 40 dB down).

On account of component tolerances and manufacturing variations, analogue circuits contained in integrated circuits, e.g. filters, but also FM detectors, must be adjusted in order to produce "one chip" receivers. An adjustment network as shown in Figure 5 is provided for this purpose. This shows a horizontal frequency oscillator 60. This is the reference circuit part.

Its frequency can easily be measured and adjusted by means of the 5-bit D/A converter 601 with an error of less than  $\pm 1\%$ . The D/A converter 601 is software adjustable at the television set production stage, the adjustment then being stored.

The memory contents may be modified in an undesirable manner due to high voltage surges in the vicinity of this D/A converter. Should this cause too great a drop in the horizontal frequency, the horizontal final stage and a switch mode supply unit could be destroyed. A parity check is for this reason carried out in the D/A converter 601. If this check establishes an error, a maximum control current is set by the switch 602. This results in an increase in the horizontal frequency and prevents circuits from being destroyed.

When the horizontal frequency oscillator 60 is adjusted the control current  $I_c$  results from the reference current  $I_{ref} = V_{ref} / R_{ext}$ . On account of manufacturing tolerances, the capacitors, for example, in the integrated circuit have an actual value  $C_{actual}$  compared with a nominal value  $C_{nominal}$ . The control current  $I_c$  is thus capacitor-adjusted and has, for example, the value  $I_c = I_{ref} + C_{actual} / C_{nominal}$ .  $C_{actual}$  is in practice measured indirectly via the frequency measurement of the horizontal frequency oscillator 60.

Although the output frequency of the horizontal frequency oscillator is basically dependent upon the control current  $I_c$ , it is also, for example, slightly dependent upon the voltage equivalent of thermal energy  $V_t$  and the peak-to-peak output voltage  $V_{pp}$ . This results in this frequency being approximately  $I_c / C_{actual} * (1 + 9 + V_t / V_{pp})$  and consequently the necessity of also subjecting certain analogue circuit parts which are adjusted by the control current  $I_c$  to a fine adjustment.

The integrated circuit therefore comprises five loops for different circuit parts in which the control current  $I_c$  is summed with a correction current ( $I_{con}$ ) at the summing points 616, 626, 636, 646 and 676.

The analogue filters 621 - 623 and the FM demodulator 624 prepare a first sound channel, the analogue filters 631 - 633 and the FM demodulator 634 a second sound channel. The criterion for the fine adjustment of the two sound channels is the d.c. voltage offset at the outputs of the FM demodulators 624 and 634. The output voltages are filtered in the low-pass filters 625 and 635 with a cut-off frequency of 10 Hz. The resulting d.c. voltage components in each case produce the correction current  $I_{con}$ .

The fine adjustment of the sound traps 611 - 612 and the equalizer 613 in the image I.F. and of the preselection filter 614 in the sound I.F. is carried out with the aid of an additional reference biquad filter 617, which is disposed in the feedback path of a phase-locked loop. The phase-locked loop comprises a reference oscillator 615 and a programmable 1 : n-divider 618. The cut-off frequency of the reference biquad filter 617 is appropriate for the frequencies of the sound traps 611 - 612, the equalizer 613 and the preselection filter 614, so as to produce a satisfactory synchronous operation.

Because gm amplifiers type 1 are used for the sound traps 611 - 612, the equalizer 613 and the preselection filter 614

on account of the high frequencies to be handled, the control current  $I_c$  is also subjected to a temperature-dependent correction in the circuit 619.

Only an error of a maximum of  $\pm 0.4\%$  may occur when subjecting the chroma bell filter 64 to a fine adjustment. Moreover, the quality factor of the chroma bell filter must reach the value of sixteen. A different fine adjustment method is therefore used. This filter is switched over to an adjustment mode during the vertical line flyback (frame). A crystal oscillator 641 with the PAL chrominance subcarrier frequency 4.43 MHz is connected to the filter and the phase at the input and output of the filter compared in a phase comparator 642. If the phase difference is zero, the mid-band frequency of the chroma bell filter 64 corresponds with the PAL chrominance subcarrier frequency. The phase comparator 642 is connected to a sampling and holding circuit 643. Because minimal leakage currents are necessary, the sampling and holding circuit 643 has operational amplifiers with NMOS inputs (not shown). This circuit is connected to an integrator 644, which produces the correction current for the control current  $I_c$ . A small correction factor of approximately 2.3% is additionally introduced during the measuring period by the correction circuit 645, as the nominal mid-band frequency (4.328 MHz) of the chroma bell filter 64 diverges slightly from the PAL chrominance subcarrier frequency (4.43 MHz).

The adjustment of the chrominance subcarrier trap 65 is less critical. The control current which is used for the chroma bell filter is also used here.

The control current correction value for a vertical sync separator 671, a  $\phi_{i2}$  loop circuit 672 and a pulse-width modulator 673 for a switch mode supply unit is obtained via a further phase-locked loop with a reference integrator 674.

The described adjustment process with the automatic fine adjustment is suitable for integrated circuits in bipolar

and BICMOS technology.

The advantage of also being able to eliminate the dependency of the circuit parts on temperature is a result of the additional fine adjustment.

Figure 4 is a precise circuit diagram of a FM detector, the mid-band frequency of which is tuned to 500 kHz. The phase detector 2 is formed from the transistors  $Q_3$ ,  $Q_5$ ,  $Q_6$ ,  $Q_8$ ,  $Q_9$  and  $Q_{10}$ . The Schmitt trigger is formed from the transistors  $Q_{15}$ ,  $Q_{16}$  and  $Q_{18}$ , the resistors  $R_{12}$ ,  $R_{13}$ ,  $R_{15}$  and the capacitors  $C_4$  and  $C_3$ . The current  $I_m$  is supplied by the transistor  $Q_{22}$ , while the current  $-2I_m$  is supplied by the transistor  $Q_{30}$  or  $Q_{21}$ . The current  $I_d$  is supplied by the transistor  $Q_{28}$ .



1. FM detector for demodulating signals, in particular audio signals, the FM detector being integrated in a module and its operation being adjustable via internal regulating or control circuits disposed in the module, the FM detector being formed in a television or radio receiver and consisting of a phase detector (2), which mixes an input signal with an oscillator signal, the oscillator signal being produced by an oscillator (1), which can be controlled by the input signal of the FM detector, by the output signal of the oscillator itself and by a reference quantity, which can be adjusted so as to be constant, and the oscillator (1) consisting of a charging capacitor (3) and a Schmitt trigger (4), characterised in that the charging capacitor (3) can be controlled by the input signal and by a charging current  $I_e$ , that the output signal ( $V_{OS2}$ ) of the oscillator (1) controls a switch (5), which superimposes either a current  $-2I_m$  or zero  $\times I_m$  on the charging current  $I_e$ ,  $I_m$  being the mean direct current with which the charging capacitor is charged in the steady state, that a finer control of the charging current is effected by means of an additional switch (6) in accordance with the input signal, this additional current being zero when the oscillator frequency locks onto the input frequency, and the total charging current constitutes the sum of these two component currents.

2. FM detector according to claim 1, characterised in that the FM detector is designed for a mid-band frequency of approximately 500 kHz or approximately 260 kHz.

3. FM detector according to claim 1, characterised in that a phase shift of  $90^\circ$  takes place at the output of the Schmitt trigger (4) when the oscillator frequency locks onto the input frequency.

4. FM detector according to claim 3, characterised in that the output signals of the phase detector are pulse-width modulated.



5. FM detector according to any one of the preceding claims, characterised in that the input signal controls the additional switch (6), which adjusts or compensates the charging current ( $I_e$ ) of the capacitor and causes the oscillator frequency to lock onto the input frequency.

6. FM detector according to claim 1, characterised in that the Schmitt trigger (4) has a lower switching potential ( $V_u$ ) and an upper switching potential ( $V_o$ ).

7. FM detector according to claim 6, characterised in that the charging current ( $I_e$ ) results from the summation of the direct current ( $I_m$ ) and the currents which can be adjusted by the switch (5) and the additional switch (6).