

The present invention relates to an integrated circuit of the logic circuit type comprising an electrically programmable non-volatile memory. It relates more specifically to an integrated circuit in which the electrically programmable non-volatile memory comprises a memory of the EPROM or EEPROM type. Such circuits are used, for example, in memory cards also called CCC cards. In this case the non-volatile memories are usually designed to receive confidential unalterable information which must not be subjected to parasitic programming as a result of abnormal conditions during use of the card.

In memories of the EPROM or EEPROM type currently available commercially, each information storage element, or memory cell, comprises a floating gate MOS transistor. This type of transistor can exist in two states. Thus, in the case of an N-channel transistor, in a first state no charge is stored on the floating gate. A conduction channel can exist between source and drain. The transistor then conducts and behaves like a closed switch. In a second state electrons have been stored on the floating gate. They inhibit the formation of a conduction channel in the substrate between source and drain. In this case the transistor is blocked and behaves like an open switch.

In order to program or read a floating gate MOS transistor, it must be possible to apply different voltages to the different electrodes of the transistor. These voltages are applied by means of write and read circuits controlled by specific signals.

Thus, as shown in Figure 1, which relates to an EPROM memory in which the memory cell comprises a floating gate transistor of the SAMOS (i.e. stacked gate avalanche injection MOS) type, each floating gate transistor 1 has two principal electrodes, 2 and 3 respectively, and a control gate 5 stacked on the floating gate 4. In the case of a memory, the floating gate transistors 1 comprising memory cells are connected in a matrix. Thus, a first principal electrode 2 or source in the technology used, is connected to the voltage V_{ss} corresponding to ground, whereas

the other electrode 3, or drain, is connected through the intermediary of a bit line (not shown) and an MOS transistor 8 forming a switch to a column address decoder 7. The control gate 5 is connected through the intermediary of another connection (not shown), called a word line, to a line address decoder 6.

More specifically, the column address decoder 7 is connected to the gate of the transistor 8 the source of which is connected to the electrode 3 of the floating gate MOS transistor 1, whereas its other electrode, or drain, is connected through the intermediary of a charge line constituted by MOS transistors 11 and 12 to the programming voltage V_{pp} . In practice, the charge line comprises a depletion mode MOS transistor 11, the drain of which is connected to V_{pp} and the source of which is connected to the drain of an enhanced mode MOS transistor 12, the gates of the two transistors 11 and 12 being connected together and being connected to a writing control circuit comprising a NOR gate 13 supplied with the voltage V_{pp} . The NOR gate 13 receives at its inputs the inverted command signal for programming $\overline{PGM}$ and the inverted data to be programmed $\overline{D}$. The signal $\overline{D}$ is emitted from a dynamic register R of known type. This register R makes it possible to perform the storage and refreshment of data. More specifically, it receives on its input the data to be written in the form of a logic level "1" or "0". Essentially it comprises storage means constituted by capacitors (not shown) provided in front of two inverters I1 and I2 and an MOS transistor 14 forming a switch connected between the output of the inverter I2 and the input of the inverter I1. This transistor is controlled by the signal CLK representing the clock signal of the memory. The MOS transistor 14 is used to perform the refreshment of the data. Thus, at the output of the inverter I1, namely at the node N', the data $\overline{D}$ is obtained which is passed to the input of the NOR gate 13.

Furthermore, the node N between the source of the MOS transistor 12 and the drain of the MOS transistor 8 is connected to a read amplifier represented by the block L.

The write circuit described above has a substantially dynamic mode of operation. Thus, the data D entered into the register R is stored in

the form of a charge on a high impedance node and this storage is refreshed periodically by making use of the clock signal CLK. If the stored information is not refreshed, the data D is lost and the write circuit behaves in a completely unpredictable manner. In the case where the integrated circuit is used in memory cards, for example, certain zones of the non-volatile memory are reserved, that is to say writing into them is strictly controlled and usually subject to the recognition of a secret code. However, with the write circuit described above, if the user sends pulses on the programming voltage V_{pp} supply, when the voltage V_{cc} is present but the clock signal CLK is absent, parasitic programming in the non-volatile memory is observed, even in the reserved zones. The reserved zones are then programmed in a quite random manner.

The aim of the present invention is to overcome these disadvantages which allow uncontrolled writing in an electrically programmable non-volatile memory.

Consequently, an object of the present invention is an integrated circuit of the logic circuit type comprising an electrically programmable non-volatile memory constituted by a matrix of memory cells of the floating gate transistor type, by write and read circuits and by means for organizing the interconnection of these circuits with the memory, the integrated circuit receiving a general supply voltage V_{cc} , a programming voltage V_{pp} and an external clock signal acting inter alia on the function of these write circuits, characterized in that the external clock signal is split into two internal complementary clock signals, the integrated circuit furthermore comprising a circuit for detecting the presence of internal clock signals sending a signal inhibiting writing in the memory when it detects the absence of one of the internal clock signals, the detection circuit (P) being constituted by a first circuit comprising a capacitor (C') and a resistor (R') connected in parallel between ground and a common connection ($N1'$), the capacitor being regularly charged through the intermediary of one (CLK1) of the two internal clock signals and a second circuit comprising a capacitor (C'') and a resistor (R'') connected in parallel between ground and a common

connection (N1"), the capacitor (C") being regularly charged through the intermediary of the other internal clock signal (CLK2), the common connections being connected respectively to each input of a logic gate (22) the output of which supplies a logic signal indicating the presence or absence of the clock signals.

In a preferred embodiment the logic gate is of the NOT-AND type.

Preferably, the output of the detection circuit is connected to the input of a gate the other input of which receives a signal essential for the control of writing in such a manner that writing is inhibited if the external clock signal is absent.

Other characteristics and advantages of the present invention will be apparent on reading the following description of different embodiments with reference to the attached drawings in which:

- Figure 1, already described, shows schematically a memory cell of an EPROM memory connected to its write and read circuits and also to means organizing the interconnection between the memory cell and the write and read circuits, and

- Figure 2 shows schematically an embodiment of a detection circuit in accordance with the present invention.

In order to simplify the description, similar elements in the Figures have the same reference numbers or letters. Furthermore, the description has been made with reference to MOS circuits made using NMOS technology and to an EPROM memory the memory cells of which comprise floating gate MOS transistors of the SAMOS (i.e. stacked gate avalanche injection MOS) type. It is evident to a person skilled in the art that the present invention can be used employing other technologies and other types of EPROM or EEPROM memory.

In general, in integrated circuits of the memory card type using electrically programmable non-volatile memories of the EPROM type,

instead of a single clock signal CLK, two complementary clock signals CLK1 and CLK2, derived from the clock signal CLK, are used. The clock signals CLK1 and CLK2 are obtained by passing the external clock signal CLK into a divider D which supplies two complementary clock signals CLK1 and CLK2 at the output.

In this case, the detection circuit in accordance with the present invention may be of the type shown in Figure 2. This detection circuit P is constituted by two identical circuits, each detecting the presence or absence of one of the internal clock signals CLK1 and CLK2, the outputs from which are sent to a NOT-AND gate 22. More specifically, the output signals CLK1 and CLK2 obtained from the divider D, from an external clock signal CLK applied on one of the inputs of the integrated circuit, are each passed to the gates 21' and 21" of the MOS transistors 19' and 19" forming switches in the first and second identical circuits which constitute with the gate 22 the detection circuit P. The first circuit is formed by connecting a capacitor C' in parallel with a resistor formed by an MOS transistor 15'. The transistor 15' is constituted by a depletion mode transistor connected in a load circuit, that is to say having a gate 18' connected to the source. The capacitor C' and the transistor 15' are connected between the voltage Vss forming the ground and the common node N1'. In addition, the node N1' is connected to the supply voltage Vcc through the intermediary of the MOS transistor 19' forming a switch, this transistor 19' receiving on its gate 21' the clock signal CLK1. The output of the first circuit is obtained from the node N1' and is applied to one of the inputs of the NOT-AND gate 22. In a similar manner, the second circuit comprises a capacitor C" and a resistor formed by an MOS transistor 15" connected in parallel. The transistor 15" is a depletion mode transistor connected in a load circuit, that is to say having a gate 18" connected to the source. The capacitor C" and the MOS transistor 15" are connected between the voltage Vss forming the ground and the common node N1". The node N1" is connected to the supply voltage Vcc through the intermediary of the MOS transistor 19" forming a switch, this MOS transistor 19" receiving on its gate 21" the clock signal CLK2. In addition, the node N1" forming the output of the second detection circuit is connected to the other input of the NOT-AND gate 22.

Figure 2 shows a circuit to make possible the inhibition of writing in an electrically programmable non-volatile memory by using the output signal from the NOT-AND gate 22. This inhibition circuit I comprises a NOR gate 23 which receives on one of its inputs the output signal of the NOT-AND gate 22 and on its other input the inverted programming control signal PGM.

The operation of the circuit shown in Figure 2 will now be explained. In fact, the first and second circuits comprised in the detection circuit P both operate in an identical manner. Thus, when the two signals CLK1 and CLK2 comprising pulses are present, the capacitors C' and C" become charged regularly at each change to the logic level "1". At the level of the nodes N1' and N1" a voltage which substantially corresponds to a logic level "1" is obtained. Furthermore, the charges present on the capacitors C' and C" are continuously discharged towards the voltage Vss representing ground through the intermediary of the transistors 15' and 15" connected in a load circuit. In order to avoid switching the voltage at the level of the nodes N1' and N1" between a logic level "1" and a logic level "0", the discharge time constant of the circuits constituted respectively by the capacitor C' or C" and the MOS transistor 15' or 15" connected in a load circuit is greater than the cycle period of the clock signals CLK1 and CLK2. Consequently, because the nodes N1' and N1" are at the logic level "1", the output of the NOT-AND gate 22 is at the logic level "0". Because of this a signal is obtained at the output of the NOR gate 23 which corresponds to the programming control signal PGM. If the clock signal CLK is absent, the two clock signals CLK1 and CLK2 are no longer pulses but constant signals and one of the two clock signals CLK1 and CLK2 is at the logic level "0". Consequently, one of the MOS transistors 21' or 21" acting as switches is open and the voltage at the level of one of the nodes N1' or N1" corresponds to the logic level "0". In this case the output of the NOT-AND gate is at the logic level "1" and as a result there is a logic level "0" at the output of the NOR gate 23 whatever the level of the signal PGM may be. This results in inhibition of writing in the electrically programmable non-volatile memory.

The advantage of the circuit described above is that it inhibits any random programming of an electrically programmable non-volatile memory designed principally to receive confidential data and it does this even in the case of operation outside normal conditions of supply voltage and clock signal. This circuit, moreover, is very simple in design, requires little space and is very reliable in operation.

It is evident to a person skilled in the art that the present invention can be adapted to any integrated circuit comprising memories in which the programming of a memory cell is performed in the same manner as in EPROM or EEPROM memories of the floating gate type and which have supply voltage and clock signal terminals which are easily accessible from the outside.

CLAIMS

1. An integrated circuit of the logic circuit type comprising an electrically programmable non-volatile memory constituted by a matrix of memory cells of the floating gate transistor (1) type, by write and read circuits (R, 11, 12, 13 and L) and by means (6, 7 and 8) for organizing the interconnection of these circuits with the memory, the integrated circuit receiving a general supply voltage V_{cc} , a programming voltage V_{pp} and an external clock signal (CLK) acting inter alia on the function of these write circuits, characterized in that the external clock signal (CLK) is split into two internal complementary clock signals (CLK1 and CLK2), the integrated circuit furthermore comprising a circuit (P) for the detection of the presence of internal clock signals sending a signal inhibiting writing in the memory when it detects the absence of one of the internal clock signals, the detection circuit (P) being constituted by a first circuit comprising a capacitor (C') and a resistor (15') connected in parallel between ground and a common connection (N1'), the capacitor being regularly charged by the intermediary of one (CLK1) of the two internal clock signals and a second circuit comprising a capacitor (C'') and a resistor (15'') connected in parallel between ground and a common connection (N1''), the capacitor (C'') being regularly charged by the intermediary of the other internal clock signal (CLK2), the common connections being connected respectively to each input of a logic gate (22) the output of which supplies a logic signal indicating the presence or absence of the clock signals.
2. An integrated circuit as claimed in claim 1, characterized in that the logic gate (22) is of the NOT-AND type.
3. An integrated circuit as claimed in claim 1, characterized in that the resistor (15' and 15'') is constituted by an MOS transistor arranged in a load circuit.
4. An integrated circuit as claimed in claim 3, characterized in that the MOS transistor arranged in a load circuit is constituted by a



depletion mode MOS transistor the gate of which is connected to one of the main electrodes.

5. An integrated circuit as claimed in any one of claims 1 to 4, characterized in that the common connection (N1' and N'') is connected to the supply voltage Vcc through the intermediary of an MOS transistor (19' and 19'') the gate of which receives the clock signal (CLK1 and CLK2).

6. An integrated circuit as claimed in any one of claims 1 to 5, characterized in that the discharge constant of the circuit constituted by the capacitor and the resistor is greater than the cycle period of the clock signal.

7. An integrated circuit as claimed in any one of claims 1 to 6, characterized in that the output of the detection circuit (P) is connected to the input of a gate (23) the other input of which receives an essential signal (PGM) for the control of writing in such a manner that writing is inhibited if at least one of the internal clock signals is absent.

