

ABSTRACT

A semiconductor failure analysis device 1 includes an analysis part 10 that analyzes a failure place in a semiconductor device D; a marking part 20 that irradiates the semiconductor device D with laser light; a device arrangement part 30 in which a wafer chuck 32, which holds the semiconductor device D and on which an alignment target 50 is provided, moves relative to the analysis part 10 and the marking part 20; and a control part 41b that outputs commands to the analysis part 10, the marking part 20 and the device arrangement part 30. The control part 41b moves the wafer chuck 32 to a position at which the analysis part 10 is capable of taking an image of the alignment target 50, then outputs an alignment command that causes the marking part 20 to be aligned with the analysis part 10 with the alignment target 50 as a reference, and irradiates the semiconductor device D with laser light in a state in which a positional relationship between the marking part 20 and the analysis part 10 is maintained.

FIG. 1