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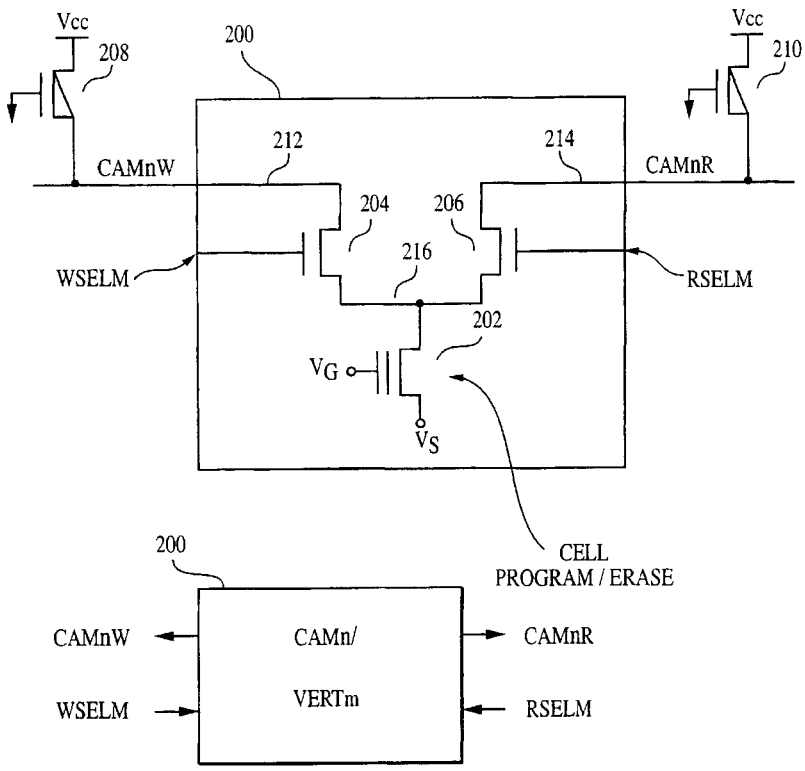
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(54) Title: DUAL-PORTED CAMS FOR A SIMULTANEOUS OPERATION FLASH MEMORY



(57) Abstract: A flash memory having redundancy content addressable memory (CAM) circuitry (106) is described. The flash memory is capable of substituting a second memory cell for an inoperative memory cell. The flash memory includes a primary array (118, 120, 122, 124, 134, 136, 138, 140) of memory cells, a redundant array (126, 128, 130, 132, 142, 144, 146, 148) of memory cells, and the redundancy CAM circuitry (106). The redundancy CAM circuitry (106) includes a plurality of dual-ported CAM stages (200). Each CAM stage (200) includes a CAM cell (202), a write data bus (204) coupled to the CAM cell (202), and a read data bus (206) coupled to the CAM cell (202). The CAM cell (202) stores information regarding a location of an inoperative memory cell in the primary array (118, 120, 122, 124, 134, 138, 140). The inoperative memory cell requires a substitution with a second memory cell in the redundant array (126, 128, 130, 132, 142, 144, 146, 148). The write data bus (204) produces the information from the CAM cell (202) responsively to a write select signal (WSELm). The write select signal (WSELm) is indicative of a write operation to be performed at memory cell locations in the primary array (18, 120, 122, 124, 134, 136, 138, 140). The read data bus (206) produces the information from the CAM cell (202) responsively to a read select signal (RSELm). The read select signal (RSELm) is indicative of a read operation to be performed at memory cell locations in the primary array (118, 120, 122, 124, 134, 136, 138, 140).

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