ABSTRACT

A METHOD TO FORM POLYCIDE LOCAL INTERCONNECTS BETWEEN NARROWLY-SPACED FEATURES WHILE ELIMINATING STRINGERS

A method of fabricating local interconnects of polycide has been achieved. A substrate is provided. Narrowly spaced features, such as MOS transistor gates and polysilicon traces, are provided overlying the substrate. A dielectric layer is deposited overlying the substrate and the narrowly spaced features. The dielectric layer is patterned to form openings between the narrowly spaced features for planned contacts to the surface of the substrate. A doped polysilicon layer is deposited overlying the dielectric layer and filling the openings. The doped polysilicon layer is etched down to the top surface of the narrowly spaced features. The doped polysilicon layer remains in the spaces between the narrowly spaced features. A polycide layer is formed overlying the narrowly spaced features and the doped polysilicon layer. The polycide layer and the doped polysilicon layer are patterned to complete the contacts and create the local interconnects of polycide, and the integrated circuit device is completed.

(FIGURE 5 IS SUGGESTED FOR PUBLICATION)