

Radio device including a frequency synthesizer and phase discriminator for such a device.

DESCRIPTION

FIELD OF THE INVENTION

The present invention relates to a radio device comprising a frequency
5 synthesizer that notably includes a phase discriminator for comparing the phase of a first
signal with the phase of a second signal, the phase discriminator being formed by a first
sequential circuit for producing output signals that represent the phase difference between said
first and second signals.

The invention also relates to such a discriminator and a process for comparing
10 the various phase levels of two signals.

BACKGROUND OF THE INVENTION

Such devices are well known and find many applications, notably in the field of
portable telephones that use a great many frequency channels determined by the synthesizer. It
will be recollected that a synthesizer is formed, in essence, by a voltage-controlled variable
15 oscillator slaved to a reference frequency after a frequency division that ultimately determines
the output frequency of the synthesizer.

When the device is in the stand-by mode, it is more or less periodically to be
connected to the network and, for reasons of saving energy, it is desirable for the synthesizer
to be longest possible in the state of rest, that is, that this implies that the variable oscillator is
20 synchronized with the reference frequency in the fastest possible way. One of the elements
that enable to obtain a fast synchronization is the phase discriminator. In patent document EP
0 500 014 the description of such a discriminator can be found.

If this known discriminator offers good indications as regards the phase
differences between $-\pi$ and $+\pi$, these indications are no longer sufficient for greater phase
25 differences, thus for signals having different frequencies.

SUMMARY OF THE INVENTION

The invention proposes a device in which the discriminator features a good
characteristic of the phase level, so as to notably obtain a fast synchronization of the variable
oscillator.

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Therefore, such a device is characterized in that the discriminator includes a second sequential circuit for producing a constant signal when said first and second signals have different frequencies.

Thus, thanks to the invention, when the frequencies of the signals are different, the DC signal whose value is equal to a maximum permits the rapid correction of the frequency of the voltage-controlled oscillator to obtain the synchronization of the oscillator in the fastest way.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects of the invention are apparent from and will be elucidated, by way of non-limitative example, with reference to the embodiment(s) described hereinafter.

In the drawings:

Fig. 1 shows a device in accordance with the invention,

Fig. 2 shows the diagram of a synthesizer forming part of the device shown in Fig. 1,

Fig. 3 shows the diagram of a discriminator that forms part of the synthesizer shown in Fig. 2.,

Fig. 4 is a first timing diagram intended for the explanation of the discriminator shown in Fig. 3,

Fig. 5 is a second timing diagram intended for the explanation of the discriminator shown in Fig. 3, and

Fig. 6 represents the discriminator response curve.

DESCRIPTION OF PREFERRED EMBODIMENTS

In Fig. 1 is represented a radio device in accordance with the invention. It is formed by a transmission circuit 1 and a receiving circuit 2 coupled to an antenna 5 via a duplexer 8. The transmission circuit 1 is formed by a microphone 11, followed by an analog/digital converter 12 which produces the speech signals to be transmitted to a modulation system 15. The receiving circuit 2 is formed by a demodulation system 20, followed by a decoder 25 and a loudspeaker 27. The receiving and transmission systems are controlled via the frequency channel by means of a synthesizer 30.

Fig. 2 shows the structure of the synthesizer 30 of a conventional type. It is formed by a voltage-controlled oscillator 35 whose signals are frequency-divided by a

frequency divider 37. The frequency division rate determines the frequency channel on which the transport will take place. The signal E1, which is the output signal of the divider 37, is compared by a phase discriminator 40 with a signal E2, which is the output signal of a quartz crystal oscillator 39. The output signal S of this discriminator is applied to the voltage-controlled oscillator 35 via a control filter 42.

Fig. 3 shows in detail the phase discriminator according to the invention.

The signals E1 and E2 are applied to the clock inputs of two D-type flip-flops referenced 51 and 52, respectively. These flip-flops permanently receive a signal having the logic "1" value on their input D, whereas the input R receives the output signal of a NAND gate 55. The output signals Q1 and Q2 of these flip-flops 51 and 52 are applied not only to the inputs of the gate 55, but also to the inputs J of the flip-flops 61 and 62 of the type JK, to the inputs K of the flip-flops 61 and 62 and to the first inputs of the OR gates 71 and 72. The outputs of these flip-flops 61 and 62 are applied to the inputs of a circuit known by the name of current pump 75 of a conventional type. The second inputs of these gates 71 and 72 are connected to the outputs of the latter flip-flops 61 and 62. The clock inputs of the flip-flops 61 and 62 receive the respective signals E1 and E2 and their output Q produces the signals QQ1 and QQ2, respectively.

In brief, this discriminator comprises a first sequential circuit formed by the flip-flops 51 and 52 which has the structure of known phase discriminators, a second sequential circuit formed by the flip-flops 61 and 62 and a coupling circuit mainly formed by the OR gates 71 and 72, which coupling circuit enables to feed control signals to the current pump from these sequential circuits.

The operation of the discriminator is explained for a first embodiment with the aid of Fig. 4. This mode relates to the case where the signals E1 and E2 have the same frequency. One starts from instant t_0 and considers that the signals Q1 and Q2 on the outputs of the flip-flops are in the logic "0" state. At the instant t_1 the low-to-high transition of the signal E1 occurs to which the flip-flops are sensitive, so that the flip-flop 51 transfers the "1" value, which was present on its input D, to its output Q. The signal Q1 then assumes the "1" value. At the instant t_2 it is the rising edge of the signal E2 that occurs, which makes that the signal Q2 on the output of the flip-flop 52 assumes the "1" value. But this state changes because of the fact that an active signal coming from the gate 55 having values "0" is applied to the inputs R of the flip-flops 51 and 52. Thus after the instant t_2 , the signals Q1 and Q2 assume the "0" value.





As regards the flip-flops 61 and 62, it should be observed that before the active transitions of the signal E1, the signal Q1 has the "0" value and the signal Q2 the "0" value, which makes that the signal QQ1 retains its value. It should also be observed that before the active transitions of the signal E2, the signal Q1 has the "1" value and the signal Q2 the "0" value, which makes that the signal QQ2 assumes the "0" value. Thus, the OR gates 71 and 72 are open and the operation of the discriminator remains that of the prior-art discriminators.

The operation of the discriminator according to another embodiment, for which the signals have different frequencies, is explained with the aid of Fig. 5. Thus in this Figure, between a first transition of the signal E1 that occurs at instant t10 and a second transition of this same signal, there are two transitions of the signal E2 which appear at the instants t11 and t12. As the transition of E2 occurring at the instant t11 comes later than at the instant t10, one is thus certain that at the instant t12 the signals Q1 and Q2 have the "0" value. Thus, after this instant t12 one has Q2 = "1" and Q1 = "0", so that at instant t13, where an active transition of E1 appears, Q1 assumes the "1" value and soon loses it due to the output signal of the gate 55.

After this instant t13, the signal QQ1 assumes the "0" value.

After that, at instant t14, the active edge of the signal E2 occurs, which edge will influence the flip-flops 52 and 62, the signal Q2 will change from the "0" value to the "1" value and because of this fact the signal QQ2 will have the "1" value.

At the instant t15 another active edge of the signal E2 occurs, the signal Q2 retains its "1" value, whereas the signal QQ2 keeps its "1" value.

At the instant t16, an active edge of the signal E1 occurs this time. Thus, the signal Q1 assumes the "1" value and loses it soon because the NAND gate is rendered conductive by the signal Q2. Signal QQ1 retains the "0" value acquired during the instant t13, because on its inputs J and K it receives the signals "0" and "0", respectively.

At the instant t17 a rising edge of the signal E2 occurs. It is admitted that this edge occurs after the transient rise of the signal Q1, so that at the inputs J and K of the flip-flop 62 there are the signals "0" and "0", thus the flip-flop keeps its state prior to the instant t17. At the instant t18, which is the instant at which a rising edge of the signal E2 occurs, the signal QQ2 still keeps the "1" value. The same state remains for this signal at the instant t19 where there is still a rising edge of the signal E2. Before the instant t20, the signals at the inputs J and K of the flip-flop 62 had the respective values "0" and "1", which keeps the signal QQ1 at "0".

Thus, it is taken into account that when the frequencies of the signals are different, the signals QQ1 and QQ2 remain constant, which makes it possible to have an error signal that causes the oscillator 35 (Fig. 2) to be synchronized fast. This is diagrammatically shown in Fig. 6, which

shows the response of the discriminator of Fig. 3, that is, the variation of the signal S as a function of the phase error and/or frequency error of the signals E1 & E2 $\Phi(E1, E2)$. It will be noted that there is a hysteresis effect involved. Actually, if the frequencies are close together, the signals QQ1 and QQ2 do not change value. For making this obvious, Fig. 5 shows that the edges 18 and 19 no longer occur, the signals Q1 and Q2 thus keep the "0" value (dotted curve) which provides that neither of the flip-flops 61 and 62 changes state. When phase coincidence is reached, the solid-line curve of Fig. 6 is described.

It is possible to realize the circuits of the invention in a different manner. For example, by using logic circuits coupled to memory elements.

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CLAIMS:



1. A radio device comprising a frequency synthesizer that notably includes a phase discriminator for comparing the phase of a first signal with the phase of a second signal, the phase discriminator being formed by a first sequential circuit for producing output signals that represent the phase difference between said first and second signals, characterized in that the discriminator includes a second sequential circuit for producing a constant signal when said first and second signals have different frequencies.
2. A device as claimed in claim 1, characterized in that said second sequential circuit is formed by at least one flip-flop that has a clock input for receiving the first and second signal respectively, and a junctor circuit for putting these flip-flops in a stable state for different frequencies of said first and second signals.
3. A device as claimed in claim 1 or 2, in which the discriminator includes a current pump circuit that has a control input for logic signals, characterized in that said discriminator includes a coupling circuit for supplying to said control input signals defined by said second sequential circuit when said first and second signals have different frequencies and signals defined by said first sequential circuit when said signals are passed through because they have phase coincidence.
4. A phase discriminator suitable for a device as claimed in one of the claims 1 to 3, characterized in that it is formed, inter alia, by a first sequential circuit for producing output signals that represent the phase difference between said first and second signals, and a second sequential circuit for producing a DC signal when said first and second signals have different frequencies.
5. A discriminator as claimed in claim 4, characterized in that it includes a coupling circuit for supplying to said control input signals defined by said second sequential circuit when said first and second signals have different frequencies and signals defined by





said first sequential circuit when said signals are passed through because they have phase coincidence.

6. A process used in a device as claimed in one of the claims 1 to 3 for controlling
5 a signal frequency synthesizer, characterized in that a frequency discriminator is used which produces phase-difference signals for signals applied to its inputs that have a same frequency and constant signals for signals applied to its inputs that have different frequencies.

7. A method as claimed in claim 6, characterized in that a hysteresis cycle is
10 provided for keeping the output signal of the discriminator at a constant level when the signals, after having had different frequencies, thereafter feature a same frequency with a different phase.

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