

Silicide/Semiconductor Structure and Method of Fabrication

[0001] This application claims priority to provisional patent application serial number 60/498,775, filed August 29, 2003, entitled "A Silicide/Semiconductor Structure and Method of Fabrication," which application is incorporated herein by reference.

TECHNICAL FIELD

[0002] This invention is related generally to semiconductor devices, and more specifically to devices employing low band gap materials.

BACKGROUND

[0003] As the size of semiconductor devices in VLSI circuits continues to shrink, the impact of contact resistance in device performance is becoming more important. Generally, when metal is in contact with doped silicon, such as at the contact to a transistor source or drain region or gate electrode, a Schottky barrier is formed at the interface. This Schottky barrier contributes to a higher contact resistance, thus decreasing device performance. Generally, higher contact resistance degrades drive current, which in turn limits device performance and speed, increases device heating, and causes other undesirable consequences.

[0004] One approach to lowering contact resistance is to increase the doping concentration of the semiconductor region to which contact is made, typically a transistor source or drain region or gate electrode, although the region could be a doped polysilicon resistor, a capacitor plate, or some other doped region. Traditionally, such regions are formed from a doped silicon region, e.g., a silicon or polysilicon layer that has been doped with impurities such as arsenic, phosphorous, boron, and the like. Generally, increasing the level of the impurity concentration impacts many device characteristics, including decreasing undesirable contact resistance. Silicon

has limited impurity solubility, however, so the ability to decrease contact resistance by increasing the dopant concentration cannot proceed beyond the impurity solubility limits of the silicon. The impurity concentration level may have significant impact on other device characteristics as well, and hence the impact on contact resistance cannot be taken in isolation of other ways that the impurity concentration may affect device performance. This may further limit the ability to reduce contact resistance by increasing impurity concentration.

[0005] The use of a silicide layer for decreasing the contact resistance is also known. In conventional devices, a metal silicide layer is formed on the doped region to which contact is to be made. This silicide region is typically formed either by depositing a silicide layer (e.g., titanium silicide, tungsten silicide, cobalt silicide) on the silicon or polysilicon region to which contact is to be made (e.g., a source or drain region, a gate region, a doped polysilicon layer), or by converting a portion of the silicon or polysilicon region to a silicide (an *in situ* process by which a metal film is deposited on the region and wherein the metal and (poly)silicon interact to form a silicide in a subsequent thermal processing step).

[0006] As the trend toward smaller device geometries increases, coupled with the desire for still further improved device performance, the need exists for structures and methods that will allow for decreased contact resistance. This is particularly true for devices having gate lengths in the 90 nm and below range.

SUMMARY OF THE INVENTION

[0007] A preferred embodiment of the present invention comprises a dielectric/metal/ 2^{nd} energy bandgap (E_g) semiconductor/ 1^{st} E_g substrate structure. In order to reduce the contact resistance, a semiconductor with a lower energy bandgap (2^{nd} E_g) is put in contact with metal. The energy bandgap of the 2^{nd} E_g semiconductor is lower than the energy bandgap of the 1^{st} E_g semiconductor and preferably lower than 1.1 eV. In addition, a layer of dielectric may be deposited on the metal. The dielectric layer has built-in stress to compensate for the stress in the metal, 2^{nd} E_g semiconductor and 1^{st} E_g substrate. A process of making the structure is also disclosed.

[0008] The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter, which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0010] Figure 1 is a cross-sectional view of a dielectric / metal / second bandgap semiconductor material / first bandgap semiconductor material structure;

[0011] Figures 2a through 2g are cross-sectional views of intermediate stages in the manufacture of a MOS transistor embodiment; and

[0012] Figure 3 is a cross-sectional view of a MOS transistor with a composite dielectric layer.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0013] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0014] An integrated circuit structure with low contact resistance is described wherein a second semiconductor material with lower energy bandgap is disposed between a contact metal and a substrate. Reducing the energy bandgap of the semiconductor may reduce the Schottky barrier. Figure 1 illustrates the cross-sectional view of a dielectric / metal / second energy bandgap semiconductor material / first energy bandgap semiconductor material structure. Figures 2a through 2g illustrate processing steps in forming a CMOS device that employs the structure shown in Figure 1. Throughout the drawings, like reference numerals will be used to indicate the same or corresponding features.

[0015] In Figure 1, substrate 2 is preferably a semiconductor or insulator. More preferably, substrate 2 is formed of silicon, either a bulk silicon wafer or a layer of silicon formed on an insulating layer such as a buried oxide layer (BOX), in the well-known silicon-on-insulator (SOI) structure. In other embodiments, substrate 2 may be formed of other semiconductor or insulator materials such as silicon dioxide, oxynitride, nitride or high-k dielectrics. Semiconductor material 12 is preferably a semiconductor material having a bandgap energy that is lower than the bandgap energy of the underlying silicon layer 2. In preferred embodiments, the second bandgap energy layer 12 is epitaxially grown on substrate 2. Preferably, layer 12 has a bandgap energy of less than 1.1 eV, which is below the bandgap energy of 1.12 eV for silicon substrate 2.

Semiconductor 12 generally lowers the Schottky barrier formed at the metal to semiconductor interface. As discussed above, the lower bandgap energy generally lowers contact resistance.

[0016] In some embodiments, a crystal lattice mismatch between substrate 2 and semiconductor layer 12 may cause stress (either compressive or tensile depending upon the materials chosen and the method of deposition) to develop at the interface between the materials. This stress may also propagate throughout layer 12, potentially degrading device performance and reliability. As will be discussed in further detail below, this stress may be compensated for in subsequently applied layers.

[0017] Also illustrated in Figure 1 is metal 14 deposited on semiconductor layer 12. Preferably, metal 14 is a metal compound or alloy of transition metals. As described in more detail below, metal 14 may be a silicide formed on the surface of semiconductor layer 12. Since metal 14 is in direct contact with semiconductor layer 12, at equilibrium the carriers flow a short distance across the interface causing a build up of charges on both sides of the interface, thereby forming a Schottky barrier. The height of the barrier is approximately determined by the bandgap of the semiconductor, in addition to other factors. Semiconductor layer 12 is selected to have a bandgap energy below that of the substrate 2 so that the Schottky barrier height between metal 14 and semiconductor 12 will be smaller than the barrier height between a directly contacting metal 14 and substrate 2 interface.

[0018] Dielectric layer 16 is deposited on metal 14. The thickness is preferably between 50Å - 1000Å, and more preferably about 200-600Å. Generally, dielectric layer 16 may serve three primary purposes. First, dielectric layer 16 compensates for the stress arising from the lattice mismatch between semiconductor layer 12 and metal 14 and between semiconductor layer 12 and substrate 2. By relieving the stress caused by lattice mismatch, the number of defects in

the metal 14, semiconductor layer 12 and substrate 2 can be reduced, thus improving device reliability and performance. As will be described in greater detail below, dielectric layer 16 can be deposited to have significant stress properties, perhaps higher than 400 MPa in order to compensate for significant stress in the underlying layers.

[0019] Second, dielectric layer 16 preferably acts as an etch stop layer and provides a margin of error for over-etching of subsequently formed layers, such as a subsequently formed inter-level dielectric (ILD) layer. Generally, as device geometries shrink, the thickness of silicide layer 14 also shrinks. For instance, an exemplary MOS device having a gate geometry of 0.13 microns might have a silicide layer (metal layer 14) of only 300-400Å in thickness. For 90 nm, 65 nm, and smaller geometry devices, the silicide layer generally will be concomitantly thinner, which significantly increases the risk that the silicide layer will be etched away when the contact window is opened in a subsequently formed ILD. While etch end-point detection technology provides for a high degree of accuracy, there is very little margin of error with silicide regions as thin as described herein. Dielectric layer 16 provides for an additional margin of error by acting as an etch stop for the overlying ILD. With dielectric layer 16 positioned between ILD 18 (Figure 2f) and the silicide layer, etching may be performed in two steps. First, etching ILD layer 18 and stopping at dielectric layer 16. Since ILD layer 18 is much thicker than dielectric layer 16, it is difficult to etch through ILD layer 18 and stop precisely at dielectric layer 16. Overetching into dielectric layer 16 should not be a big concern as long as layer 16 is not completely etched through. Second, etching dielectric layer 16 and stopping at silicide layer 14. Dielectric layer 16 (200-600Å) is significantly thinner than ILD layer 18, so it is much easier to etch through it and stop at a thin layer of silicide than to etch through a thick layer of ILD 18 (typically > 3000Å) and stop at the thin silicide layer 14.

[0020] Third, dielectric layer 16 helps stabilize the underlying silicide by inhibiting contamination during downstream process steps. Such contamination may come from the oxidation of the silicide layer during the deposition of ILD layer 18. Further details are provided in "Advanced Thermally Stable Silicide S/D Electrodes for High-Speed Logic Circuits with Large-Scale Embedded Ta₂O₅-Capacitor DRAMS," by M. Saito, et al., IEDM 99-805, which is hereby incorporated herein by reference.

[0021] Figures 2a through 2g illustrate one embodiment of the present invention wherein the structure illustrated in Figure 1 is integrated into the process of forming a MOS transistor. One skilled in the art will recognize that the teachings herein could apply to a wide range of devices, including NMOS and PMOS transistors, CMOS devices, doped polysilicon resistors, integrated capacitors and inductors, and contact regions to bulk silicon. Other applications of the teachings contained herein will become apparent with routine experimentation. In the illustrated embodiment, the dielectric / metal / second bandgap energy semiconductor / first bandgap energy substrate structure is used in source and drain regions to lower contact resistance. The structure may also be used in the gate electrode region as well.

[0022] Figure 2a illustrates a substrate 2 with Shallow Trench Isolation (STI) regions 4. The STI regions are preferably formed by etching shallow trenches in substrate 2, and filling the trenches with an insulator such as silicon oxide. As is well known, STI regions isolate the active regions in which transistors and the like will be formed. Substrate 2 can be either a bulk semiconductor wafer or an SOI configuration. In other embodiments, substrate 2 may be strained-Si on relaxed SiGe; it may also comprise Si, Ge, C, a compound semiconductor or combinations thereof.

[0023] Gate dielectric 6 and gate electrode 8 are also illustrated in Figure 2a. As is known in the art, a gate dielectric layer is first formed on substrate 2, followed by a gate electrode layer. These layers are then patterned and etched to form the gate electrode 8 and gate dielectric layer 6. Gate dielectric layer 6 may comprise SiO₂, oxynitride, nitride and high-k materials. Gate electrode 8 is preferably polysilicon, although it may be formed of metal or a compound structure of dielectric / metal / semiconductor. This compound structure plus the gate dielectric may be formed from the structure disclosed in Figure 1.

[0024] Figure 2b illustrates a pair of spacers 10 formed along the sidewalls of the gate dielectric 6 and gate electrode 8. Spacers 10 serve as self-aligning masks for subsequent source/drain formation steps, as described below. The spacers may be formed by well-known methods such as blanket depositing a dielectric layer over the entire region including substrate 2 and gate electrode 8, then anisotropically etching to remove the dielectric from the horizontal surfaces and leaving spacers 10. Doping of the regions of substrate 2 on either side of gate dielectric 6 or spacers 10 may be performed to form part or all of the transistor source and drain regions.

[0025] As shown in Figure 2c, a semiconductor material 12, which may be used as part or all of the transistor source and drain regions, is epitaxially deposited to a thickness of 400Å – 600Å. A preferred method of forming semiconductor material 12 is selective epitaxy. An SiO₂ layer is formed to cover the substrate. Openings are then formed through the SiO₂ to expose the source/drain regions. Semiconductor material 12 is then epitaxially grown. Semiconductor material 12 is preferably formed using Molecular Beam Epitaxy (MBE), although other deposition techniques, including Chemical Vapor Deposition (CVD), Ultra High Vacuum Chemical Vapor Deposition (UHVCVD), Atomic Layer Chemical Vapor Deposition (ALCVD)

or Metal Organic Chemical Vapor Deposition (MOCVD). Deposition preferably occurs at a temperature in the range of 300°C - 950°C, and more preferably in the range of 450°C to 850°C, and at a pressure less than 100 mTorr. In the region where the single crystal substrate is exposed, semiconductor layer 12 is grown epitaxially. On the SiO₂ layer, poly-crystal is formed. The poly-crystal and SiO₂ are then etched, leaving only semiconductor layer 12. Semiconductor material 12 forms part of the source and drain regions for the resulting MOS transistor.

Generally, it is desirable that the source and drain regions formed from semiconductor material 12 be highly doped (e.g., $>2 \times 10^{20} \text{ cm}^{-3}$).

[0026] Doping of semiconductor material 12 can be accomplished either during the epitaxial growth process or subsequently in an ion implantation step. In a preferred embodiment, doping of semiconductor material 12 occurs concurrently with the epitaxial growth step. This is accomplished by introducing appropriate dopants, such as boron, phosphorous, arsenic, and the like into the chamber along with other process gases, such as silicon, germanium, hydrogen, chlorine, nitrogen, helium, and the like, during the epitaxial growth step.

[0027] Semiconductor layer 12 has an energy bandgap lower than the underlying substrate 2, which is typically lower than 1.1 eV when the substrate is silicon. In a preferred embodiment, semiconductor layer 12 comprises a Si and Ge compound. Carbon can optionally be added to compensate for the lattice spacing difference between semiconductor layer 12 and substrate 2. In a preferred embodiment, the germanium content is more than 10%, and more preferably in the range of 10% to 50%. The carbon content is typically less than 4%, and preferably in the range of 0.1% to 2%.

[0028] In other embodiments, instead of being formed on the surface of substrate 2, semiconductor material 12 is recessed (partly or in whole) in substrate 2. A pair of recesses (not

shown) is formed on either side of gate electrode 8 by etching substrate 2. Note that substrate 2 may be undercut beneath spacers 10, resulting in the recesses being aligned with gate electrode 8. Spacers 10 are designed so as to allow for precise alignment of the recesses with the gate electrodes. In other embodiments, spacers 10 may be designed so that the recessed regions are spaced apart (in the vertical alignment sense) from the gate electrode 8. In yet other embodiments, it may be desirable to have recesses formed within the vertical boundaries of gate electrode 8, such that the channel region resulting from the subsequently formed source and drain regions is shorter than the gate electrode width. One skilled in the art will recognize that the optimum alignment of the recesses can be derived through routine experimentation. In a preferred embodiment, wherein substrate 2 is a semiconductor wafer or a semiconductor layer on an underlying BOX insulator, recesses may be formed by anisotropically etching the substrate using, e.g., ion etching.

[0029] In other embodiments, semiconductor material 12 may have a layered structure and the top layer may cover all of the bottom layer or only part of the bottom layer. In this embodiment, the bandgap of the top layer, which is in direct contact with metal, is lower than the bandgap of substrate 2.

[0030] As illustrated in Figure 2d, metal layer 14 is formed over source and drain regions and preferably over gate electrode 8 as well. The thickness of metal 14 is preferably less than about 500Å. Metal 14 may be a transition metal or metal compound such as titanium, cobalt, tungsten, tantalum, or the like or other appropriate conductive material deposited via Chemical Vapor Deposition (CVD), Physical Vapor Deposition (PVD) or other alternatives. As discussed, a Schottky barrier formed between metal 14 and semiconductor material 12 has a lower barrier height than a barrier height that would be formed between direct contact of metal 14 and

substrate 2. Layer 14 is referred to interchangeably as a metal layer or a silicide layer in the specification. It should be recognized that, depending upon the embodiment, layer 14 could be either a metal layer or a silicide formed from a metal layer that has interacted with the underlying semiconductor regions, or a combination thereof (e.g., a metal layer over a silicide layer).

[0031] In a preferred embodiment, metal 14 is a metal silicide. The metal silicide may contain N or C, and may contain between 1% and 25% Ge, preferably 1-5% Ge. The metal silicide may take the form of transition-metal silicide and may contain more than one transition metal. In a preferred embodiment, metal layer 14 is formed by first depositing a thin layer of metal, such as titanium, cobalt, nickel, tungsten, or the like, over the device, including the exposed surfaces of semiconductor layer 12 and gate electrode 8. The device is then annealed at a temperature higher than 300°C, and preferably between 400-800°C, and at a pressure lower than about 10 Torr, and more preferably lower than about 1 Torr to form a silicide between the deposited metal and the underlying exposed silicon regions (specifically source/drain regions and polysilicon gate conductor 8). The resulting metal silicide regions are illustrated as metal layer 14 in Figure 2d. Preferably, the resulting silicide layer 14 is in the range of 300Å to 500Å thick, although the desired thickness is a matter of design choice. In yet another embodiment, silicide layer 14 could be formed by the deposition of a silicide, such as cobalt silicide or nickel silicide, directly onto the surface of source and drain regions and gate electrode 8 using known deposition techniques, such as CVD.

[0032] As illustrated in Figure 2e, a dielectric layer 16 is next blanket deposited over the device. Dielectric layer 16 is preferably formed to a thickness of about 50Å - 1000Å. Dielectric layer 16 may be formed using Low Pressure Chemical Vapor Deposition (LPCVD), but other CVD methods, such as Plasma Enhanced Chemical Vapor Deposition (PECVD), and thermal

CVD may also be used. As discussed above, dielectric layer 16 is preferably chosen not only for its dielectric properties, but also for its ability to compensate for stress arising from the lattice mismatch between semiconductor material 12 and metal layer 14 and between semiconductor material 12 and underlying substrate 2. The lattice mismatch may cause performance degrading defects at the interfaces, which defects may propagate throughout the affected layers.

[0033] In the above preferred embodiments, in which source and drain regions of SiGeC are formed on a silicon substrate and a silicide layer is formed on the upper surface of the source and drain regions, the lattice mismatch between the layers may cause an overall stress (e.g., tensile or compressive) on the silicide layer, typically in the range of 400Mpa-4GPa. The material and deposition method of dielectric layer 16 may be chosen, at least in part, to compensate for this stress. In a preferred embodiment, dielectric layer 16 is formed of a composite oxide/oxynitride structure, in which a first oxide sub-layer of approximately 100Å is first formed, followed by an oxynitride layer of approximately 300Å. The oxide and oxynitride layer is preferably formed by PECVD at a temperature lower than 550°C. Figure 3 illustrates a device employing an oxide/oxynitride composite dielectric layer 16, where material 24 is oxynitride and material 22 is oxide.

[0034] The above described dielectric layer will preferably provide for stress of approximately 400MPa-4GPa, preferably in the range of 400MPa-2GPa. One of ordinary skill in the art will recognize that a wide range of compressive and tensile stresses can be compensated for by adjusting the materials used for dielectric layer 16 and the method of deposition. For instance, silicon nitride deposited by Low Pressure Chemical Vapor Deposition (LPCVD) may be used to provide for tensile film stress. Likewise, silicon nitride deposited by PECVD may be used to provide for compressive film stress.

[0035] As illustrated in Figure 2f, an inter-level dielectric (ILD) layer, also sometimes known as a pre-metal dielectric (PMD) or an inter-metal dielectric (IMD) layer, is next deposited over the surface of the dielectric layer 16. This ILD layer 18 is preferably silicon dioxide deposited using, e.g., Tetraethyl orthosilicate (TEOS), CVD, PECVD, LPCVD, or other well-known deposition techniques. This ILD layer 18 provides insulation between the transistor and overlying metal lines. A photoresist material (not shown) may be formed and patterned over the ILD layer 18 in order to form contact openings to the source and drain regions and the gate dielectric. Figure 2g illustrates the device after the exposed portions of ILD dielectric layer 18 have been etched away, thus opening contact openings in the ILD dielectric layer. Note that dielectric layer 16 operates as an etch stop layer during the etching of ILD dielectric layer 18 and thus protects the underlying silicide layer 14. Next, the exposed portions of dielectric layer 16 in the contact openings are etched, preferably using Reactive Ion Etching (RIE). Because dielectric layer 16 is quite thin relative to ILD dielectric layer 18, process control and end-point detection are more closely controlled, thus limiting the likelihood of over-etching through the underlying silicide layer 14.

[0036] Figure 2g illustrates the device after metal plugs 20 have been formed in the contact openings. Metal plugs 20 may be formed of tungsten, aluminum, copper, or other well known alternatives. Metal plugs 20 may also be composite structures, including, e.g., barrier and adhesion layers, such as titanium / titanium nitride or tantalum nitride, and other layers as well. By providing a novel structure in which metal plugs 20 contact a silicide layer 14, which contacts the underlying low bandgap energy material 12, coupled with stress-compensating dielectric layer 16, the contact resistance and stress-induced defects may be reduced, thus improving device performance.

[0037] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

WHAT IS CLAIMED IS:

1. An integrated circuit device comprising:
 - a substrate formed of a first kind of semiconductor having a first energy bandgap;
 - a gate dielectric on said substrate;
 - a gate electrode on said gate dielectric;
 - source and drain regions comprising dopant regions in the substrate on two sides of the gate dielectric and top dopant portions formed of a second kind of semiconductor with a second energy bandgap on said dopant regions, wherein the second energy bandgap is lower than the first energy bandgap;
 - a metal or metal compound on the top dopant portions of the source and drain regions;
 - a first dielectric layer on the metal or metal compound;
 - a second dielectric layer on the first dielectric layer; and
 - a conductive plug contacting the metal and disposed in said first and second dielectric layers.
2. The device of claim 1 wherein said first dielectric layer has inherent compressive stress.
3. The device of claim 1 wherein said first dielectric layer has inherent tensile stress.
4. The device of claim 1 wherein said first dielectric layer comprises a material selected from the group consisting of silicon nitride, silicon oxynitride, silicon oxide, and combinations thereof.

5. The device of claim 1 wherein said substrate comprises a material selected from the group consisting of Si, Ge, compound semiconductor, SOI, strained-Si on relaxed SiGe, SiO₂, oxynitride, nitride, and high-k materials ($k > 8$).
6. The device of claim 1 wherein said top dopant portions of said source and drain regions extends throughout said source and drain regions.
7. The device of claim 1 wherein said top dopant portions of said source and drain regions has a thickness of more than about 50 Å.
8. The device of claim 1 wherein said top dopant portions of said source and drain regions comprises at least two materials selected from the group consisting of Si, Ge, C and combinations thereof.
9. The device of claim 1 wherein said top dopant portions of said source and drain regions contains at least 10 atomic percent Ge.
10. The device of claim 1 wherein said top dopant portions of said source and drain regions contains up to about 4 atomic percent C.
11. The device of claim 1 wherein said source and drain regions have an impurity with doping concentration higher than $2 \times 10^{20} \text{ cm}^{-3}$ and said impurity is selected from the group consisting of B, P, As, In, Sb and combination thereof.

12. The device of claim 1 wherein said metal compound is a metal silicide.
13. The device of claim 12 wherein said metal silicide has a thickness of less than about 300 Å.
14. The device of claim 12 wherein said metal silicide comprises at least two materials selected from the group consisting of N, C and combinations thereof.
15. The device of claim 12 wherein said metal silicide contains between about 1 and about 25 atomic percent Ge.
16. The device of claim 12 wherein said metal silicide is a transition-metal silicide.
17. The device of claim 1 wherein said metal compound comprises two or more transition metals.
18. The device of claim 1 wherein said first dielectric layer comprises at least two materials selected from the group consisting of Si, O, N and combinations thereof.
19. The device of claim 1 wherein said first dielectric layer has a thickness between about 50 Å to about 1000 Å.
20. The device of claim 1 wherein said gate electrode comprises a second semiconductor on said gate dielectric and a second metal on said second semiconductor, and wherein an energy bandgap of said second semiconductor is lower than an energy bandgap of said first semiconductor.

21. The device of claim 20 wherein said second semiconductor contains between about 10 and about 50 atomic percent Ge.
22. The device of claim 20 wherein said gate dielectric comprises a material selected from the group of SiO₂, oxynitride, nitride and combinations thereof.
23. The device of claim 1 wherein said source and drain regions are recessed within said substrate.

24. A method of forming an integrated circuit device, said method comprising:
- forming a gate dielectric on a surface of a substrate, said substrate having a first energy bandgap;
 - forming a gate electrode on said gate dielectric;
 - forming a pair of spacers along opposite sidewalls of said gate electrode and said gate dielectric;
 - forming source and drain regions by forming dopant regions in said substrate on two sides of the gate dielectric and forming top dopant portions formed of a second kind of semiconductor with a second energy bandgap on said dopant regions, wherein said second energy bandgap of said top dopant portions of said source and drain regions is lower than the first energy bandgap of said substrate;
 - forming a metal layer on said source and drain regions;
 - forming a first dielectric on said metal layer;
 - forming a second dielectric layer on said first dielectric layer;
 - forming an opening in said first and second dielectric layers; and
 - forming a conductive plug in said opening.

25. The method of claim 24 comprising epitaxially growing said top dopant portions of source and drain regions on said surface of said substrate on two sides of the gate dielectric, wherein said top dopant portions of said source and drain regions are formed of a second kind of semiconductor.

26. The method of claim 25 wherein said epitaxially growing said top dopant portions of source and drain regions comprises selective epitaxy.

27. The method of claim 26 wherein said selective epitaxy is selected from the group consisting of Molecular Beam Epitaxy (MBE), Ultra High Vacuum Chemical Vapor Deposition (UHVCVD), Atomic Layer Chemical Deposition (ALCVD), Metal Organic Chemical Vapor Deposition (MOCVD), and combinations thereof.

28. The method of claim 26 wherein said selective epitaxy includes forming gases comprising an element selected from the group consisting of Si, Ge, H, Cl, N, He, P, B, As and combinations thereof.

29. The method of claim 26 wherein said selective epitaxy comprises a deposition temperature in the range of about 300-950°C.

30. The method of claim 24 wherein said metal layer is a metal compound comprising two or more transition metals and wherein said forming a metal comprises a method selected from the group consisting of CVD, Physical Vapor Deposition (PVD) and combinations thereof.

31. The method of claim 24 wherein said metal layer is a metal silicide formed by a silicide process.

32. The method of claim 31 wherein said silicide process comprises a method selected from the group consisting of Low Pressure Chemical Vapor Deposition (LPCVD), Plasma Enhanced Chemical Vapor Deposition (PECVD), thermal CVD, laser ablation, ion sputter, e-beam sputter, and combinations thereof.

33. The method of claim 31 wherein said forming said metal layer further comprises:
a first annealing at a temperature higher than about 300°C and at a pressure of less than about 10 Torr in a gaseous ambient comprising elements selected from the group consisting of H, N, He, Ar, Xe and combinations thereof, said first annealing performed after said salicide process.
34. The method of claim 33 further comprising:
selective metal removal by wet etching after said first annealing; and
a second annealing.
35. The method of claim 33 further comprising:
forming a TiN or Ti cap during said first annealing; and
selective metal removal by wet etching.
36. The method of claim 24 wherein the forming of said first dielectric comprises a CVD method selected from the group consisting of LPCVD, PECVD, thermal CVD, and combinations thereof.
37. The method of claim 24 wherein said first dielectric layer is formed with an inherent tensile stress.
38. The method of claim 24 wherein said first dielectric layer is formed with an inherent compressive stress.