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(19)

(54) RASTER STABILIZATION ON CRT DISPLAYS

(71) We, HONEYWELL INFORMATION SYSTEMS INC., a Corporation organised and existing under the Laws of the State of Delaware, United States of America of 200 Smith Street, Waltham, Massachusetts 02154, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement: —

This invention relates to CRT display systems of the type commonly known as VDU's (visual display units). Such a system normally consists of a source of information to be displayed, a CRT, and CRT control circuitry which generates a continuous sequence of rasters, each raster comprising a set of line scans. The raster is generated by digital techniques, so that each line, and a sequence of points along a line, are defined by digital counts. A variety of techniques are available for generating characters to be displayed at predetermined position on the raster lines. The raster is usually of the conventional type consisting of a number of left-to-right line scans, each scan being below the previous one. The beam deflection is normally accomplished by beam deflection circuitry which deflects the beam magnetically.

Magnetic fields other than those of the beam drive circuitry also cause deflection of the electron beam. Stray magnetic fields are commonly produced by the power supply which provides the power for the entire display device. It has been observed that these particular stray fields produce visible distortion on the screen when the frequency of the AC input power to the power supply varies with respect to the raster scan frequency. The information on the screen appears to "swim" thereby giving rise to a dynamic distortion to the viewer.

The object of this invention is to overcome this problem.

Accordingly the present invention provides apparatus, energised from an AC power supply, for generating and controlling a raster on a CRT display, comprising:
a high frequency clock source whose frequency is such that the raster period is slightly less than the period of the power supply;
a series of cascaded cyclic counters fed by the clock source, their counts defining the scans and segments of each scan of the raster;
means responsive to a predetermined combination of counts to stop at least some of the counters from counting; and
means responsive to a predetermined phase instant of the power supply to cause the counters to recommence counting.

A display device embodying the invention will now be described by way of example, with reference to the accompanying drawings, wherein:

Figure 1 is a video display of information on the screen of a computer terminal;

Figure 2 illustrates the formation of a character within the video display of Figure 1;

Figure 3 illustrates the raster scan necessary to accomplish the video display of Figure 1;

Figure 4 is a block diagram of the display logic necessary to form video display of Figure 1;

Figure 5 is a block diagram of the raster scan logic which performs the raster scan of Figure 3;

Figure 6 is a detailed illustration of the power cycle detector appearing in Figures 4 and 5; and

Figure 7 is a further detailed illustration of the raster scan logic of Figure 5.

Figure 1 shows a display screen 10 with various characters displayed on its left-

hand side. On the right of the screen a notional grid is shown, consisting of continuous horizontal zones 12 and vertical zones 14; each character is formed within the rectangle formed by the intersection of a horizontal zone and a vertical zone, giving a total of twenty four (rows) by eighty (columns) character positions. Figure 2 shows a character rectangle in greater detail; each horizontal zone comprises ten horizontal lines 0 to 9, and each line is divided into seven points 0′ to 6′ in each vertical zone. In Figure 2, the character "E" is shown, generated by brightening the CRT beam at appropriate ones of the 7 by 10 points in the rectangle. (To achieve separation between characters, spot brightening only occurs on lines 1 to 7 and points 1′ to 5′).

Figure 3 shows a raster for the entire screen 10; this raster is necessary to form the displayed arrangement of characters in Figure 1. The raster comprises a number of individual rows 16, corresponding to the horizontal zones 12. Each individual row comprises 10 individual horizontal scan paths such as 18. Each individual scan path is accompanied by a retrace path such as 20 which brings the electron beam back to a position for the next horizontal scan from left to right. The next row of characters begins once a retrace path has been completed for the tenth scan path of the previous row of characters; thus the tenth retrace path 22 of the first row 16 brings the electron beam back to a point 24 for the first scan path of the next row 16. This process continues until twenty-four separate rows 16 have been formed on the screen 10. At this time, the electron beam will have traversed a final horizontal scan path 26 in the bottomost row. This final horizontal scan is then repeated until such time as the next cycle of AC input power is detected. The next time the electron beam reaches point 28 at the end of the scan path 26, it is caused to retrace the path 30 back to point 32, where the next succession of horizontal scans begins. The path 30 may be termed the vertical retrace.

Successive rasters must of course occur at a sufficient rate to refresh the information on the screen 10. Further, this rate is locked to the frequency of the power supply. More precisely, the "natural" rate is chosen to be slightly above the highest frequency which the power supply is likely to assume, the power supply frequency varying of course with conditions within predetermined limits. The raster is scanned at its "natural" frequency until the last line 26 is reached, and the raster frequency is then adjusted to match the power supply frequency by repetition of the last scan line 26 as many times as is necessary.

Referring now to Figure 4, a power cycle detector 34 is coupled to a raster scan logic 36 and synchronizes the operations of the raster scan logic 36 to the power supply cycles. The raster scan logic 36 controls the display of information through a video display signal that is applied to a dot pattern generator 38 via a line 39. The dot pattern generator 38 feeds a video generator 40 which in turn energizes an electron beam within a display monitor 42. This results in the successive illumination of various dots on the screen 10, illustrated in Figure 2.

This illumination of dots occurs while the electron beam is being driven in a horizontal direction across the screen 10. This is accomplished within the display monitor 10 by the beam circuitry. This circuitry is responsive to a horizontal drive signal, from the horizontal scan logic 36, on a line 44 which initiates horizontal scans and the horizontal retraces by the electron beam. The raster scan logic disables the dot pattern generator 38 during such retraces, by generating an appropriate video display signal on the line 39.

The raster scan logic also initiates a vertical retrace of the electron beam within the display monitor 42. The vertical retrace is not initiated until the power cycle detector 34 has detected the next power cycle. At this time, the power cycle detector signals the raster scan logic 36 which in turn generates a vertical drive signal on a line 46. This causes the beam drive circuitry within the display monitor 42 to move the electron beam back to the top of the screen. The raster scan logic also disables the dot pattern generator 38 during this vertical retrace. At the end of vertical retrace, the raster scan logic again generates appropriate video display and horizontal drive signals to initiate the next succession of horizontal scans by the display monitor.

With the exception of the power cycle detector 34 and certain other details, this system is conventional.

Figure 5 illustrates the raster scan logic of Figure 4 in further detail. The raster scan logic begins with a high frequency clock source (continuously running oscillator) 48 which drives a scale-of-seven dot counter 50, which defines the seven dot locations that occur for each character in a given horizontal scan. The output of the dot counter 50 clocks a scale-of-112 column counter 52 which generates cyclical column counts of 0 to 111. The cyclical column count is applied to a horizontal scan logic 54, which generates a horizontal drive signal on the line 44 and a horizontal video signal on a line 56. The horizontal

drive signal is applied to the beam deflection circuitry within the display monitor 42 of Figure 4. The horizontal video signal is applied to an AND gate 57, whose output constitutes the video display signal which is applied to the dot pattern generator 38 of Figure 4.

The horizontal scan logic causes the beam deflection circuitry to perform a horizontal retrace during column counts 0 to 31, by generating an appropriate horizontal drive signal on the line 44. The horizontal scan logic also causes the beam deflection circuitry to produce a horizontal scan during the column counts of 32 to 111, by generating another appropriate horizontal drive signal on the line 44. The horizontal scan logic furthermore disables the dot pattern generator during column counts of 0 to 31 and enables it during column counts of 32 to 111, by generating an appropriate horizontal video signal on the line 56 which in turn influences the video display signal occurring at the output of the AND gate 57.

The video output of the horizontal scan logic 54 is also applied to a scale-of-ten scan counter 58 via a line 59. The scan counter 58 incrementally counts the horizonal scans of the electron beam. The scan counter 58 thus defines the ten horizontal scans necessary to complete a given row of characters.

The scan counter 58 signals a scale-of-26 row counter 60 when the tenth scan is occurring, over a line 62. The row counter 60 also receives the horizontal video signal from the horizontal scan logic 54. It will be remembered that the horizontal scan logic 54 defines the length of time in which a horizontal scan is to take place. Thus the horizontal video signal indicates when a given horizontal scan has been completed. The row counter 60 is thus informed of when a tenth scan is occurring, via the line 62, and when it has been completed, via the line 64. The latter increments the row counter to a new row count, so that the row counter 60 is successively incremented from a row count of 0 to a row count of 23, giving the twenty-four rows which are displayed on the screen 10 of Figure 1. It is important to note that the row counter 60 produces an additional two row counts 24 and 25, after the row count of 23 has been reached, for reasons to be discussed below.

The row count from the row counter 60 is applied to a vertical scan logic 66 via a conduit 68. The vertical scan logic 66 also receives the output from the scan counter 58 via a line 70, and suspends any further operations of the horizontal scan logic 54 when a row count of 23 is received along with an output signal from the scan counter 58 indicating that a tenth scan is occurring. This set of signal conditions will occur when the electron beam is completing the tenth scan of the twenty-fourth row. The vertical scan logic signals the horizontal scan logic 54 by a set signal occurring on a line 72.

The horizontal scan logic suspends operations until the power cycle detector 34 detects the beginning of the next power cycle. At this time, the power cycle detector 34 signals the horizontal scan logic to again initiate operations. The signal from the power cycle detector 34 occurs on a line 74 and is applied to the column counter 52 as well as the horizontal scan logic. The horizontal scan logic 54 subsequently increments both the scan counter 58 and the row counter 60. This causes the row count appearing at the output of the row counter 60 to reach a row count of 24. The vertical scan logic 66 is responsive to this row count of 24 to generate a vertical drive signal on the line 46 and a vertical video signal on a line 73. The vertical drive signal initiates the vertical retrace within the display monitor 42. The vertical video signal is applied to the AND gate 57, and the video display signal which is subsequently produced at the output of the AND gate 57 blanks the dot pattern generator during the vertical retrace. The vertical retrace is completed by a row count of 25, which thereby allows the electron beam to begin the uppermost horizontal scan on the screen 10, this horizontal scan having a scan count of 0 and a row count of 0. The electron beam is now again driven through twenty-four rows of ten scans each under the control of the horizontal scan logic 54.

Having now described the overall operation of the raster scan logic, we now turn to the details of the power cycle detector 34, which is shown in Figure 6. A transformer 76 provides an appropriate step-down of the AC input power prior to rectification by a diode bridge 78. The output of the diode bridge 78 is connected in a conventional manner to a power supply 80. The power supply 80 provides appropriate voltage levels throughout the communications terminal.

A band-pass filter 82 is connected to a terminal of the diode bridge 78 so as to receive a half-wave rectification of the stepped-down AC input from the transformer 76. This band-pass filter receives the position half-cycle of the AC input voltage, and filters it to eliminate any noise. The signal occurring at the output of the band-pass filter 82 is a positive half-cycle signal A, which is applied to the negative input of a comparator 84. The output of the comparator 84 is fed back to its positive input via a feedback path

86. The output of the comparator 84 is logically high until a non-zero signal level is detected at the output of the band-pass filter 82. At this time, the output of the differential amplifier 84 switches logically low and is moreover latched in that state by the positive feedback path 86. This logically low signal condition continues until the filtered half-cycle of the band-pass filter 82 returns to zero, when the output of the comparator 84 switches logically high.

The output signal of the comparator 84 is a power signal B occurring on an output line 88; this power signal B will be logically low during the positive half-cycle of the AC input voltage cycle and logically high during the negative half-cycle of the AC input voltage signal.

The power signal B is inverted by an inverter 90 and applied to a trailing edge detection circuit 92, which trailing edge detection circuit 92 generates a narrow negative pulse C on a line 74 on the negative-going edge of the inverted power signal. The pulse signal C thus represents the initial detection of the negative half-cycle of AC input voltage by the comparator 84, and is used by the raster scan logic to initiate raster scans.

Figure 7 shows the power cycle detector 34 together with the raster scan logic of Figure 5 in greater detail. In Figure 7, various counters are shown as blocks. Clock inputs are denoted by vertical arrows, a positive signal transition at one of these clocking inputs causing the counter to incrementally change count. Each counter also contains a load input terminal L. A logically low signal at the load input will cause the counter to load a count of zero when a positive signal transition occurs at the clock input. Some of the counters also include a carry enable terminal C. A logically high signal at the carry enable input enables the counter to incrementally count upon the occurrence of the next positive signal transition at the clocking input. Finally, certain of the counters also have reset inputs R. A logically low signal at the reset input terminal R will cause the count of the counter to be reset to 0.

As has been previously discussed, the raster scan logic includes an oscillator 48 which drives a dot counter 50, which includes a binary counter 100 with output terminals DC1, DC2 and DC4 which go logically high to indicate their respective binary dot counts. The dot count outputs of DC2 and DC4 are applied to a NAND gate 102 which generates a logically low signal to the load input L of the counter 100 upon the occurrence of a dot count of 6. The logically low signal at the load input L causes the counter 100 to load in a dot count of zero upon the next positive signal transition at the clocking input. The counter 100 hence defines a cyclical dot count of 0 to 6. These dot counts are utilized to define the dot locations for a character as has been previously described with regard to Figure 2.

The NAND gate 102 also feeds an inverter 104, which produces a positive signal transition each time a dot count of 6 occurs. This signal is fed to the clocking inputs of a pair of counters 106 and 108, within the column counter 52, which incrementally count the column or character spaces each time a dot count of 6 occurs. The counters 106 and 108 are joined by a carry link 110, the counter 106 providing a logically high carry signal to the carry enable input C of the counter 108 each time the maximum count of 15 occurs. This enables the counter 108, which counts up on the next positive signal transition from the dot counter 50.

The maximum count of the column counters 106 and 108 is limited to 111 by a NAND gate 112 whose output goes logically low at this count. This logically low signal is fed to the load inputs L of the counters 106 and 108 to load them to 0 following count 111.

The counters 106 and 108 each receive the pulse signal C from the power cycle detector 34. This pulse signal is applied to the reset inputs "R" of the counters 106 and 108 to reset them to column count of zero, as will be more fully discussed later.

Turning now to the horizontal scan logic 54, this logic receives certain column count signals from the column counter 52. The column count signal CC64 is applied to a trailing edge detector 114 which generates a narrow-width negative pulse when the signal for column count 64 goes logically low. This occurs when a zero count is loaded into the counter 108 following a column count of 111. The narrow-width negative pulse from the trailing edge detector 114 is applied to an AND gate 116 which also receives the pulse signal C from the power cycle detector 34 via the line 74. As has been previously discussed, a narrow-width negative pulse occurs in the pulse signal C when the power cycle detector detects the next power cycle. Thus both signals applied to the AND gate 116 are normally logically high except for the momentary occurrences of narrow-width negative pulses. The output of the AND gate 116 is therefore normally logically high except for the momentary occurrences of the narrow-width negative pulses.

AND gate 116 feeds a latch circuit 118 comprising a pair of cross-coupled NAND gates 120 and 122. The bottom NAND

gate 122 of the latch 118 receives the negation of column count 32 from CC32 via an inverter 124.

The output of the latch 118, from NAND gate 122, is applied via a line 126 to an NAND gate 128, which is also fed by a flip-flop 130 whose output is normally logically high to enable NAND gate 128 to respond to the output of latch 118. Thus NAND gate 128 acts as an inverter to the output of latch 118. The functions of flip-flop 130 will be discussed later.

The output of NAND gate 128 constitutes the video output of the horizontal scan logic 54. This output produces the horizontal video signal on line 56 which is applied to AND gate 57. NAND gate 128 also feeds an inverter 132 which produces the horizontal drive signal on line 44.

The horizontal video signal is applied to the scan counter 58 via line 59. The signal transition of the horizontal video signal at a column count of 0 increments a four-bit binary counter 134. The outputs SC1, and SC8 of the counter 134 are applied to an NAND gate 136 which signals the negation of scan count 9. This is inverted by an inverter 138 to define scan count 9, which is fed back to the load input L of the counter 134, so that it counts cyclically from scan counts 0 to 9.

The scan counter 58 feeds the J and K inputs of a flip-flop 140 within the row counter 60, and the clocking input of flip-flop 140 receives the horizontal video signal via line 64. The flip-flop 140 follows the signal applied to its J-input upon receipt of a positive signal transition at its clocking input.

It will be evident that under normal conditions, i.e. during the course of a raster, the resetting of the column counter 52 to column count 0 produces a narrow pulse from the trailing edge detector which sets the output of latch 118 low. When column count 32 is reached, signal CC32 is inverted and changes the state of latch 118, its output going high. This output remains high until the column counter 52 counts past column count 111 and is reset again to column count 0. Thus the horizontal video signal is high for column counts 0 to 31 and low for column counts 32 to 111, while the horizontal drive signal is the inverse of this.

The scan counter 58 feeds the row counter 60, which is a scale-of-26 counter. This counter is formed by a flip-flop 140, which forms the lowest order bit position; a 4-bit counter 148, which forms the 2nd to 5th bit positions; and a resetting NAND gate 142, which detects row count 25 and resets the counter to row count 0. The counter is clocked by the horizontal video signals on line 59 in combination with the scan count 9 signal from the scan counter 58.

The vertical scan logic 66 is fed with the binary row count signals RC1 to RC16 and the scan count 9 signal SC9. This vertical scan logic 66 generates a vertical drive signal to cause the electron beam to retrace a substantially vertical path from the bottom to the top of the screen 10. The vertical drive signal is internally produced within the vertical scan logic by an AND gate 154 which receives the binary row count signals RC8 and RC16. The AND gate 154 produces a logically high vertical drive signal for a row count of 24, which causes the display monitor 42 to perform a vertical retrace. This logically high signal remains until the row counter 60 returns to row count 0 following scan count 9 and row count 25. This allows ample time for the vertical retrace to occur within the display monitor 42. The vertical scan logic also produces a vertical video signal, by merely inverting the vertical drive signal by an inverter 155. The vertical video signal is applied to the AND gate 57 via the line 73 to produce a logically low video signal to the dot pattern generator which disables the dot pattern generator during vertical retrace.

The vertical scan logic 66 also produces a set signal on the line 70 which governs the flip-flop 130. This signal is produced by a NAND gate 156 which is fed by inverter 158 and AND gates 160 and 162 as shown, and goes logically low on the combination of row count 23 and scan count 9. This logically low signal constitutes the set signal which is applied to the W-input of flip-flop 130 via line 70.

It will be remembered from the discussion of the power cycle detector 34 in Figure 6 that the power signal B is logically low for the positive half of the AC power cycle. This low power signal B combines with the low set signal from the vertical scan logic to give low signals at both the J and K inputs of flip-flop 130. This causes the output of flip-flop 130 to go low upon the next positive signal transition from the latch circuit 118, which occurs when the tenth horizontal scan of the twenty-fourth row (row count 23 and scan count 9) is completed. Flip-flop 130 thereby goes low and disables NAND gate 128. The disabled NAND gate 128 ceases to produce any positive signal transitions in the horizontal video signal. This in turn disables any further clocking of the scan counter 58 and the row counter 60, so that these maintain a row count of 23 and a scan count of 9.

The power signal B subsequently goes logically high during the next positive

power half cycle, and the narrow-width negative pulse in the power pulse signal C is produced at this time. This narrow-width negative pulse resets flip-flop 130 high which in turn enables NAND gate 128. The narrow-width pulse in the power pulse signal C is also applied via line 74 to the reset inputs of counters 106 and 108 within the column counter 52. This causes these counters to begin counting from a column count of zero. The narrow-width pulse in the power pulse signal C is also applied via line 74 to AND gate 116. This produces a momentary low input signal to latch 118 which sets its output low. Latch 118 is now ready to respond to the next occurrence of column count 32. In this manner, appropriate signal transitions again occur at the output of the latch 118 for column counts of 0 and 32. These transitions are inverted through the NAND gate 128 so as to produce the positive signal transitions in the horizontal video signal at column counts of 0. The positive signal transitions at the zero column counts increment the scan counter 58 and the row counter 60 so as to produce the row counts of 24 and 25 at the output of the row counter 60. The row count of 24 initiates the vertical drive signal which continues through to a row count of 25. As has been previously explained, the row counter 60 is automatically returned to a zero count upon the occurrence of a row count of 25 followed by a scan count of 9. The horizontal scan logic 54 subsequently causes the first horizontal scan to occur for the row count of zero.

WHAT WE CLAIM IS:

1. Apparatus, energized from an AC power supply, for generating and controlling a raster on a CRT display, comprising: a high frequency clock source whose frequency is such that the raster period is slightly less than the period of the power supply:

a series of cascaded cyclic counters fed by the clock source, their counts defining the scans and segments of each scan of the raster;

means responsive to a predetermined combination of counts to stop at least some of the counters from counting; and

means responsive to a predetermined phase instant of the power supply to cause the counters to recommence counting.

2. Apparatus according to claim 1 wherein the predetermined combination of counts is that defining the extreme scan at the end of the raster.

3. Apparatus according to either previous claim wherein the extreme scan is repeated until the predetermined phase instant is detected.

4. Apparatus according to either of claims 2 and 3 wherein the extreme scan is followed by at least one scan effecting a retrace to the extreme scan at the start of the raster.

5. Apparatus according to any previous claim wherein the means responsive to the predetermined phase instant comprise means for half-wave rectifying the power supply and means for detecting when the rectified power supply rises above zero.

6. Display apparatus substantially as herein described with reference to the accompanying drawings.

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