WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a substrate;

a peripheral circuit layer having a transistor provided on the substrate and a first junction metal provided on a first surface; and

a ~~plurality of~~ memory cell array layer~~s that include a~~ provided on the first surface including a stacked structure in which a plurality of electrode layers and a plurality of insulating layers are alternately stacked in the first direction, a columnar structure extending in the first direction in the stacked structure and forming a plurality of memory cells at the intersection with the plurality of electrode layers, a first wiring layer provided between the stacked structure and the first surface, a plug electrically connecting one of the plurality of electrode layers with the first wiring layer and extending in the first direction and a second junction metal provided on the first junction metal and electrically connected with the first wiring layer~~and a second surface opposite to the first surface and do not include a substrate and that include a plurality of memory cells arranged 3-~~

~~dimensionally in a memory cell array region and a surface wiring layer embedded in the first surface or/and the second surface~~,

wherein the second junction metal overlaps the stacked structure when viewed from the first direction~~surface wiring layer of each of the memory cell array layers is formed to overlap the first surface when viewed in a direction vertical to the first surface, and the surface wiring layers are bonded to each other so that the plurality of memory cell array layers are stacked~~.

2. The~~A~~ semiconductor memory device according to claim 1,~~comprising:~~

wherein the first junction metal and the second junction metal ~~a peripheral circuit layer that includes a circuit board, a control circuit formed on a circuit formation surface of the circuit board, and a circuit-side wiring layer formed on the circuit formation surface of the circuit board and electrically connected to the control circuit;~~

~~a first memory cell array layer which includes a first surface and a second surface opposite to the first surface and does not include a first substrate and which includes a~~

~~plurality of first memory cells arranged 3-dimensionally in a memory cell array region, a first signal line extraction electrode, a first external connection electrode formed outside the memory cell array region when viewed in a direction vertical to the first surface, and a first surface wiring layer and a second surface wiring layer connected to the first signal line extraction electrode and the first external connection electrode and formed in the first and second surfaces, respectively, in which the first surface is stacked to face the peripheral circuit layer, and the circuit-side wiring layer and the first surface wiring layer~~ are directly bonded~~; and~~

~~a second memory cell array layer which includes a third surface and a fourth surface opposite to the third surface and does not include a second substrate and which includes a plurality of second memory cells arranged 3-dimensionally in the memory cell array region, a second signal line extraction electrode, a second external connection electrode formed outside the memory cell array region when viewed in a direction vertical to the third surface, and a third surface wiring layer and a fourth surface wiring layer connected to the second signal line extraction electrode and the second external connection~~

~~electrode and formed in the third and fourth surfaces, respectively, in which the third surface is stacked to face the first memory cell array layer, and the second surface wiring layer and the third surface wiring layer are bonded~~.

3. The semiconductor memory device according to claim 1, wherein the memory cell array layer comprises:

a second surface in contact with the first surface and a third surface opposite to the second surface,

a second wiring layer provided between the third surface and the laminate,

a third junction metal provided on the third surface electrically connected to the second wiring layer and overlapping the stacked structure when viewed from the first direction, and

a signal line extraction electrode that electrically connecting the first wiring layer and the second wiring layer and extending in the first direction

~~2,~~

~~wherein the circuit-side wiring layer and the first surface wiring layer are directly bonded and the second surface wiring layer and the third surface wiring layer are directly bonded~~.

4. The semiconductor memory device according to claim ~~2 or~~ 3, further comprising,

~~wherein the plurality of first memory cells include a first stacked body in which a plurality of insulating layers and a plurality of electrode layers are alternately stacked and first columnar portions extending in a stacking direction of the first stacked body,~~ a ~~first~~ bit line ~~is~~ electrically connected to ~~the first columnar portion on a side of the first~~ a second surface side of the columnar structure~~,~~; and a ~~first~~ source line ~~is~~ electrically connected to ~~the first columnar portion on a side of the second~~ a third surface side of the columnar structure, ~~and a first source side~~ wherein the second wiring layer is provided on the third ~~formed to be closer to the side of the second~~ surface side of ~~than~~ the ~~first~~ source line.

~~5. The semiconductor memory device according to any one of claims 2 to 4,~~

~~wherein the plurality of second memory cells include a second stacked body in which a plurality of insulating layers and a plurality of electrode layers are alternately stacked and second columnar portions extending in a~~

~~stacking direction of the second stacked body, a second bit line is electrically connected to the second columnar portion on a side of the third surface, a second source line is electrically connected to the second columnar portion on a side of the fourth surface, and a second source-side wiring layer is formed to be closer to the side of the fourth surface than the second source line.~~

~~6. The semiconductor memory device according to claim 2 or 3,~~

~~wherein the plurality of first memory cells include a first stacked body in which a plurality of insulating layers and a plurality of electrode layers are alternately stacked and first columnar portions extending in a stacking direction of the first stacked body, a first bit line is electrically connected to the first columnar portion on a side of the first surface, a first source line is electrically connected to the first columnar portion on a side of the second surface, and a first source-side wiring layer is formed to be closer to the side of the second surface than the first source line,~~

~~the plurality of second memory cells include a second stacked body in which a plurality of insulating layers and~~

~~a plurality of electrode layers are alternately stacked and second columnar portions extending in a stacking direction of the second stacked body, a second bit line is electrically connected to the second columnar portion on a side of the third surface, a second source line is electrically connected to the second columnar portion on a side of the fourth surface, and a second source-side wiring layer is formed to be closer to the side of the fourth surface than the second source line, and~~

~~the first source-side wiring layer of the first memory cell array layer is connected to the second bit line of the second memory cell array layer inside the memory cell array region when viewed in the direction vertical to the first surface.~~

~~7. The semiconductor memory device according to any one of claims 2 to 6,~~

~~wherein the second surface wiring layer and the third surface wiring layer respectively connected to the first signal line extraction electrode and the second signal line extraction electrode are formed inside the memory cell array region.~~

~~8~~5. The semiconductor memory device according to ~~any one of claims 2 to 7~~claim 3 or claim 4, further comprising:

at least one ~~another~~ other memory cell array layer of the same type as the memory cell array layer ~~that is~~ stacked so as to face the ~~second~~ memory cell array layer, ~~thereby including three or more layers of the~~and having a plurality of memory cell array layers.

~~9~~6. The semiconductor memory device according to ~~any one of claims 2 to 8~~claim 5, further comprising,

~~wherein in the first memory cell array layer or the second memory cell array layer,~~ a memory string ~~that includes~~having ~~a~~ memory cells storing ~~an array layer~~the ID of each of the plurality of memory cell array layers provided in at least one of the plurality of memory cell array layers, ~~and~~ a transistor provided in at least one of the plurality of ~~selecting the first memory cell array layer or the second memory cell array layer as a part of an array layer select circuit is formed, and the memory string is electrically connected to the first signal line extraction electrode of the first memory cell array layer or the second signal line extraction electrode of the second~~ memory cell array layers.

~~10. The semiconductor memory device according to claim 1 or 8,~~

~~wherein in at least one memory cell array layer among the plurality of memory cell array layers, a memory string that includes a memory cell storing an array layer ID and a transistor selecting the memory cell array layer as a part of an array layer select circuit is formed.~~

~~11~~7. The semiconductor memory device according to claim ~~10~~6,

wherein the plurality of memory cell array layers are at least three ~~memory cell array~~or more layers, and the transistor provided in one memory cell array layer between another ~~and a part of the array layer select circuit is formed in~~ one memory cell array layer ~~vertically interposed between~~and one other memory cell array layer~~s among the plurality of memory cell array layers~~.

~~12~~8. The semiconductor memory device according to claim ~~10 or 11~~6,

wherein the transistor is provided in each of the plurality of ~~wherein a part of the array layer select~~

~~circuit is formed for each memory area or memory block of at least one layer of the~~ memory cell array layers.