

- 1 -

SOLENOID VALVE CONTROL CIRCUIT

The present invention relates to a circuit for controlling the operation of a solenoid valve, and more particularly to a solenoid valve control circuit which employs a battery as a power supply.

5 Some washroom faucets have an automatic water supply control unit for automatically supplying water by actuating a faucet solenoid valve when the approach of a user to the faucet is detected, and for automatically stopping the water supply by actuating the solenoid valve again when
10 the leaving of the user from the faucet is detected.

 Generally, such solenoid valve comprises a plunger serving as a valve body and a latching solenoid for driving the plunger when it is energized. As shown in FIG. 4A of the accompanying drawings, it is empirically known that the
15 solenoid valve has a certain characteristic between a power supply voltage V_{cc} applied to the solenoid and the quantity of electricity Q (i.e., all the electric current flowing through the solenoid, hereinafter referred to as an "electric quantity") through the solenoid. When the power
20 supply voltage V_{cc} is low, the electric quantity Q_n which is required by the solenoid to drive the plunger is larger than the electric quantity Q_n that is required by the solenoid to drive the plunger when the voltage V_{cc} is sufficiently high. Stated otherwise, the electric quantity Q_n which is required
25 and sufficient to drive the plunger has to be passed through the solenoid for a relatively long time when the power supply voltage V_{cc} is lower and for a relatively short time when the power supply voltage V_{cc} is higher.

 Where a battery is employed as the power supply for
30 the solenoid valve and the solenoid is to be energized for a constant period of time, a problem arises either when the voltage V_{cc} of the battery is higher because the battery is new or when the voltage V_{cc} of the battery is lower because

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the battery is old or deteriorated. More specifically, if the time for which the solenoid is to be energized is selected to be relatively short in view of new battery conditions, then the solenoid will not be sufficiently energized when the battery voltage V_{cc} becomes lower and the plunger will not be driven to a desired stroke. Conversely, if the time of energization of the solenoid is selected to be relatively long in view of old or deteriorated battery conditions, then the solenoid will be excessively energized when the battery voltage V_{cc} becomes higher, resulting in excessive electric power consumption and a shorter battery service life.

The present invention has been made in view of the aforesaid problems with conventional solenoid valve control circuits.

It is an object of the present invention to provide a solenoid valve control circuit which can energize a solenoid under optimum conditions irrespective of the voltage of a battery applied to the solenoid, so that the electric power from the battery will efficiently be consumed and the service life of the battery will be increased.

To accomplish the above object, there is provided in accordance with the present invention a solenoid valve control circuit for operatively connecting a battery to a solenoid to energize the solenoid to actuate a valve, the control circuit including coulomb controlling means for controllably supplying an electric quantity to the solenoid.

The above and further objects, details and advantages of the present invention will become apparent from the following detailed description of preferred embodiments thereof, given by way of example only, when read in conjunction with the accompanying drawings.

FIG. 1 is a block diagram of a solenoid valve control circuit according to a first embodiment of the present invention;



FIG. 2 is a circuit diagram, partly shown in block form, illustrating the solenoid valve control circuit in greater detail;

FIG. 3 is a timing chart of output signals or operating conditions of circuit elements in the circuit shown in FIG. 2;

FIG. 4A is a graph showing the relationship between a power supply voltage and an electric quantity required by a solenoid;

FIG. 4B is a graph showing the relationship between a voltage produced by dividing the power supply voltage, and a sawtooth voltage;

FIG. 5 is a block diagram of a solenoid valve control circuit according to a first modification;

FIG. 6 is a block diagram showing some of the blocks of FIG. 5 in detail;

FIG. 7 is a block diagram of a solenoid valve control circuit according to a second embodiment of the present invention;

FIG. 8 is a circuit diagram, partly shown in block form, illustrating the solenoid valve control circuit in greater detail;

FIG. 9 is a timing chart of output signals or operating conditions of circuit elements in the circuit shown in FIG. 8;

FIG. 10 is a graph showing voltage characteristics of a general battery;

FIG. 11 is a block diagram of a solenoid valve control circuit according to a second modification;

FIG. 12 is a block diagram showing some of the blocks of FIG. 11 in detail;

FIG. 13 is a block diagram illustrating a decision circuit in the solenoid valve control circuit shown in each of FIGS. 1 and 7;

FIG. 14 is a timing chart of output conditions of circuit elements in the circuit shown in FIG. 13;



FIG. 15 is a block diagram of a portion of a solenoid valve control circuit according to a third modification;

FIG. 16 is a timing chart of output conditions of
5 circuit elements in the circuit shown in FIG. 15;

FIG. 17 is a block diagram of a portion of a solenoid valve control circuit according to a fourth modification;

FIG. 18 is a block diagram of a portion of a
10 solenoid valve control circuit according to a fifth modification; and

FIG. 19 is a block diagram of a portion of a solenoid valve control circuit according to a sixth modification.

15 FIG. 1 shows a solenoid valve control circuit 10 according to a first embodiment of the present invention. The control circuit 10 in its entirety constitutes part of an automatic faucet unit (not shown). The control circuit 10 comprises a valve operation decision circuit 3 for
20 determining valve operation, a voltage monitoring circuit 4 for monitoring a power supply voltage, a coulomb controlling circuit 5 for controlling the electric quantity to be supplied to a latching solenoid 2 of a solenoid valve (not shown), and a drive circuit 6 for driving the solenoid 2.
25 The control circuit 10 controllably drives the latching solenoid 2 with electric power supplied from a battery 1 which is employed as the power supply for the control circuit 10. The solenoid 2 may have either a single winding (in which case the opening or closing of the solenoid valve
30 is determined by the direction in which an electric current flows through the solenoid 2) or double windings (i.e., a winding for opening the solenoid valve and a winding for closing the solenoid valve). The power supply voltage V_{CC} is applied to the decision circuit 3 at all times. The
35 decision circuit 3 is associated with an infrared-radiation



light-emitting diode 3a which is intermittently energized to emit infrared radiation by the battery 1, and a phototransistor 3b which detects reflected light to detect whether a user moves toward or away from the automatic faucet device.

5 Dependent on a detected signal from the phototransistor 3b, the decision circuit 3 applies valve opening/closing signals S1, S2 each of which can selectively take ON and OFF states (i.e., "high" and "low") to the drive circuit 6.

The automatic faucet unit with the control circuit
10 may be incorporated in various devices. Where the automatic faucet unit is assembled in a washroom faucet, both the signals S1, S2 are OFF when no user is present at the faucet. When an approaching user is detected, only the signal S1 is turned ON and the signal S2 remains OFF. As
15 described later on, the signal S1 is turned OFF after the solenoid 2 has been energized with a suitable electric quantity. Thereafter, when the leaving of the user is detected, only the signal S2 is turned ON and the signal S1 remains OFF. After the solenoid 2 has been energized with
20 a suitable electric quantity, the signal S2 is turned off. Therefore, the signal S1 is a solenoid valve opening signal, and the signal S2 is a solenoid valve closing signal. The light-emitting diode 3a and the phototransistor 3b are located at a suitable position near the faucet.

25 The power supply voltage monitoring circuit 4 monitors the voltage Vcc of the battery 1 and applies a signal dependent on the magnitude of the voltage Vcc to the coulomb controlling circuit 5.

When either one of the signals S1, S2 is turned ON,
30 the solenoid valve drive circuit 6 supplies the solenoid 2 with an electric current I of a prescribed polarity to drive a plunger (not shown) serving as a valve body in a given direction. As shown in FIG. 4A, the electric quantity $Q_n = Q_o$ which is required to open the valve is greater than the
35 electric quantity $Q_n = Q_c$ which is required to close the



valve. In each of the opening and closing of the valve, the electric quantity required by the solenoid 2 to drive the plunger when the voltage V_{cc} of the battery 1 is low is greater than the electric quantity required by the solenoid 2 to drive the plunger when the battery voltage V_{cc} is sufficiently high. The horizontal axis of FIG. 4A represents the battery voltage V_{cc} , and the vertical axis the electric quantity Q_n required by the solenoid 2 to drive the plunger. Reference characters E_a , E_b , Q_3 will be described later with reference to FIG. 4A, and reference characters E_0 through E_4 will be described later with reference to FIG. 10.

Generally, the entire electric charge quantity Q (= total electric quantity) passing through the solenoid is expressed by:

$$Q = \int Idt$$

where I is the electric current flowing through the solenoid and t is the time for which the solenoid is energized.

The coulomb controlling circuit 5 applies a detected signal S_3 of a "high" level to the decision circuit 3 when the electric quantity Q supplied to the solenoid 2 reaches a prescribed value (= $Q_n = Q_0$ or Q_c). The solenoid valve opening/closing signals S_1 , S_2 are also supplied to the coulomb controlling circuit 5, which varies output conditions for the detected signal S_3 based on the signals S_1 , S_2 .

In response to the detected signal S_3 from the coulomb controlling circuit 5, the decision circuit 3 turns OFF the one of the signals S_1 , S_2 which is ON at the time, whereupon the drive circuit 6 de-energizes the solenoid 2.

FIG. 2 shows the solenoid valve control circuit 10, particularly the voltage monitoring circuit 4 and the coulomb controlling circuit 5, in detail. The decision circuit 3 comprises a plurality of logic circuits, for example, and each time it detects the approach or leaving of a user, it turns on a power supply switch 7 to apply the power supply voltage V_{cc} to the voltage monitoring circuit 4 and the coulomb controlling circuit 5.



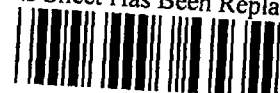
The drive circuit 6 is in the form of a bridge circuit comprising four power transistors, for example. The solenoid 2 is connected between the two output terminals of the bridge circuit. One of the two input terminals of the bridge circuit is connected to the positive terminal of the battery 1, whereas the other input terminal of the bridge circuit is grounded through a resistor. The signals S1, S2 are supplied to a pair of coacting power transistors which form opposite sides of the bridge circuit. While the solenoid 2 is being energized, part of the current I flowing through the solenoid 2 is supplied to a current amplifying circuit 5a of the coulomb controlling circuit 5 (Actually, a voltage signal similar to the solenoid current I is supplied to the amplifying circuit 5a).

The current supplied to the amplifying circuit 5a is supplied as a charging current i through resistors R1, R2 to a monitoring capacitor 5d.

Feedback signals are applied from those terminals of the resistors R1, R2 which are closer to the capacitor 5d to the amplifying circuit 5a through switches 5b, 5c. The switches 5b, 5c are mutually exclusively closed by an output signal from the voltage monitoring signal 4. While only the switch 5b is closed, the current gain of the amplifying circuit 5a is maintained at k1, and while only the switch 5c is closed, the current gain of the amplifying circuit 5a is maintained at k2. k represents a prescribed gain determined by the circuit arrangement, and the current gains k1, k2 are selected such that $k1 = k/R1$ and $k2 = k/(R1 + R2)$, and hence $k1 > k2$. Therefore, as described later on, the average current gain of the amplifying circuit 5a is varied by the closing and opening of the switches 5b, 5c dependent on variations in the power supply voltage Vcc.

The charging current i which flows while only the switch 5b is closed is indicated by:

$$i = k1 \cdot I = (k/R1) \cdot I = k \cdot I/R1.$$



The charging current i which flows while only the switch 5c is closed is indicated by:

$$i = k_2 \cdot I = (k / (R_1 + R_2)) \cdot I = k \cdot I / (R_1 + R_2).$$

When the power supply switch 7 is turned ON, a sawtooth oscillator 4a of the voltage monitoring circuit 4 starts operating to supply a sawtooth voltage V_{sa} as a reference voltage to a comparator 4b. The sawtooth oscillator 4a may be replaced with a triangle generator. When the power supply switch 7 is turned ON, the power supply voltage V_{cc} is divided by resistors R_3 , R_4 , and a divided voltage V_1 is applied to the comparator 4b. The comparator 4b compares the applied voltage V_1 with the reference voltage V_{sa} . While $V_1 > V_{sa}$, the comparator 4b issues an output signal of a "high" level, and while $V_1 < V_{sa}$, the comparator 4b issues an output signal of a "low" level. The output signal from the comparator 4b is applied directly to one of the switches 5b of the coulomb controlling circuit 5 and via an inverter 4e to the other switch 5c. The switches 5b, 5c are closed only when they are supplied with a high-level signal, and hence they are exclusively or alternatively closed. More specifically, while $V_1 > V_{sa}$, the switch 5b is closed and the amplifying circuit 5a has the current gain k_1 , and while $V_1 < V_{sa}$, the switch 5c is closed and the amplifying circuit 5a has the current gain k_2 during which time the charging current i is lower. Denoted at F in FIG. 2 is an input line for closing the valve through a manual override.

As long as the current I flows through the solenoid 2, the capacitor 5d is continuously charged and a voltage V_3 at the input terminal of the capacitor 5d progressively rises. The voltage V_3 is applied as an input voltage to a comparator 5f which is supplied with a reference voltage V_r . While $V_3 < V_r$, the comparator 5f issues an output signal of a "low" level, and when $V_3 > V_r$, the comparator 5f issues an output signal of a "high" level. The high-level signal from the comparator 5f is sent as the de-energizing signal S_3 to



the decision circuit 3. The reference voltage V_r is determined according to the electric quantity Q_n required by the solenoid 2, and thus has different values when the valve is to be opened (i.e., when the signal S_1 is turned ON) and
5 when the valve is to be closed (i.e., when the signal S_2 is turned ON). The reference voltage V_r is selected to be equal to the voltage V_3 across the capacitor 5d when the required electric quantity Q_n ($= Q_o, Q_c$) has flowed through the solenoid 2 in the case where the power supply voltage V_{cc} is
10 sufficiently high. The reference voltage V_r is produced by dividing, with resistors R_5, R_6, R_7 and switches $5h, 5i$, an output voltage from a constant voltage circuit or reference voltage generator 5g to which the power supply voltage V_{cc} is applied through the power supply switch 7. The switches
15 $5h, 5i$ are closed respectively by the signals S_1, S_2 .

As described above with reference to FIG. 4A, the electric quantity Q_n ($= Q_o$) required by the solenoid 2 to open the valve is greater than the electric quantity Q_n ($= Q_c$) required by the solenoid 2 to close the valve.
20 Therefore, when opening the valve, the switch $5h$ is closed by the signal S_1 to supply a relatively high divided voltage V_r as a reference voltage to the comparator 5f. When closing the valve, the switch $5i$ is closed by the signal S_2 to supply a relatively low divided voltage V_r as a reference
25 voltage to the comparator 5f.

Regardless of whether the valve is opened or closed, the voltage V_3 across the capacitor 5d becomes equal to the reference voltage V_r when the electric quantity Q passing through the solenoid 2 reaches the required electric
30 quantity Q_n . At this time, the comparator 5f sends the high-level de-energizing signal S_3 to the decision circuit 3.

At the same time as the decision circuit 3 receives the signal S_3 , it turns OFF the one of the signals S_1, S_2 which
35 is ON at the time, opens the power supply switch 7, and



applies an output signal S4 of a "high" level to a discharging switch 5j. The energization of the solenoid 2 is stopped, the circuits 4, 5 are de-energized, and the capacitor 5d is discharged, readying the control circuit 10 for a next cycle of operation.

As enclosed by the broken lines in FIG. 2, the voltage monitoring circuit 4 is constructed from the circuit elements 4a, 4b and the resistors R3, R4, and the coulomb controlling circuit 5 is constructed from the circuit elements 5a through 5j and the resistors R1, R2, R5, R6, R7.

FIG. 3 shows a timing chart of output signals or operating conditions of the circuit elements illustrated in FIG. 2. Those output signals shown in a lefthand area A in FIG. 3 are produced when the voltage Vcc of the battery 1 is sufficiently high, and those output signals shown in a righthand area B in FIG. 3 are generated when the battery voltage Vcc is lower. FIG. 3 only illustrates the output signals in the areas A, B for opening the valve. The output signals produced for closing the valve are similar and are not shown.

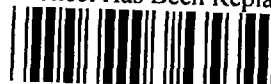
The charts of FIG. 3 represent the following conditions:

(a) The operating condition of the decision circuit 3, i.e., the manner in which the circuit 3 detects the approach of a user.

(b) The length of a processing time required to open the valve.

(c) The opening and closing condition of the power supply switch 7.

(d) The ON/OFF condition of the valve opening signal S1, i.e., the driving condition of the drive circuit 6. The drive circuit 6 is energized about 1 msec. after the power supply switch 7 is closed as shown at (c), and de-energized substantially at the same time that the power supply switch 7 is opened.



(e) The current I flowing through the solenoid 2.

(f) The battery voltage V_{cc} . In the area B, since the internal resistance of the battery 1 is high, the voltage V_{cc} considerably drops when the solenoid 2 is energized.

5 (g) The output voltage V_{sa} from the sawtooth generator 4a. The waveform and peak value of the voltage V_{sa} remain unchanged in the areas A, B.

(h) The output condition of the comparator 4b, which indirectly represents the opening and closing condition of the switch 5b.
10

(i) The opening and closing condition of the switch 5c, which is a reversal of the condition of (h).

With respect to the above charts (f), (g), (h), and (i), while the divided voltage V_1 is higher than the sawtooth voltage V_{sa} , only the switch 5b is closed, and while the
15 divided voltage V_1 is lower than the voltage V_{sa} , only the switch 5c is closed.

(j) The voltage V_3 for charging the capacitor 5d.

(k) The output condition of the comparator 5f, i.e., the output condition of the de-energizing signal S_3 .
20

(l) The time required for the decision circuit 3 to end the energization of the solenoid 2, i.e., the time in which the signal S_4 is rendered "high" in level to close the discharging switch 5j for a time long enough to discharge
25 the capacitor 5d.

In the area A, the switch 5b remains continuously closed since $V_1 > V_{sa}$ at all times. Therefore, while the solenoid 2 is being energized, the charging current $i = k_1 \cdot I$ flows into the capacitor 5d.

30 In the area B, the switches 5b, 5c are exclusively closed based on the magnitude relationship between the sawtooth voltage V_{sa} and the divided voltage V_1 . As described above, the current gain of the amplifying circuit 5a is k_1 when the switch 5b is closed and it is k_2 when the switch 5c
35 is closed. Therefore, the average gain k_{10} of the amplifying circuit 5a in the area B can be determined as follows:

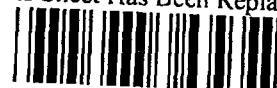


FIG. 4B is a graph showing, at an enlarged scale, the charts (f) and (g) in overlapping relationship in the area B of FIG. 3. The reference characters $V_{sa}(\max)$ and $V_{sa}(\min)$ represent maximum and minimum values of the sawtooth voltage V_{sa} , and τ_0 indicates the cyclic period of the sawtooth voltage V_{sa} . If the period in which $V_1 < V_{sa}$ within one cycle of the voltage V_{sa} is τ ($0 \leq \tau \leq \tau_0$), then the average gain k_{10} of the amplifying circuit 5a can be expressed by:

10
$$k_{10} = (1 - (\tau/\tau_0)) \cdot k_1 + (\tau/\tau_0) \cdot k_2$$

Since $0 \leq \tau \leq \tau_0$ and $k_1 > k_2$ as described above,

$$k_1 \geq k_{10} \geq k_2.$$

Particularly, when $V_1 \geq V_{sa}(\max)$, since $\tau = 0$,

$$k_{10} = k_1.$$

15 When $V_1 \leq V_{sa}(\min)$, since $\tau = \tau_0$,

$$k_{10} = k_2$$

Within the range of $V_{sa}(\min) \leq V_1 \leq V_{sa}(\max)$,

because the period τ is in inverse proportion to the divided voltage V_1 , the average gain k_{10} is proportional to the divided voltage V_1 . In the area B, therefore, the average gain k_{10} is proportional to the power supply voltage V_{cc} , and hence as the voltage V_{cc} is lowered, so is the average gain k_{10} .

When the power supply voltage V_{cc} is relatively high, i.e., in the range of $V_{cc} > E_a$, in FIG. 4A, the electric quantity Q_0 required by the solenoid 2 to open the valve is of a substantially constant value Q_1 . When the power supply voltage V_{cc} is relatively low, i.e., $V_{cc} = E_\beta$, the electric quantity Q_0 required by the solenoid to open the valve is of a value Q_3 . When the power supply voltage V_{cc} is in the range of $E_\beta \leq V_{cc} \leq E_a$, $Q_1 \leq Q_0 \leq Q_3$. The



range $E\beta \leq V_{cc} \leq E\alpha$ corresponds to the area B in FIG. 3.

The control circuit 10 is arranged such that when the power supply voltage V_{cc} is $E\alpha$ and $E\beta$, the divided voltage V_1 is equal to the maximum value $V_{sa}(\max)$ and the minimum value $V_{sa}(\min)$, respectively, of the sawtooth voltage V_{sa} . The values of the resistors R_1 , R_2 , the value of the reference voltage V_r supplied to the comparator 5f, and the capacitance of the capacitor 5d are selected such that when $V_{cc} = E\alpha$, the electric quantity Q supplied to the solenoid 2 is $Q = Q_1$ and when $V_{cc} = E\beta$, $Q = Q_3$. Therefore, $Q = Q_1$ when $V_{cc} > E\alpha$. Since the average gain k_{10} is proportional to the power supply voltage V_{cc} when $E\beta \leq V_{cc} \leq E\alpha$, as described above, the electric quantity Q supplied to the solenoid 2 is controlled so as to be substantially equal to Q_0 in FIG. 4A.

The aforesaid description has been directed to the opening of the valve. For closing the valve, the electric quantity Q supplied to the solenoid 2 in the area B is controlled so as to be equal to Q_c in FIG. 4A since only the reference voltage V_r supplied to the comparator 5f is lower.

As is apparent from the above description, the electric quantity Q supplied to the solenoid 2 is controlled so as to be dependent on the power supply voltage V_{cc} by the solenoid valve drive circuit 10. More specifically, the electric quantity Q is controlled so as to be equal to Q_0 , Q_c shown in FIG. 4A. Therefore, the solenoid 2 is energized in an optimum fashion regardless of whether the battery voltage V_{cc} is high or low. As a consequence, the electric power from the battery 1 is efficiently consumed, and the service life of the battery 1 is prolonged.

FIGS. 5 and 6 show a solenoid valve control circuit according to a first modification of the present invention. Those components in FIGS. 5 and 6 which are identical to those of the control circuit 10 of the first embodiment are denoted by identical reference numerals, and will not be described.



The control circuit 20 has a coulomb controlling circuit 5 comprising an energizing time determining circuit 50, a counter 51, and a switch driving circuit 52. The energizing time determining circuit 50 receives an analog output V1' from the voltage monitoring circuit 4 and determines a time t for which the solenoid 2 is to be energized, based on the analog output V1' and the valve opening/closing signals S1, S2 from the decision circuit 3. The counter 51 counts the determined energizing time t. While the counter 51 is counting the energizing time t, the switch driving circuit 52 closes a switch 60 to energize the solenoid 2. The switch 60 comprises a directional element such as a bridge circuit or the like for energizing the solenoid 2. The analog output V1' from the voltage monitoring circuit 4 is produced by dividing the power supply voltage Vcc at a prescribed ratio.

As shown in FIG. 6, the energizing time determining circuit 50 comprises an A/D converter 50a for converting the analog output V1' from the voltage monitoring circuit 4 into a digital signal V1'', and a memory 50b for determining an energizing time t in response to the digital signal V1'' and the valve opening/closing signals S1, S2. The memory 50b has two memory maps which can be selected by the signals S1, S2, respectively. Each of the memory maps stores data on required energizing times t based on the characteristics of the required electric quantity Qn and the time-base current characteristics of the solenoid 2. The digital signal V1'' is applied as an address signal to the memory 50b to read data on the required energizing time t from the memory map which has been selected by the signal S1 or S2.

The electric quantity Q supplied to the solenoid valve 2 can be controlled so as to be of a magnitude dependent on the power supply voltage Vcc by the solenoid valve control circuit 20. Accordingly, the solenoid 2 is energized in an optimum fashion regardless of whether the



battery voltage V_{cc} is high or low. As a consequence, the electric power from the battery 1 is efficiently consumed, and the service life of the battery 1 is prolonged.

The circuit components 50, 51 of the control circuit 20 may be replaced with a PWM (Pulse Width Modulation) circuit responsive to the output from the power supply voltage monitoring circuit for producing pulses of a duration inversely proportional to the power supply voltage V_{cc} , and an output signal from the PWM circuit may be supplied to the switch driving circuit 52. In this case, the PWM circuit doubles as a timer circuit. Thus, a pulse generator with the pulse duration variable by the output from the power supply voltage monitoring circuit may be used as a timer.

A solenoid valve control circuit 100 according to a second embodiment of the present invention will be described below with reference to FIGS. 7 through 9. Those parts in FIGS. 7 through 9 which are identical to those of the control circuit 10 of the first embodiment are designated by identical reference numerals, and will not be described in detail.

The control circuit 100 differs from the control circuit 10 of the first embodiment in that it lacks the power supply voltage monitoring circuit 4, the switches 5b, 5c, and the resistors R_1 , R_2 of the control circuit 10. Instead, the current gain of the current amplifying circuit 5a is set to a value k_3 . While the solenoid 2 is being energized, a charging current i ($= k_3 \cdot I$) flowing through a resistor R_{11} is supplied to the capacitor 5d at all times.

FIG. 9 is a timing chart showing output signals or operating conditions of the circuit elements in the control circuit 100. The charts (a) through (f) and (j) through (l) in FIG. 9 indicate the same conditions as those in FIG. 3. It is assumed that the power supply voltage V_{cc} varies in a relatively high range in the area A, and in a relatively low range in the area B.



As shown in FIG. 9, the solenoid 2 is energized for a time Ta' in the area A, and for a time Tb' in the area B. The electric quantity Q supplied to the solenoid 2 is indicated by the areas of sector-shaped portions Qa , Qb in the chart (e) in the areas A, B.

It is now assumed that the valve is to be opened.

When the voltage $V3$ across the capacitor 5d is equal to the reference voltage Vr , the de-energizing signal $S3$ is issued. Assuming that the capacitor 5d has a capacitance C , the charge q stored in the capacitor 5d is of a constant value qr which is given by:

$$qr (C \cdot V3) = C \cdot Vr \quad \dots(1)$$

In the area A, the following equation is established:

$$qr = \int_0^{Ta'} i dt \quad \dots(2)$$

Since $i = k3 \cdot I$ as described above, the equation (2) can be modified as follows:

$$qr = \int_0^{Ta'} k3 \cdot I dt = k3 \cdot \int_0^{Ta'} I dt \quad \dots(3)$$

Inasmuch as $\int_0^{Ta'} I dt$ represents the electric quantity Q supplied to the solenoid 2 in the area A, the following is obtained from the equation (3):

$$qr = k3 \cdot Qa \quad \dots(4)$$

The equation (4) can be modified into:

$$Qa = qr/k3 \quad \dots(5)$$

Likewise, in the area B,

$$qr = \int_0^{Tb'} i dt \quad \dots(6)$$

Since $i = k3 \cdot I$ as described above, the equation (6) can be modified as follows:



$$q_r = \int_0^{T_b'} k_3 \cdot I dt = k_3 \cdot \int_0^{T_b'} I dt \quad \dots (7)$$

Inasmuch as $\int_0^{T_b'} I dt$ represents the electric quan-

tity Q supplied to the solenoid 2 in the area B, the following is obtained from the equation (7):

5 $q_r = k_3 \cdot Q_b \quad \dots (8)$

The equation (8) can be modified into:

$$Q_b = q_r / k_3 \quad \dots (9)$$

In the control circuit 100, the reference voltage V_r supplied to the comparator 5f when the drive signal S_1 is
10 turned ON, is set to a prescribed value $V_r = k_3 \cdot Q_{10} / C$. The value Q_{10} may be the same as the value Q_1 in FIG. 4A.

Since

$$q_r = C \cdot V_r \quad \dots (1)$$

as described above,

15 $q_r = C \cdot (k_3 \cdot Q_{10} / C) = k_3 \cdot Q_{10} \quad \dots (10)$

By putting the equation (10) into the equations (5) and (6), the following equations can be obtained:

$$Q_b = Q_{10} \quad \dots (11)$$

$$Q_a = Q_{10} \quad \dots (12)$$

20 From the equations (11), (12) results the following:

$$Q_a = Q_b = Q_{10} \quad \dots (13)$$

The electric quantities Q_a , Q_b supplied to the solenoid 2 in the respective areas A, B are equal to each
25 other, and to the value Q_{10} . With $Q_{10} = Q_1$, the electric quantities Q_a , Q_b are equal to Q_1 .

According to the control circuit 100, therefore, the electric quantity Q supplied to the solenoid 2 is controlled at the constant value Q_{10} irrespective of variations
30 in the power supply voltage V_{cc} .

This also holds true for closing the valve. When closing the valve, the reference voltage V_r is set to $V_r =$



k3·Q20/C. Q20 may be set so as to be equal to Q2 in FIG. 4A.

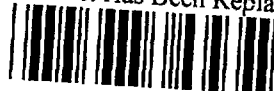
With the control circuit 100, accordingly, the constant electric quantity is always supplied to the solenoid
5 regardless of irregularities in the power supply voltage. As a result, the electric power of the battery is efficiently consumed and the battery has a prolonged service life.

FIG. 10 shows voltage characteristics of a general
10 lithium battery. The horizontal axis of the graph of FIG. 10 represents the amount of electric power of the battery which is consumed with time, and the vertical axis represents the voltage E of the battery when there is a load connected to the battery. As shown, the voltage E of the
15 lithium battery has an initial value E_0 when not in use, and as the stored electric energy is consumed, the battery voltage is gradually lowered stably in the range of $E_2 > E > E_3$. When the voltage E is further lowered to a lower limit E_4 as a result of continued energy consumption, the battery can no
20 longer be used as a power supply. The above characteristics are similar to those of other batteries such as an alkaline battery. The reference character E_1 indicates an electromotive force in the battery.

Referring back to FIG. 4A, the above voltage range
25 of $E_2 > E > E_3$ is very narrow, and the electric quantity Q_n ($= Q_0, Q_c$) required by the solenoid 2 has a substantially constant value (Q_1, Q_2) in this voltage range. It is assumed that the power supply voltage V_{cc} represents the battery voltage E ($V_{cc} = E$).

30 By controlling the electric quantity Q supplied to the solenoid 2 so as to be of a value (Q_1, Q_2) within the above range of $E_2 > E > E_3$ in FIG. 4A, the solenoid 2 can be energized optimally in most of the period of time in which the battery is used.

35 By setting the value Q_{10} in the control circuit 100 to $Q_{10} = Q_1$, the electric quantity Q supplied to the sole-



noid 2 can be controlled so as to be the required electric quantity Q_n ($= Q_1$) even if the power supply voltage V_{cc} varies in the range ($E_2 > E > E_3$).

The above operation remains the same when the valve
5 is closed. By setting the value Q_{20} to $Q_{20} = Q_2$, the electric quantity Q supplied to the solenoid 2 can be controlled so as to be the required electric quantity Q_n ($= Q_2$) even if the power supply voltage V_{cc} varies in the range ($E_2 > E > E_3$).

10 Where the values Q_{10} , Q_{20} in the control circuit 100 are thus established, the solenoid 2 can be energized optimally in most of the period of time in which the battery is used. The electric energy stored in the battery 1 is thus efficiently consumed, and the service life of the bat-
15 tery 1 is prolonged.

FIGS. 11 and 12 illustrate a solenoid valve control circuit 200 according to a second modification of the present invention. Those parts in FIGS. 11 and 12 which are identical to those of the control device 20 of the first
20 modification are denoted by identical reference numerals, and will not be described in detail.

The control circuit 200 has a coulomb controlling circuit 5 comprising an energizing time determining circuit 50, a counter 51, and a switch driving circuit 52. The
25 energizing time determining circuit 50 determines a time t for which the solenoid 2 is to be energized, based on the valve opening/closing signals S_1 , S_2 from the decision circuit 3. The circuit elements 52, 60 are equivalent to the drive circuit 6 shown in FIG. 1.

30 As shown in FIG. 12, the energizing time determining circuit 50 comprises a memory 50a for determining an energizing time t in response to the valve opening/closing signals supplied thereto. The memory 50a has two data which can be selected by the signals S_1 , S_2 , respectively. These
35 data represent values of the time t required to supply a



prescribed electric quantity, e.g., the required electric quantity Q_n ($= Q_1, Q_2$) in the range of $E_2 > E > E_3$ in FIG. 4A, to the solenoid. The time data selected from the memory 50a by the signal S1 or S2 is sent to the counter 51.

5 According to the solenoid valve control circuit 200, the electric quantity Q supplied to the solenoid valve 2 is controlled at a prescribed magnitude ($Q_n = Q_1, Q_2$) dependent on the power supply voltage V_{cc} in most of the period of time in which the battery is used. As a
10 consequence, the solenoid 2 is energized optimally in most of the period of time of use of the battery. The electric energy stored in the battery 1 is efficiently consumed and the service life of the battery 1 is thus prolonged through a simple and inexpensive circuit arrangement.

15 The control circuit 200 is advantageous over the control circuit 20 shown in FIGS. 5 and 6 in that it requires no power supply voltage monitoring circuit and no A/D converter, and that the size of the memory 50a used is small.

20 The memory 50a and the counter 51 may be replaced with a timer circuit which receives the valve opening/closing signals S1, S2 and issues an energizing time t for directly obtaining a prescribed electric quantity to be supplied to the solenoid.

25 For a simpler circuit arrangement, the pulse generating times produced in response to the valve opening/closing signals S1, S2 may be equal to each other to equalize the electric quantities for opening and closing the valve.

FIG. 13 shows one detailed circuit arrangement for
30 the decision circuit 3, and FIG. 14 is a timing chart showing output conditions of circuit components in the circuit 3.

The circuit 3 normally generates the valve opening/closing signals S1, S2 based on signals S01, S02 which serve
35 as origins of the signals S1, S2. The signals S01, S02 have



waveforms as shown in the charts (d) in FIGS. 3 and 9. When the de-energizing signal S3 is generated, these signals S01, S02 are changed to a "low" level by a non-illustrated logic circuit.

5 If no de-energizing signal S3 is produced due for example to a failure of the coulomb controlling circuit 5 even when the signal S1 or S2 is generated, then the circuit 3 temporarily stops the issuance of the signals S1, S2. Thereafter, the circuit 3 produces the signals S1, S2 again.
10 If a de-energizing signal S3 is still not produced even by the regenerated signals S1, S2, the circuit 3 forcibly closes the valve and stops its controlling operation on the solenoid 2.

 More specifically, the origin signals S01, S02 go
15 high in level when the approach/leaving of a user is detected. The origin signals S01, S02 are applied respectively to D input terminals of F/F (flip-flop) circuits 301, 302 which serve as latch circuits. The signals S01, S02 are also applied to an OR gate 303, the output signal of which
20 is applied to a CLK input terminal of the F/Fs 301, 302. Therefore, when either one of the origin signals S01, S02 goes high, both the F/Fs 301, 302 are operated, and a high-level output signal is issued from the Q output terminal of one of the F/Fs to which the high-level signal has
25 been applied. Specifically, when the signal S01 goes high, the high-level output signal is issued only from the Q terminal of the F/F 301. When the signal S02 goes high, the high-level output signal is issued only from the Q terminal of the F/F 302. The output condition of the Q terminals of
30 the F/Fs 301, 302 is latched until the signals S01, S02 go high again after they have gone low. The F/Fs 301, 302 are thus triggered by positive-going edges of the signals applied to their CLK input terminals.

 The signals S01, S02 are also applied to an OR gate
35 304, the output of which is applied to a START terminal of a



timer 305. Therefore, the output signal from the OR gate 304 goes high when at least one of the signals S01, S02 goes high, starting the timer 305. The output signal from the timer 305 is normally low in level. When the timer 305 reaches a time-out condition after it has counted the output signal from the OR gate 304 for a prescribed period of time, the timer 305 continuously issues a signal To of a high level. When a retry signal Re of a high level from a retry commander 306 is applied to a RESET terminal of the timer 305 under this condition, the output signal from the timer 305 goes low and starts counting the output signal from the OR gate 304. Times for which the timer 305 counts the input signal in response to signals applied to the START and RESET terminals thereof are equal to each other. These counting times are selected to be longer than the energizing time Tb shown in FIG. 3 at (j).

The output signal from the timer 305 which is normally low is applied to input terminals of AND gates 307, 308 through an inverter 309 to enable the AND gates 307, 308. The other input terminals of the AND gates 307, 308 are supplied with the output signals from the F/Fs 301, 302. The de-energizing signal S3 is applied to the STOP terminals of the timer 305 and the retry commander 306 for stopping the operation of the timer 305 and the retry commander 306. Therefore, insofar as the de-energizing signal S3 is normally generated, the timer 305 does not produce a high-level output signal. Normally, the output signals from the AND gates 307, 308 are thus equal to the origin signals S01, S02, respectively.

The high-level time-out signal To from the timer 305 is applied to the retry commander 306. Simultaneously in response to the time-out signal To, the retry commander 306 applies the high-level retry signal Re to the RESET terminal of the timer 305 and an input terminal of an AND gate 310. The output terminal of the AND gate 310 thus issues a



failure signal Tr of a high level only when the timer 305 issues the time-out signal To after the retry signal Re has been issued. The retry command 306 may comprise a latch circuit.

5 The output signal from the AND gate 310 is supplied through an inverter 313 to an input terminal of an AND gate 311 and directly to an input terminal of an OR gate 312. The other input terminals of the AND gate 311 and the OR gate 312 are supplied with the signals S01, S02 from the AND
10 gates 307, 308, respectively. Since the output signal from the AND gate 310 is low in level under normal condition, the output signal from the AND gate 311 is equal to the signals S01, S02 under normal condition.

 The output signal from the AND gate 310 is sent to
15 a trouble display circuit 314. When the failure signal Tr is issued from the AND gate 310, the trouble display circuit 314 indicates a failure condition through a pilot lamp or the like to show that the control circuit is suffering a failure somewhere therein.

20 The output signal from the AND gate 310 is also applied to a START terminal of a timer 317. The timer 317 normally continues to issue a low-level output signal. When the high-level failure signal Tr is applied to the START terminal of the timer 317, the timer 317 counts a prescribed
25 period of time, and then continuously issues an output inhibit signal In of a high level. The time interval which is counted by the timer 317 is selected to be longer than the time counted by the timer 305.

 The output signal from the timer 317 is applied via
30 an inverter 318 to input terminals of AND gates 315, 316, the other input terminals of which are supplied with the output signals from the AND gate 311 and the OR gate 312. Normally, the output signal from the timer 317 is low in level, and the output signals from the AND gates 315, 316
35 are the same as the origin signals S01, S02, respectively,



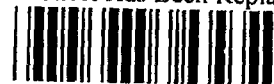
under normal condition. The output signals from the AND gates 315, 316 are supplied as the valve opening/closing signals S1, S2 to the coulomb controlling circuit 5 and the solenoid valve drive circuit 6, respectively.

5 Operation of the control circuit 3 shown in FIG. 13 will hereinafter be described with reference to FIG. 14. The timing chart of FIG. 14 shows the output conditions of the circuit elements indicated by the corresponding reference characters, and illustrates a failure condition of the
10 control circuit 3 due to trouble of the coulomb controlling circuit 5, for example. As described above, the origin signals S01, S02 are generated by the non-illustrated logic circuit. Indicated at 316, S2(Tr) is a valve closing override signal produced by the failure signal Tr, and indicates
15 that the signal functions in the same manner as the signal S2. Denoted at St in FIG. 14 is a time at which the timers 305, 317 start counting time.

When either the origin signal S01 or S02 goes high in level, the corresponding one of the valve opening/closing
20 signals S1, S2 goes high, starting to energize the solenoid 2. At the same time, the START terminal of the timer 305 is supplied with a high-level signal through the OR gate 304 to start counting a prescribed period of time ($> T_b$).

Normally, the de-energizing signal S3 is generated
25 before the timer 305 reaches a time-out condition, the origin signals S01, S02 go low, and the timer 305 and the retry commander 306 stop their operation. These conditions are illustrated in FIG. 14.

In the event that no de-energizing signal S3 is
30 produced upon elapse of the energizing time, e.g., T_b , for some reason, the timer 305 reaches a time-out condition. The timer 305 continuously issues a high-level time-out signal To. Therefore, one of the input terminals of each of the AND gates 307, 308 is supplied with a low-level signal
35 from the inverter 309, with the result that the output sig-



nals from the AND gates 307, 308 go low again. The conditions of the origin signals S01, S02 are maintained by the Q output signals from the F/Fs 301, 302.

5 The time-out signal To is sent to the retry commander 306 to enable the latter to issue a retry signal Re after it has closed the discharging switch 5j for a prescribed period of time with a delay circuit (not shown). The retry signal Re is applied to the RESET terminal of the timer 305, which then issues a low-level signal and restarts counting a prescribed period of time (T_b). Since the output signal from the timer 305 goes low, the AND gates 307, 308 are enabled again to issue the condition of the origin signals S01, S02 which are held in the F/Fs 301, 302. While the retry signal Re is also applied to the AND gate 310, the output signal from the timer 305 remains low. The signals from the AND gates 307, 308 are finally issued as the valve opening/closing signals S1, S2 from the AND gates 315, 316, respectively. This condition is indicated by a second "high" state of the chart represented by (307, 308) S1, S2 in FIG. 14, i.e., a retry condition.

20 After the signals S1, S2 have been issued again, the origin signals S01, S02 go low if the de-energizing signal S3 is produced before the time-out condition of the timer 305, and the operation of the timer 305 and the retry commander 306 is stopped. This condition is not illustrated in FIG. 14.

30 If no de-energizing signal S3 is produced upon elapse of the energizing time, e.g., T_b , for some reason, then the timer 305 reaches a time-out condition. The timer 305 continues to issues a high-level time-out signal To again. Therefore, the output signals from the AND gates 307, 308 go low, thus inhibiting the transmission of the origin signals S01, S02 past the AND gates 307, 308. As a result, the output of the valve opening/closing signals S1, S2 is inhibited.



Since the retry signal Re is maintained at the high level at this time, the high-level failure signal Tr is issued from the AND gate 310.

5 The failure signal Tr is sent to the trouble display circuit 314, which then continuously indicates the failure condition.

10 The failure signal Tr is also applied to the START terminal of the timer 317 to enable the latter to start counting a prescribed period of time. Since the output signal from the timer 317 is low until it reaches a time-out condition, a high-level signal is applied to one input terminal of the AND gate 316 to enable the latter.

15 The failure signal Tr is also fed to the OR gate 312. Therefore, the output signal from the OR gate 312 goes high, and is issued as the valve closing signal S2 (Tr) caused by the failure signal Tr. The solenoid valve drive circuit 6 closes the valve in response to the signal S2 (Tr).

20 When the timer 317 has completed the counting of the prescribed time, it issues a high-level output inhibit signal In to disable the AND gates 315, 316, so that the issuance of the valve closing signal S2 (Tr) is inhibited. The timer 317 subsequently continues to issue the output inhibit signal In to inhibit the issuance of the valve opening/closing signals S1, S2.

25 Even after the forced closing of the valve with the override signal S2 (Tr) has been brought to an end, the failure signal Tr and the output inhibit signal In are maintained to inhibit the solenoid 2 from being energized and to indicate the failure.

30 With the aforesaid arrangement of the decision circuit 3, any wasteful consumption of the electric energy stored in the battery, which would otherwise be caused by some failure of the control circuit, can be avoided. Even
35 if no de-energizing signal S3 is obtained within a pre-



scribed period of time, the valve opening/closing signals S1, S2 are automatically rendered low, thus effectively preventing a reverse latching phenomenon in which if the energizing time is long, the valve which has once been opened is
5 closed again because of solenoid characteristics exhibited when closing the solenoid.

Since the circuit 3 informs the operator of a failure condition, the operator can immediately find such a failure of the control circuit. In addition, the valve is
10 forcibly closed when the circuit 3 determines that the control circuit suffers a failure. Accordingly, the control circuit is associated with an effective fail-safe system.

The circuit 3 does not regard a single time-out condition of the timer 305 as a failure, but tries to energize the solenoid again through the retry commander 306
15 should such a time-out condition occur. This prevents the control circuit from being de-energized by a single extrinsic error which may be caused by noise or the like.

A solenoid valve control circuit 400 according to a
20 third modification will be described with reference to FIGS. 15 and 16. Circuit elements 401, 402, 403, 404 illustrated in FIG. 15 are added to the control circuit 10 or 100, described above for detecting a drop in the battery voltage Vcc.

25 A voltage produced by dividing the output voltage from the reference voltage generator 5g at a prescribed ratio is applied as a reference voltage Th to a comparator 401, the reference voltage Th providing a threshold value. The battery voltage Vcc is divided into an input voltage Vcc' which is applied to the comparator 401. When the input
30 voltage Vcc' is higher than the threshold voltage Th, the comparator 401 issues a high-level signal to one input terminal of an AND gate 403 through an inverter 402.

The valve opening/closing signals S1, S2 are
35 applied to an OR gate 404, the output signal of which is





- 28 -

applied to the other input terminal of the AND gate 403. Thus, while either the signal S1 or S2 is high in level, the AND gate 403 is enabled to issue an output signal. That is, the AND gate 403 can issue an output signal only when the
5 solenoid 2 is energized.

If the voltage V_{cc} drops lower than the threshold voltage T_h while either the signal S1 or S2 is high and the solenoid 2 is being energized, the output signal from the comparator 401 goes low. The low-level signal from the com-
10 parator 401 is applied through an inverter 402 as a high-level signal to the AND gate 403. Consequently, the AND gate 403 issues a signal S5 of a high level which represents that the battery voltage V_{cc} drops lower than a prescribed voltage level.

15 FIG. 16 shows the output condition of the voltage drop signal S5. The voltage drop signal S5 is delivered to a non-illustrated circuit so as to be processed thereby in a predetermined manner.

For example, the signal S5 is sent to a latch cir-
20 cuit (not shown) which produces an output signal to enable a liquid crystal display, for example, to display the reduction in the battery voltage.

The signal S5 may be employed to perform the same function as the failure signal T_r shown in FIGS. 13 and 14.

25 A drop in the battery voltage V_{cc} when there is no load on the battery can be detected even by dispensing with the OR gate 404 and the AND gate 403. It is in practice preferable, however, to detect any drop in the voltage V_{cc} when the battery is loaded by energizing the solenoid 2 as
30 illustrated. While only one threshold T_h is employed in the above modification, two threshold values may be established, with the higher threshold value used for warning the operator about a voltage drop and the lower threshold value for de-energizing the entire control system.

35 FIG. 17 illustrates a solenoid valve control circuit 500 according to a fourth modification of the present

invention. Circuit components 501, 502, 503 shown in FIG. 17 are added to the control circuit 10 or 100 for determining that the battery is used up when the solenoid 2 is energized a number of times in excess of a predetermined number.

5 The solenoid opening/closing signals S1, S2 are applied to an OR gate 501, the output signal of which is applied to a counter 502 to count the number of times which the solenoid 2 is energized. The count is then applied as a digital signal to a digital comparator 503.

10 A reference count applied to the digital comparator 503 is set to a prescribed value (= an integer) through a jumper switch J. The reference count is selected to be a number of times the solenoid 2 is energized to use up the electric energy stored in the battery. The digital comparator 503 issues an output signal S6 of a high level when the
15 count exceeds the reference count.

 The signal S6 is a signal which statistically or indirectly represents that the battery voltage Vcc drops below a prescribed value. The voltage drop signal S6 is
20 sent to a certain circuit (not shown) so as to be processed thereby. The signal S6 is practically equivalent to the voltage drop signal S5 described above, and the manner of utilizing the signal S6 is also the same as the manner of utilizing the signal S5.

25 A solenoid valve control circuit 600 in accordance with a fifth modification of the present invention is shown in FIG. 18. Circuit elements 401, 402, 403, 404 (or 501), 502, 503 shown in FIG. 18 are added to the control circuit 10 or 100. Those circuit elements in FIG. 18 which are
30 identical to those of the control circuits 400 and 500 will not be described below.

 The control circuit 600 simultaneously performs the functions of the control circuits 400, 500. However, the signals S5, S6 are applied to an OR gate 601, which produces
35 an output signal S7 of a high level when the signal S5 or S6



goes high. The signal S7 is applied a certain circuit and processed thereby.

The signal S7 is produced when the solenoid 2 has been energized a number of times in excess of a predetermined number or when the battery voltage Vcc drops below a prescribed value. By using the signal S7 as a battery consumption signal, the battery can reliably be replaced with a new one before the battery power is completely used up.

FIG. 19 shows a solenoid valve control circuit 700 according to a sixth modification of the present invention.

The control circuit 700 includes a solenoid valve drive circuit 6 in the form of a bridge circuit, and a capacitor 701 connected parallel to the drive circuit 6. The capacitor 701 has a relatively large capacitance C1 for supplying the solenoid 2 with an electric current which is large enough to open the valve.

Under normal condition, the valve opening/closing signals S1, S2 are low in level, rendering the drive circuit 6 nonconductive. At this time, the capacitor 701 is charged to a voltage equal to the battery voltage Vcc at the time there is no load on the battery. Therefore, the capacitor 701 is charged to $C1 \cdot Vcc$.

When the approach of a user is detected and the valve opening signal S1 goes high, for example, the drive circuit 6 is rendered conductive. Under this condition, a current flows mainly from the capacitor 701 into the drive circuit 6. Upon elapse of a prescribed period of time in which the electric quantity Q supplied to the solenoid 2 should reach a predetermined value, the signal S1 goes low, making the drive circuit 6 nonconductive. Thereafter, the capacitor 701 is gradually charged in readiness for a next cycle of energization of the solenoid 2.

While the signal S1 is high in level and the solenoid 2 is being energized, the battery voltage Vcc does not largely drop.



While the above valve is opened in the above description, the solenoid 2 is also energized mainly by the capacitor 701 for closing the valve.

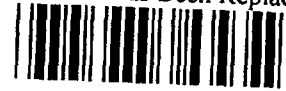
In the control circuit 700, the solenoid 2 is energized mainly by the capacitor 701. Therefore, even if the battery voltage V_{cc} when the battery is loaded is considerably lowered at the end of the service life of the battery, the solenoid 2 is supplied with the same electric quantity as that which is available at the beginning of the battery service life. As a result, the electric energy stored in the battery can fully be utilized without being wasted.

The aforesaid modifications of the invention may be combined in various combinations.

Although there have been described what are at present considered to be the preferred embodiments of the present invention, it will be understood that the invention may be embodied in other specific forms without departing from the essential characteristics thereof. The present embodiments are therefore to be considered in all aspects as illustrative, and not restrictive. The scope of the invention is indicated by the appended claims rather than by the foregoing description.

This Sheet Has Been Replaced





Claims:

- 32 -

1. A solenoid valve control circuit [10; 20; 100; 200; 400; 500; 600; 700] for operatively connecting a battery [1] to a solenoid [2] to energize the solenoid to actuate a valve, said control circuit including coulomb controlling means [4, 5; 5] for supplying a controllable electric charge quantity [Qn; Q10] to the solenoid [2].

2. A solenoid valve control circuit [10; 20; 200] according to claim 1, wherein said electric quantity [Qn] is a required electric quantity [Qn] corresponding to the voltage [Vcc] of said battery [1],

said coulomb controlling means [4, 5] comprising means for supplying said required electric quantity [Qn] to said solenoid [2].

3. A solenoid valve control circuit [10] according to claim 2, further comprising:

a decision circuit [3] for producing an energizing signal [S1, S2] indicating that said battery [1] is to be connected to said solenoid [2] under a prescribed condition; and

a solenoid valve drive circuit [6] responsive to said energizing signal [S1, S2] for operatively connecting said battery [1] to said solenoid [2] to energize said solenoid [2], and





wherein said coulomb controlling means [4, 5] comprises:

a power supply voltage monitoring circuit [4] for monitoring the voltage [Vcc] of said battery [1] and producing a signal [f; g] corresponding to the battery voltage [Vcc]; and

a coulomb controlling circuit [5] for monitoring the electric quantity [Q, V3] supplied from said battery [1] to said solenoid [2] and for producing a de-energizing signal [S3] based on the signal [f; g] from said power supply voltage monitoring circuit [4] when the electric quantity [Q] supplied to said solenoid [2] is equal to said required electric quantity [Qn] corresponding to said battery voltage [Vcc].

15 4. A solenoid valve control circuit [10] according to claim 3, wherein said coulomb controlling circuit [5] comprises:

an amplifying circuit [5a, 5b, 5c, R1, R2] connected to said solenoid [2] for amplifying an electric current [I] to be supplied to the solenoid [2];

a capacitor [5d] chargeable to a prescribed charge level [C·V3] in response to the amplified current [k1·I, k2·I] from said amplifying circuit [5a, 5b, 5c, R1, R2]; and

a comparator [5f] for comparing a voltage [V3] across said capacitor [5d] with a reference voltage [Vr] and





- 34 -

producing said de-energizing signal [S3] when the voltage [V3] across said capacitor [5d] is equal to said reference voltage [Vr]; and

5 said amplifying circuit [5a] being responsive to said signal [f; g] corresponding to the battery voltage from said power supply voltage monitoring circuit [4] for amplifying said electric current to be supplied to said solenoid [2] at a gain [k10] proportional to said battery voltage [Vcc].

10 5. A solenoid valve control circuit [10] according to claim 3, wherein said amplifying circuit [5a, 5b, 5c, R1, R2] amplifies said electric current [I] at a constant gain [k1] when said battery voltage [Vcc] is relatively high,

15 said reference voltage [Vr] of said comparator [5f] being set to be equal to the voltage [V3] across said capacitor [5d] when said required electric quantity [Qn = Q1, Q2] is supplied to said solenoid [2] in case said battery voltage [Vcc] is relatively high.

20 6. A solenoid valve control circuit [10] according to claim 3, wherein said de-energizing signal [S3] from said coulomb controlling circuit [5] is supplied to said decision circuit [3], said decision circuit [3] being responsive to said de-energizing signal [S3] for stopping the generation of said energizing signal [S1, S2].





7. A solenoid valve control circuit [20] according to claim 1, further comprising:

a decision circuit [3] for producing an energizing signal [S1, S2] indicating that said battery [1] is to be
5 connected to said solenoid [2] under a prescribed condition, and

wherein said coulomb controlling means [4, 5, 60] comprises:

a power supply voltage monitoring circuit [4] for
10 monitoring the voltage [Vcc] of said battery [1] and producing a signal [V1'] corresponding to the battery voltage [Vcc];

an energizing time decision circuit [50] for determining an energizing time [t] in which said solenoid [2] is
15 to be energized, in response to said energizing signal [S1, S2] from said decision circuit [3] and said signal [V1'] corresponding to said battery voltage from said power supply voltage monitoring circuit [4]; and

a drive circuit [51, 52, 60] for connecting said
20 battery [1] to said solenoid [2] to energize said solenoid [2] for said determined energizing time [t].

8. A solenoid valve control circuit [100; 200] according to claim 1, wherein said electric quantity [Q10, Q20] is an electric quantity [Q10, Q20] having a constant
25 value; and





- 36 -

said coulomb controlling means [5] having means for supplying said constant-value electric quantity [Q10, Q20] to said solenoid [2].

9. A solenoid valve control circuit [100] according to claim 8, further comprising:

a decision circuit [3] for producing an energizing signal [S1, S2] indicating that said battery [1] is to be connected to said solenoid [2] under a prescribed condition, and

10 a solenoid valve drive circuit [6] responsive to said energizing signal [S1, S2] for operatively connecting said battery [1] to said solenoid [2] to energize said solenoid [2], and

wherein said coulomb controlling means [5] comprises:

a coulomb controlling circuit [5] for monitoring the electric quantity [Q, V3] supplied from said battery [1] to said solenoid [2] and for producing a de-energizing signal [S3] when the electric quantity [Q] supplied to said solenoid [2] is equal to said constant-value electric quantity [Q10, Q20].

10. A solenoid valve control circuit [100] according to claim 9, wherein said coulomb controlling circuit [5] comprises:



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- 37 -

an amplifying circuit [5a, R11] connected to said solenoid [2] for amplifying an electric current [I] to be supplied to the solenoid [2] at a prescribed gain [k3];

5 a capacitor [5d] chargeable to a prescribed charge level [C·V3] in response to the amplified current [k3·I] from said amplifying circuit [5a, R11]; and

10 a comparator [5f] for comparing a voltage [V3] across said capacitor [5d] with a reference voltage [Vr] and producing said de-energizing signal [S3] when the voltage [V3] across said capacitor [5d] is equal to said reference voltage [Vr].

11. A solenoid valve control circuit [100] according to claim 10, wherein said constant-value electric quantity [Q10, Q20] is an electric quantity [Qn = Q1, Q2] required by said solenoid [2] when the voltage [Vcc] of said battery [1] is of a stable value [E2 > E > E3], and

15 said reference voltage [Vr] of said comparator [5f] is equal to the voltage [V3] across said capacitor [5d] when said required electric quantity [Qn = Q1, Q2] is supplied to said solenoid [2].

12. A solenoid valve control circuit [100] according to claim 9, wherein said de-energizing signal [S3] from said coulomb controlling circuit [5] is supplied to said decision circuit [3], said decision circuit [3] being



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- 38 -

responsive to said de-energizing signal [S3] for stopping the generation of said energizing signal [S1, S2].

13. A solenoid valve control circuit [200] according to claim 1, further comprising:

5 a decision circuit [3] for producing an energizing signal [S1, S2] indicating that said battery [1] is to be connected to said solenoid [2] under a prescribed condition, and

wherein said coulomb controlling means [5, 60] comprises:

10 an energizing time decision circuit [50] for determining an energizing time [t] in which said solenoid [2] is to be energized, in response to said energizing signal [S1, S2] from said decision circuit [3]; and

15 a drive circuit [51, 52, 60] for connecting said battery [1] to said solenoid [2] to energize said solenoid [2] for said determined energizing time [t].

14. A solenoid valve control circuit [FIG. 13] according to claim 3 or 9, wherein said decision circuit [3] comprises a timer circuit [305] for producing a time-out signal [To] to stop the generation of said energizing signal [S1, S2] when said de-energizing signal [S3] is not produced upon elapse of a predetermined period of time [$> T_b$] after said energizing signal [S1, S2] has been produced.



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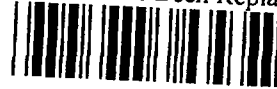
15. A solenoid valve control circuit [FIG. 13] according to claim 14, wherein said decision circuit [3] further comprises a retry commander [306] for producing a retry signal [Re] to generate said energizing signal [S1, S2] once more when said time-out signal [To] is produced by said timer circuit [305].

16. A solenoid valve control circuit [FIG. 13] according to claim 15, wherein said decision circuit [3] further comprises a failure determining circuit [310 ~ 318] for producing a failure signal [Tr] to stop controlling said solenoid [2] when said de-energizing signal [S3] is not produced upon elapse of a predetermined period of time [$> T_b$] after said energizing signal [S1, S2] has been produced again based on said retry signal [Re].

17. A solenoid valve control circuit [FIG. 13] according to claim 16, wherein said failure determining circuit [310 ~ 318] comprises a valve closing override circuit [312, 316 ~ 318] for forcibly closing said valve, and a trouble display circuit [314] for indicating a failure condition.

18. A solenoid valve control circuit [FIG. 13] according to claim 3 or 9, wherein said decision circuit [3] further comprises a failure determining circuit [304 ~ 318]





for producing a failure signal [Tr] to stop controlling said solenoid [2] when said de-energizing signal [S3] is not produced upon elapse of a predetermined period of time after said energizing signal [S1, S2] has been produced.

5 19. A solenoid valve control circuit [400] according to claim 1, further comprising:

 a voltage drop detecting circuit [401, 402, 403, 404] for detecting a drop in the voltage [Vcc] of said battery [1] below a predetermined value [Th] and for producing
10 a voltage drop signal [S5] indicative of the detected voltage drop.

 20. A solenoid valve control circuit [500] according to claim 1, further comprising a counting circuit [501, 502, 503] for detecting that the number of times said solenoid [2] is energized by said battery [1] exceeds a predetermined number and for producing a voltage drop signal [S5]
15 indicative of the detected number of times.

 21. A solenoid valve control circuit [600] according to claim 1, further comprising:

20 a voltage drop detecting circuit [401, 402, 403, 404] for detecting a drop in the voltage [Vcc] of said battery [1] below a predetermined value [Th] and for producing a first voltage drop signal [S5] indicative of the detected voltage drop; and



a counting circuit [501, 502, 503] for detecting that the number of times said solenoid [2] is energized by said battery [1] exceeds a predetermined number and for producing a second voltage drop signal [S5] indicative of the
5 detected number of times.

22. A solenoid valve control circuit [700] according to claim 1, further comprising:

a capacitor [701] chargeable to a charge level [C1·Vcc] by said battery [1] while said solenoid [2] is not
10 being energized by said battery [1], said solenoid [2] being supplied with an electric current from said capacitor [701] when said solenoid [2] is energized.

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ABSTRACT

Solenoid valve control circuit

A solenoid valve control circuit [10] for operatively connecting a battery [1] to a solenoid [2] to energize the solenoid to actuate a valve has a coulomb controlling circuit [5] for supplying a controllable electric charge quantity to the solenoid [2].

[Fig.1]

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FIG. 1

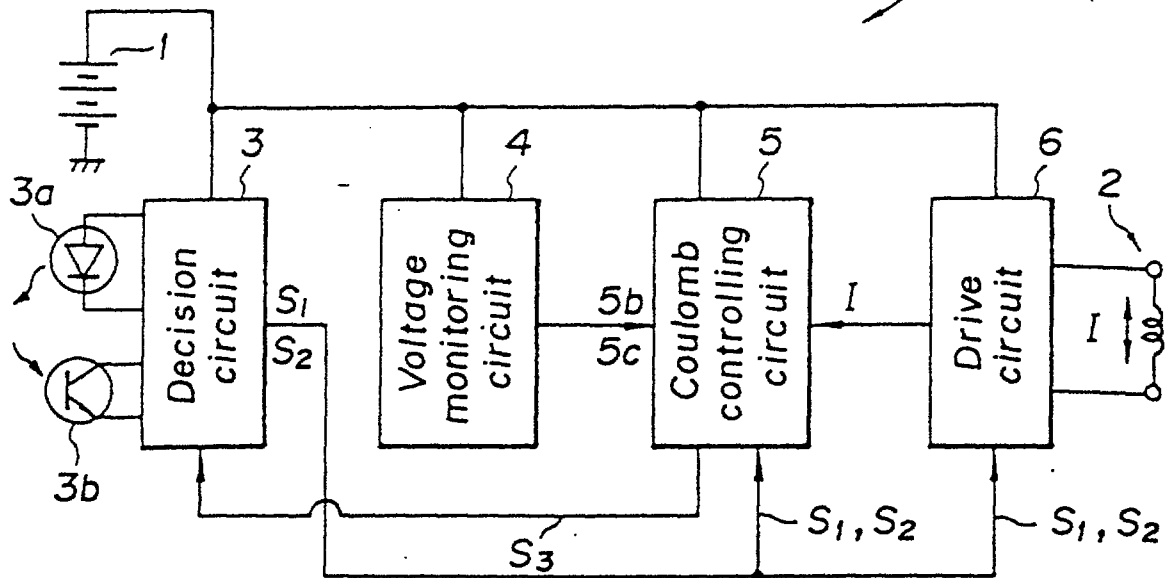


FIG. 4A

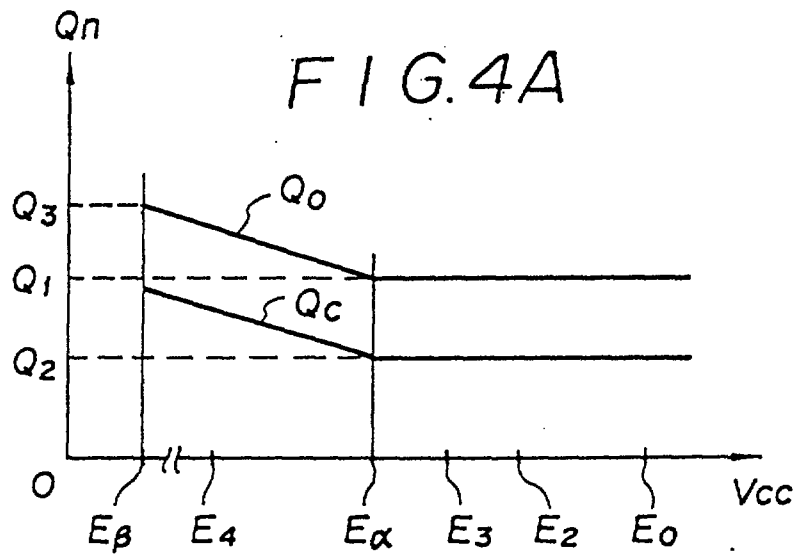


FIG. 4B

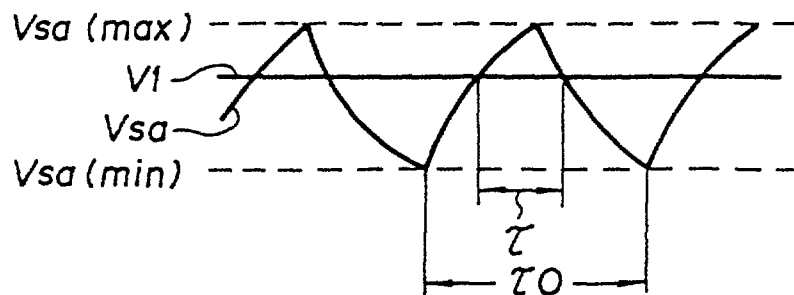
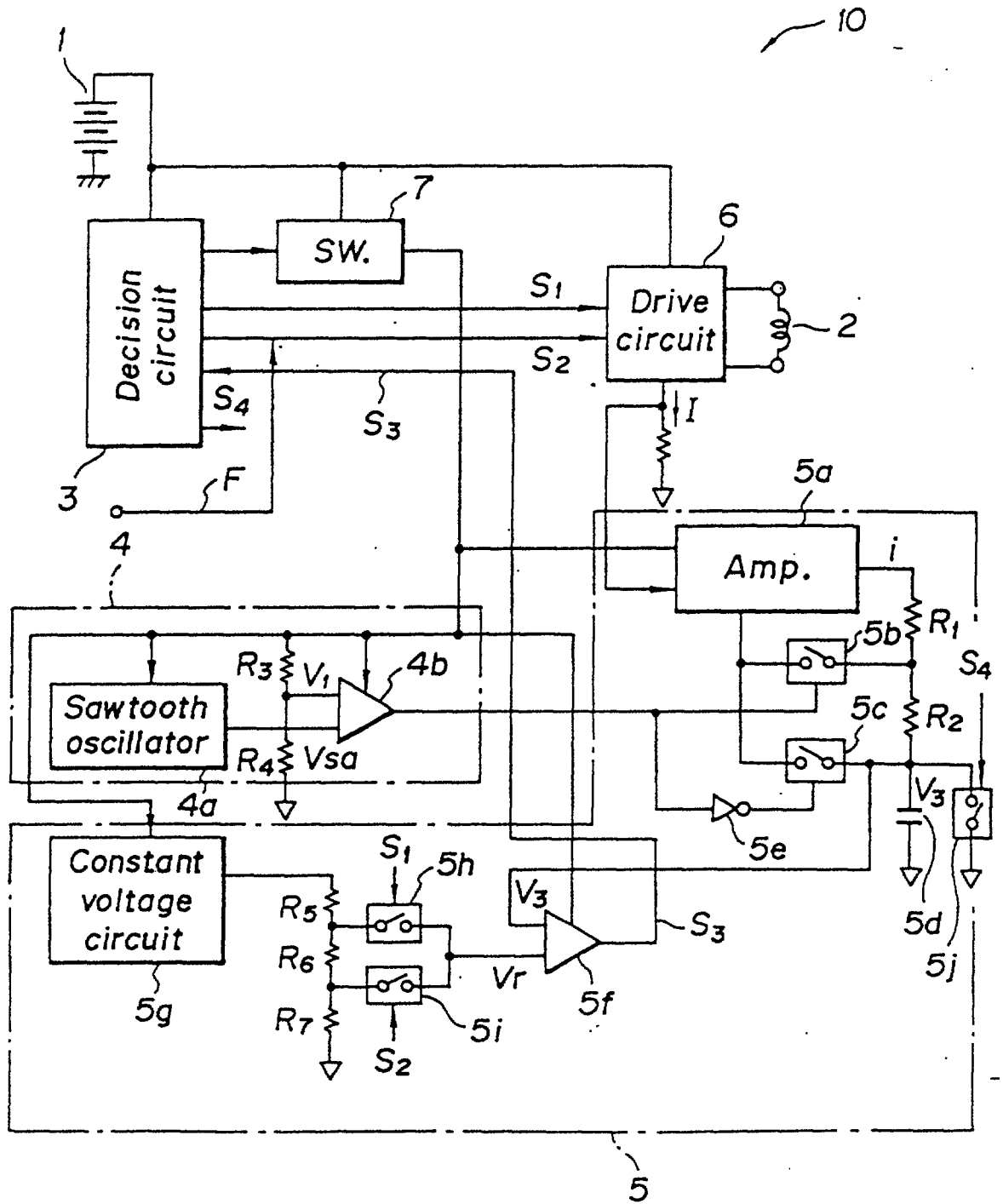


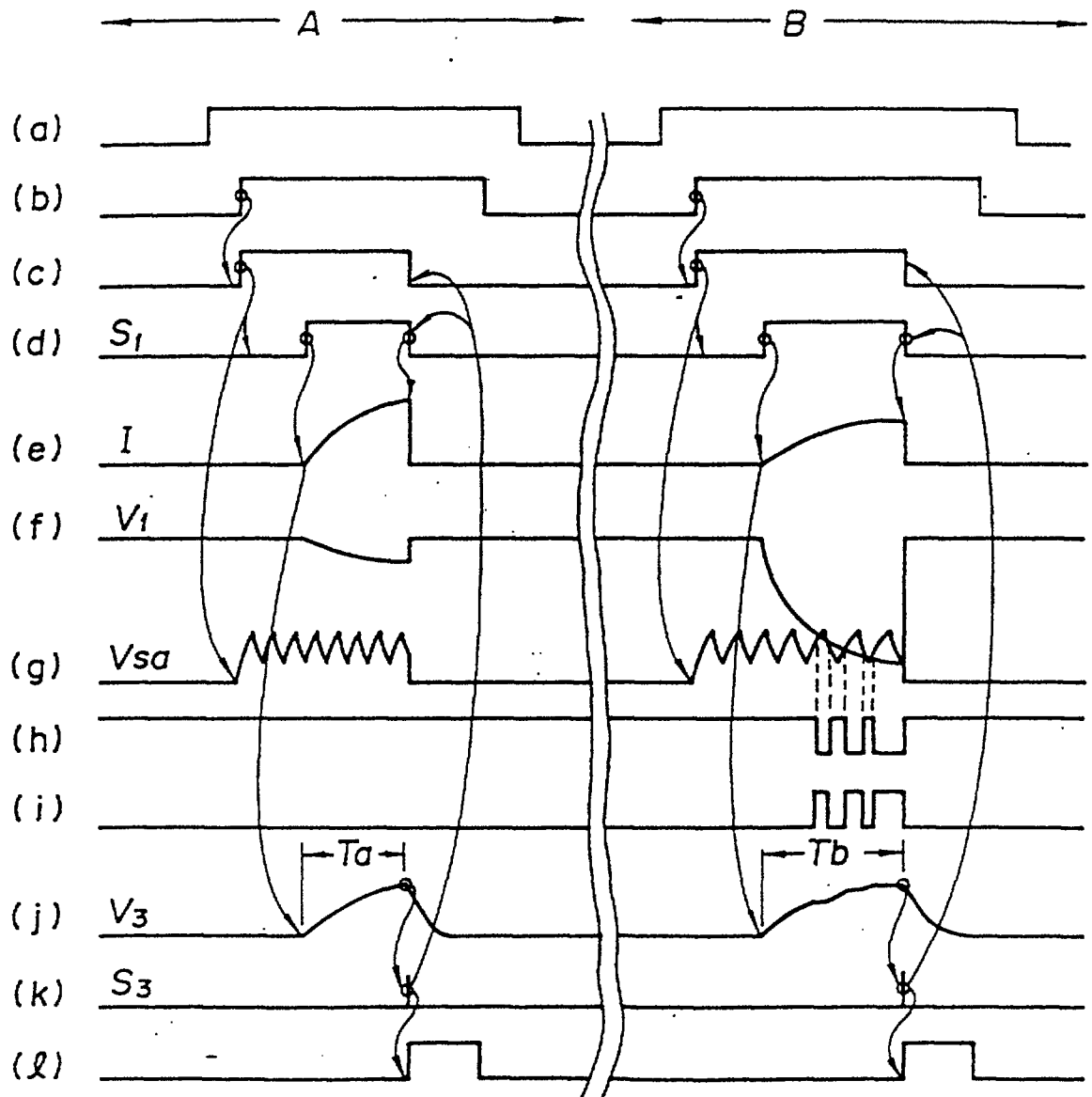
FIG. 2



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FIG. 3



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FIG. 5

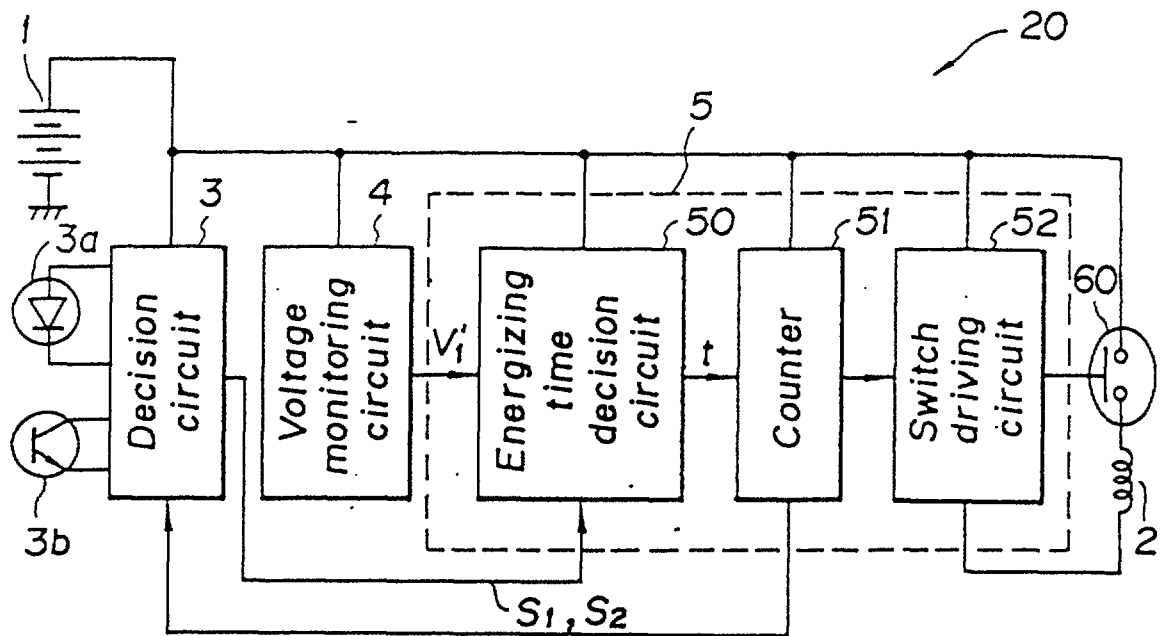
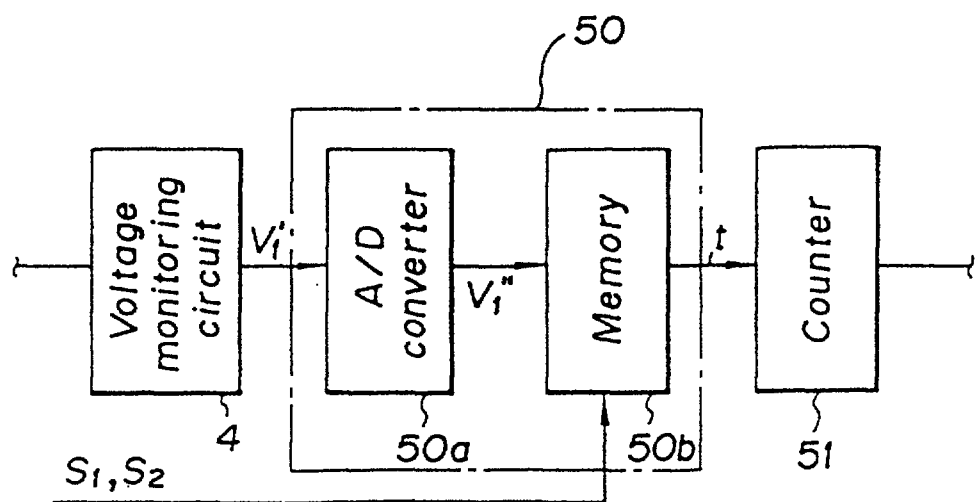


FIG. 6



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FIG. 7

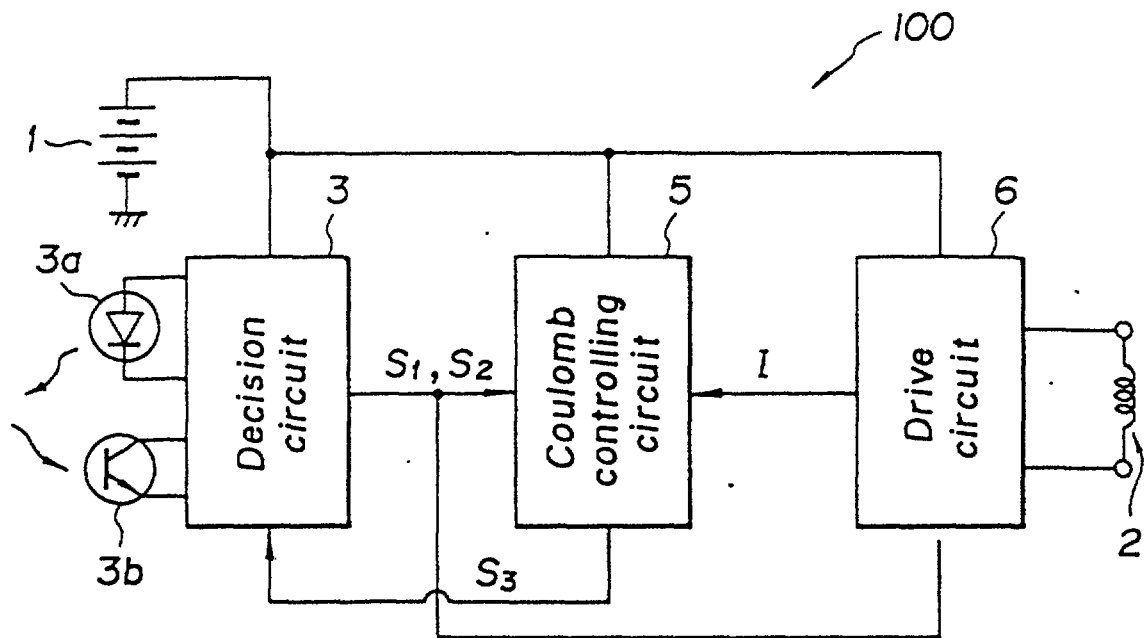
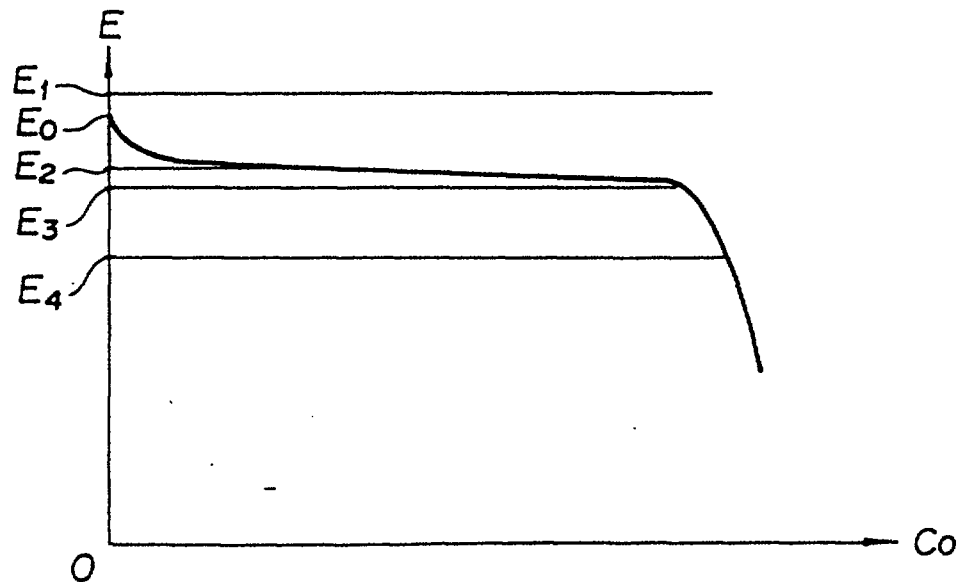


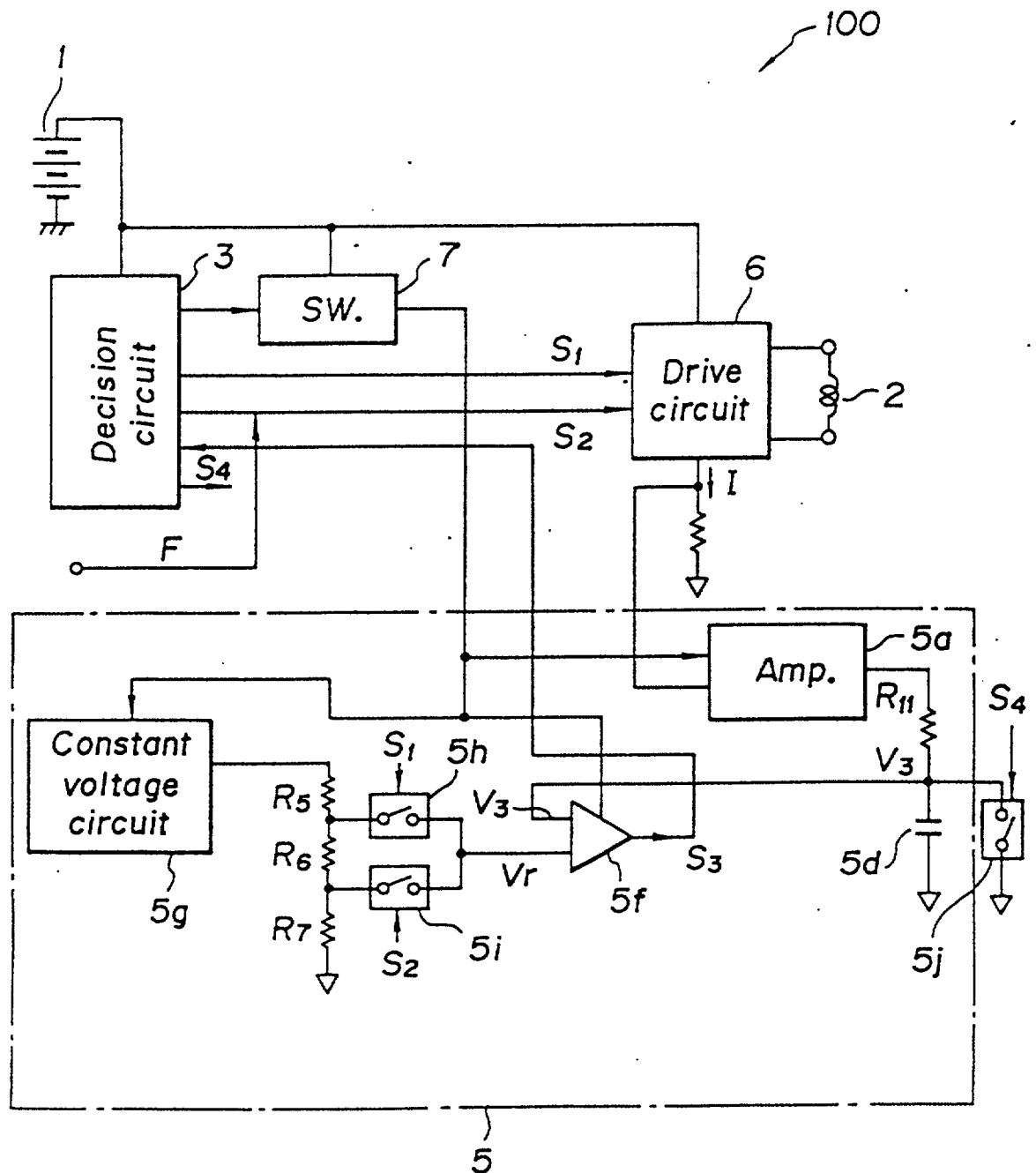
FIG. 10



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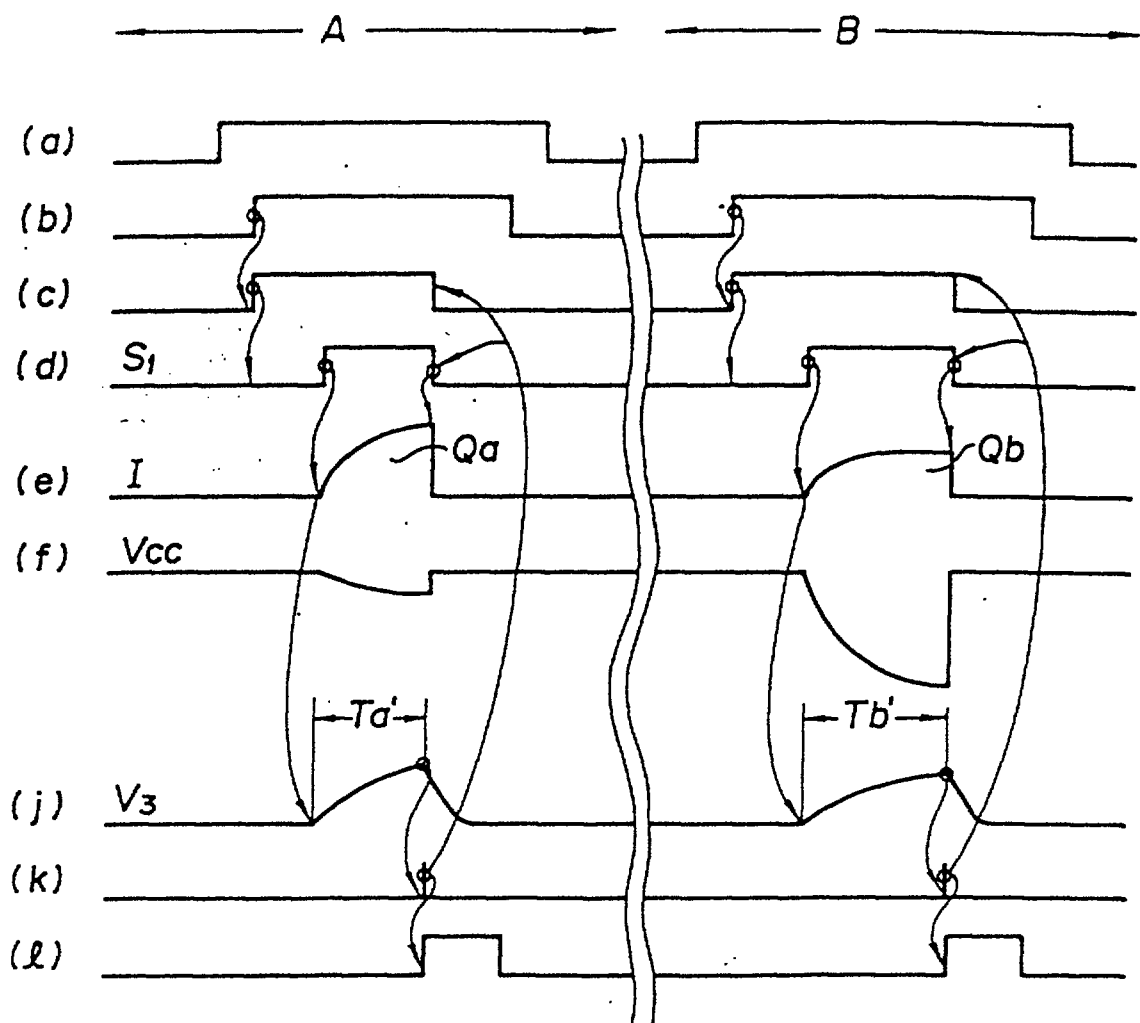
FIG. 8



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FIG. 9



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FIG. 11

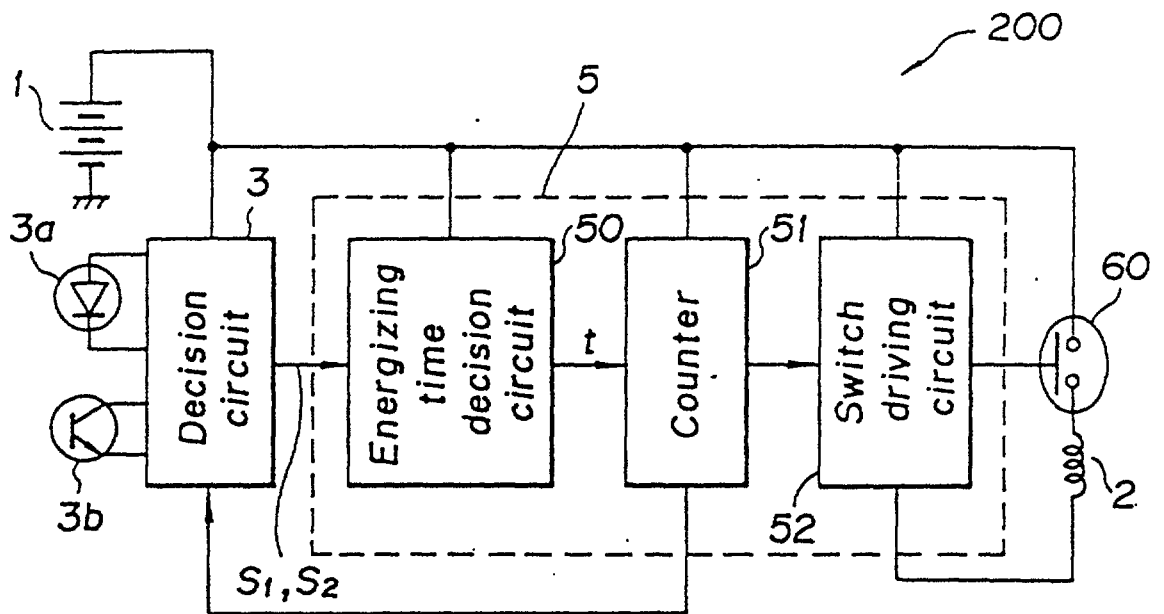
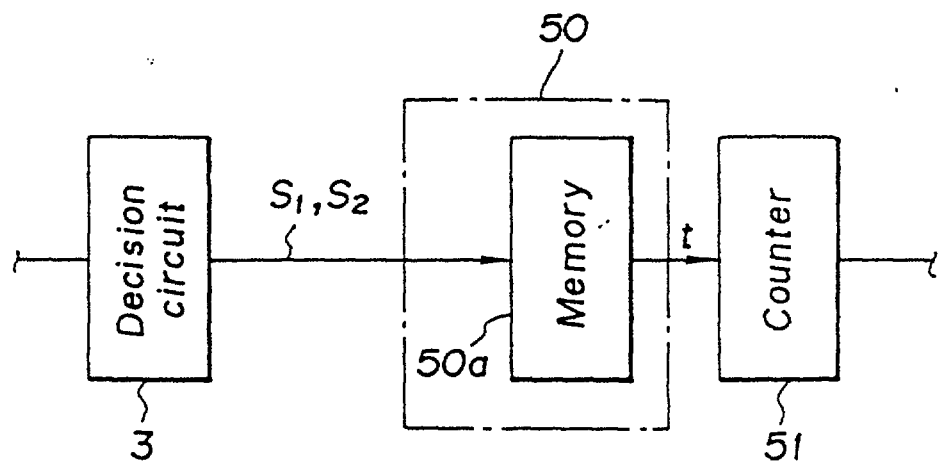


FIG. 12



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F I G. 13

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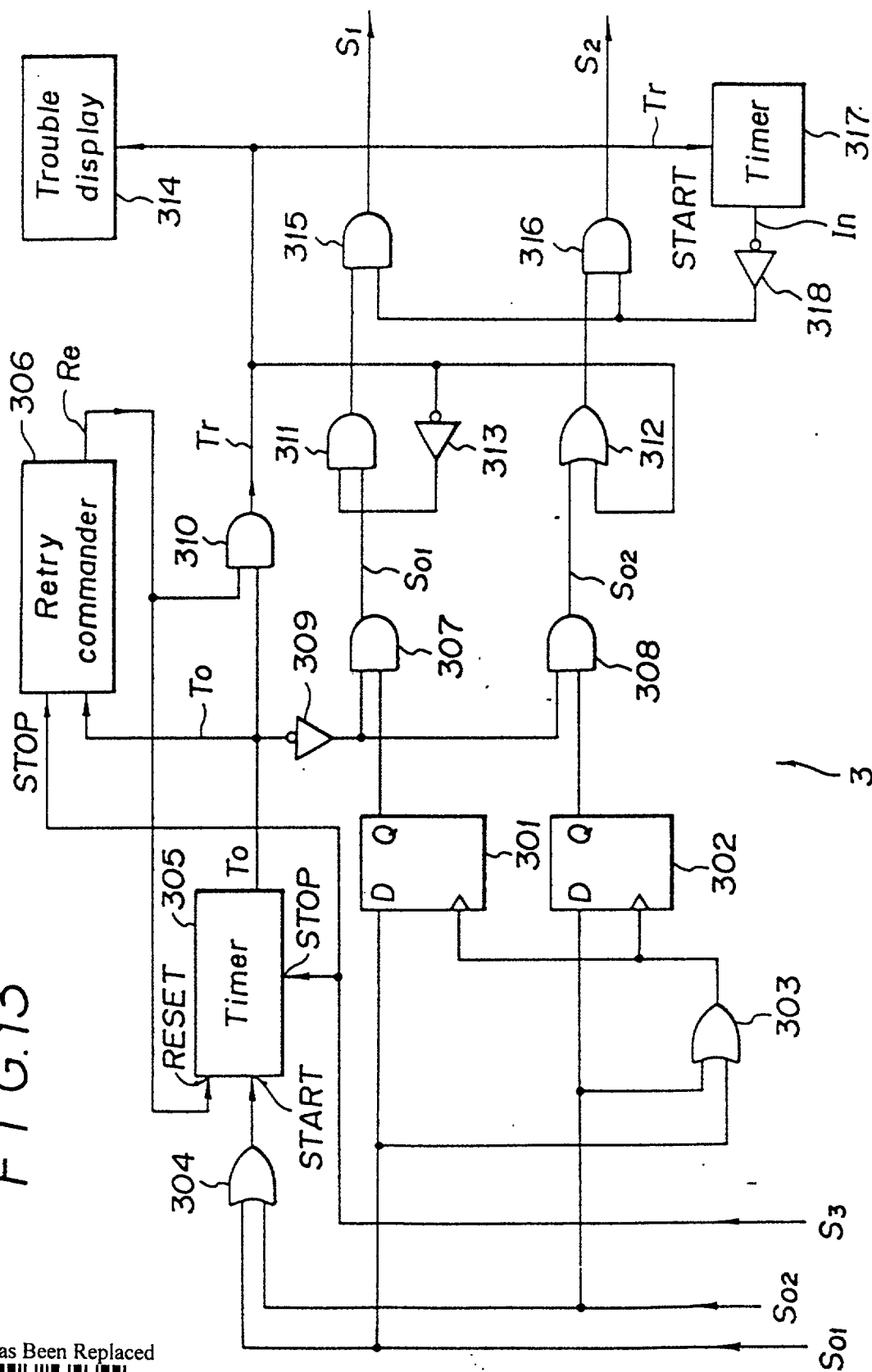


FIG. 14

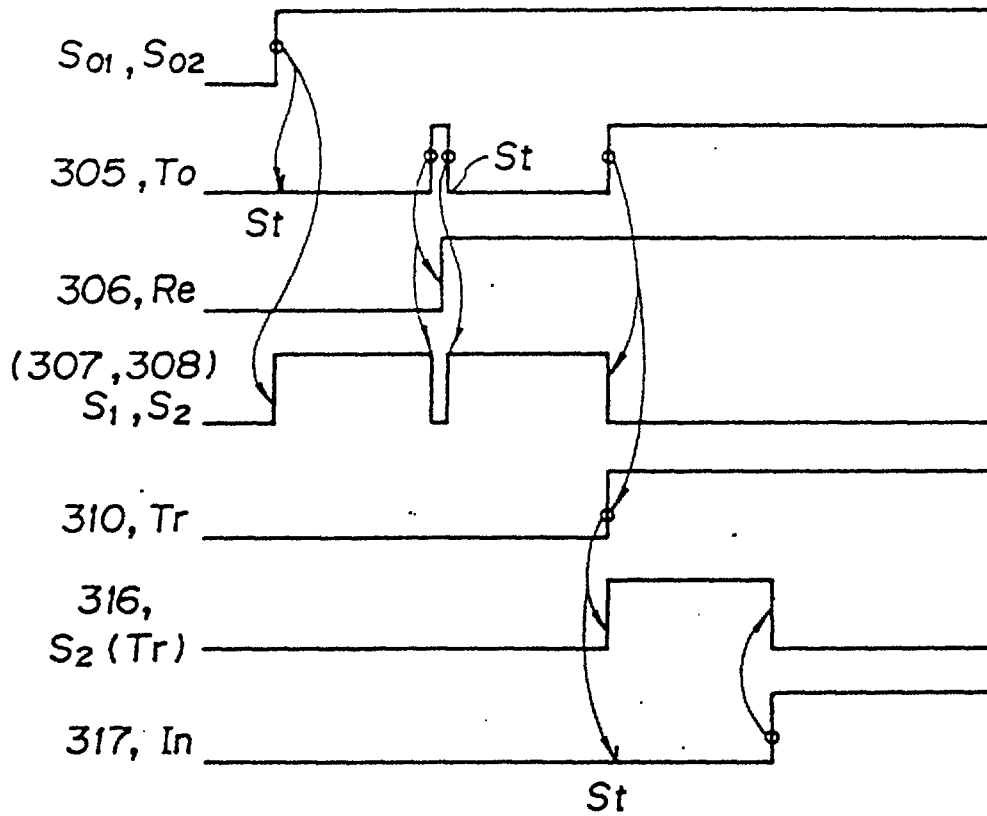


FIG. 15

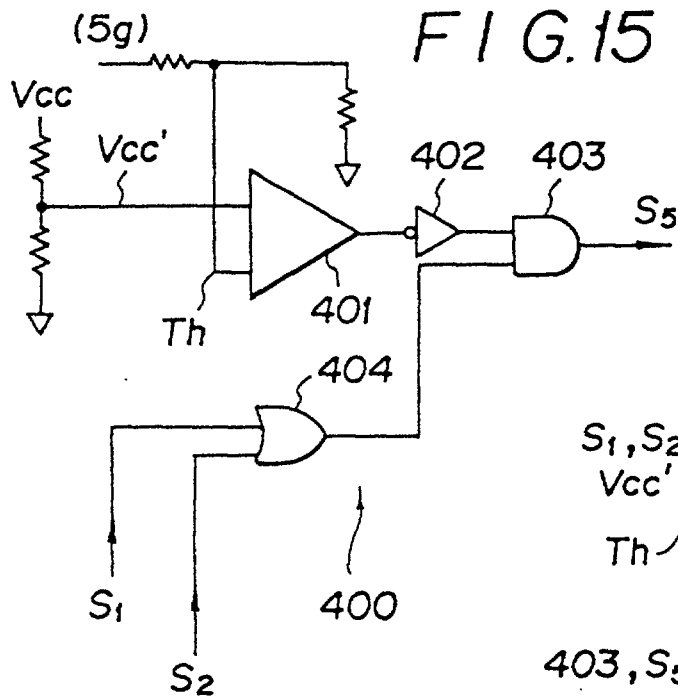
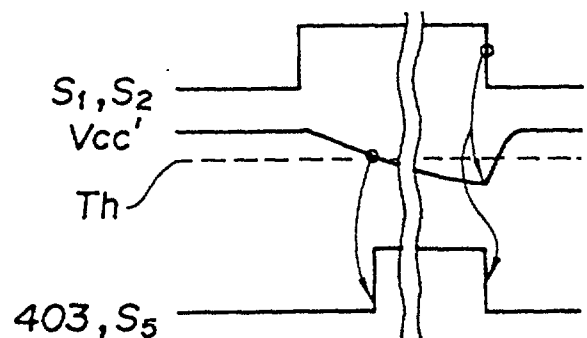


FIG. 16



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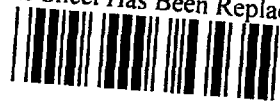


FIG. 17

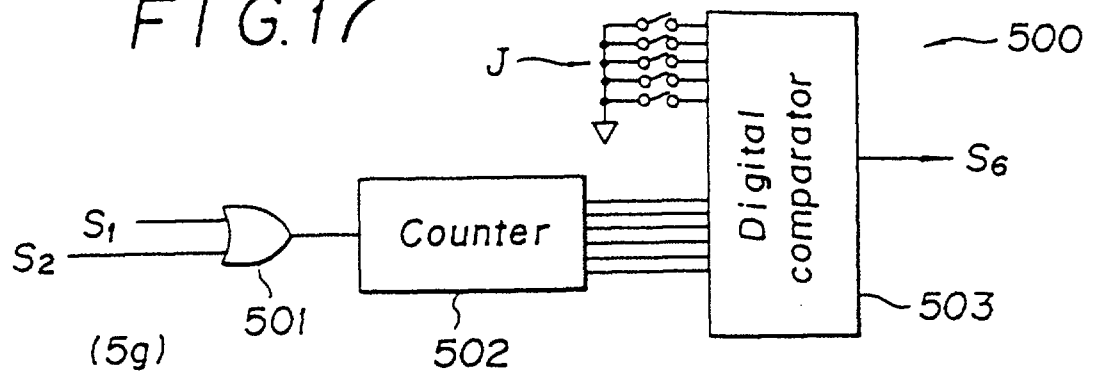


FIG. 18

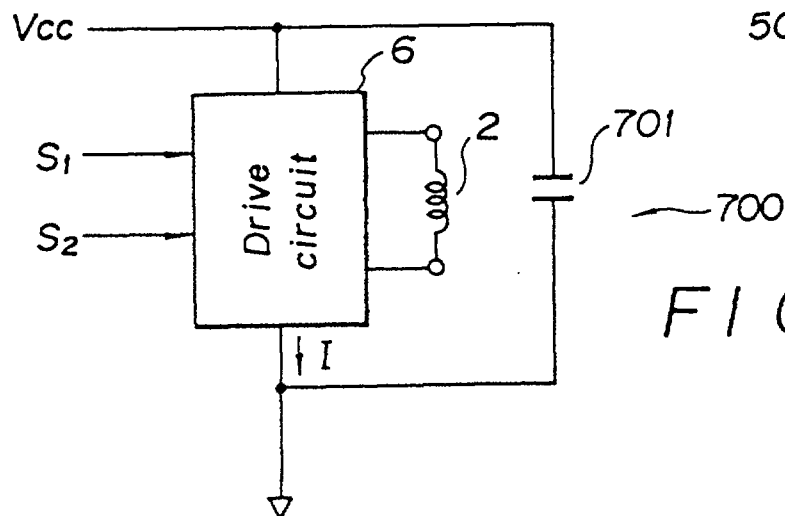
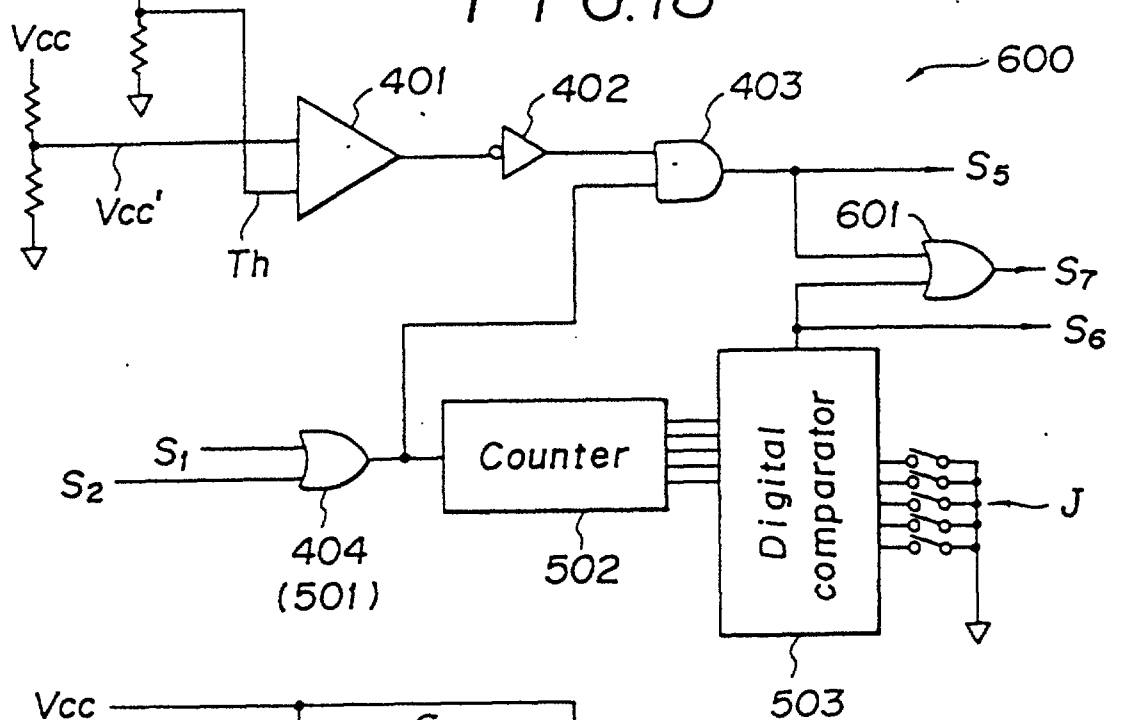


FIG. 19

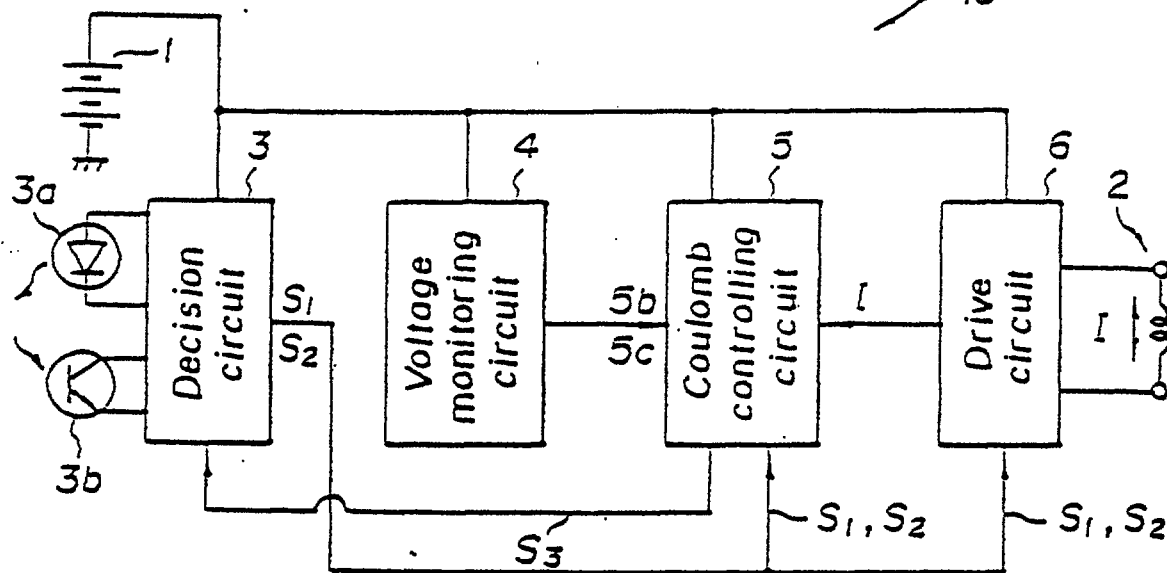
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FIG. 1



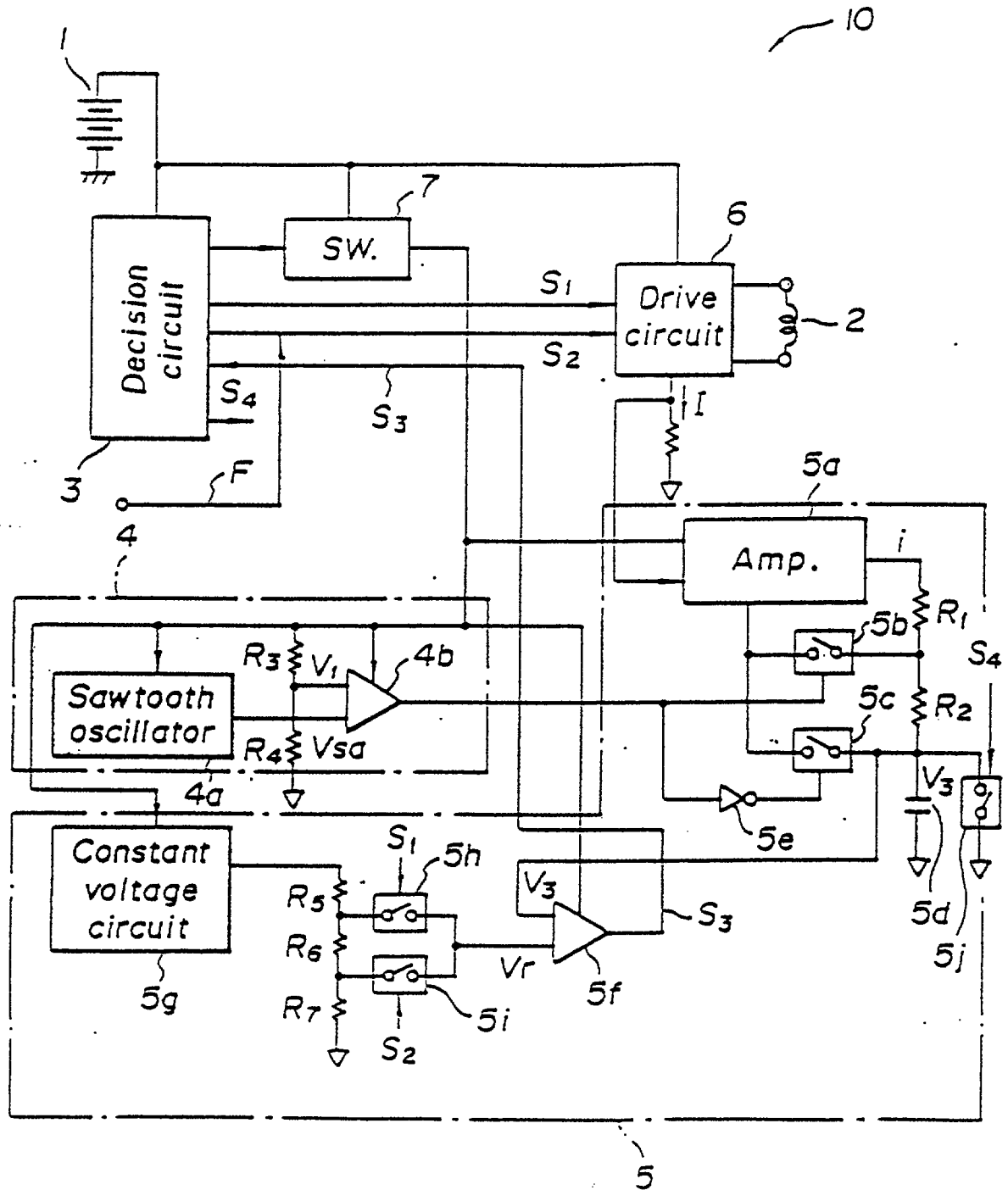
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FIG. 2



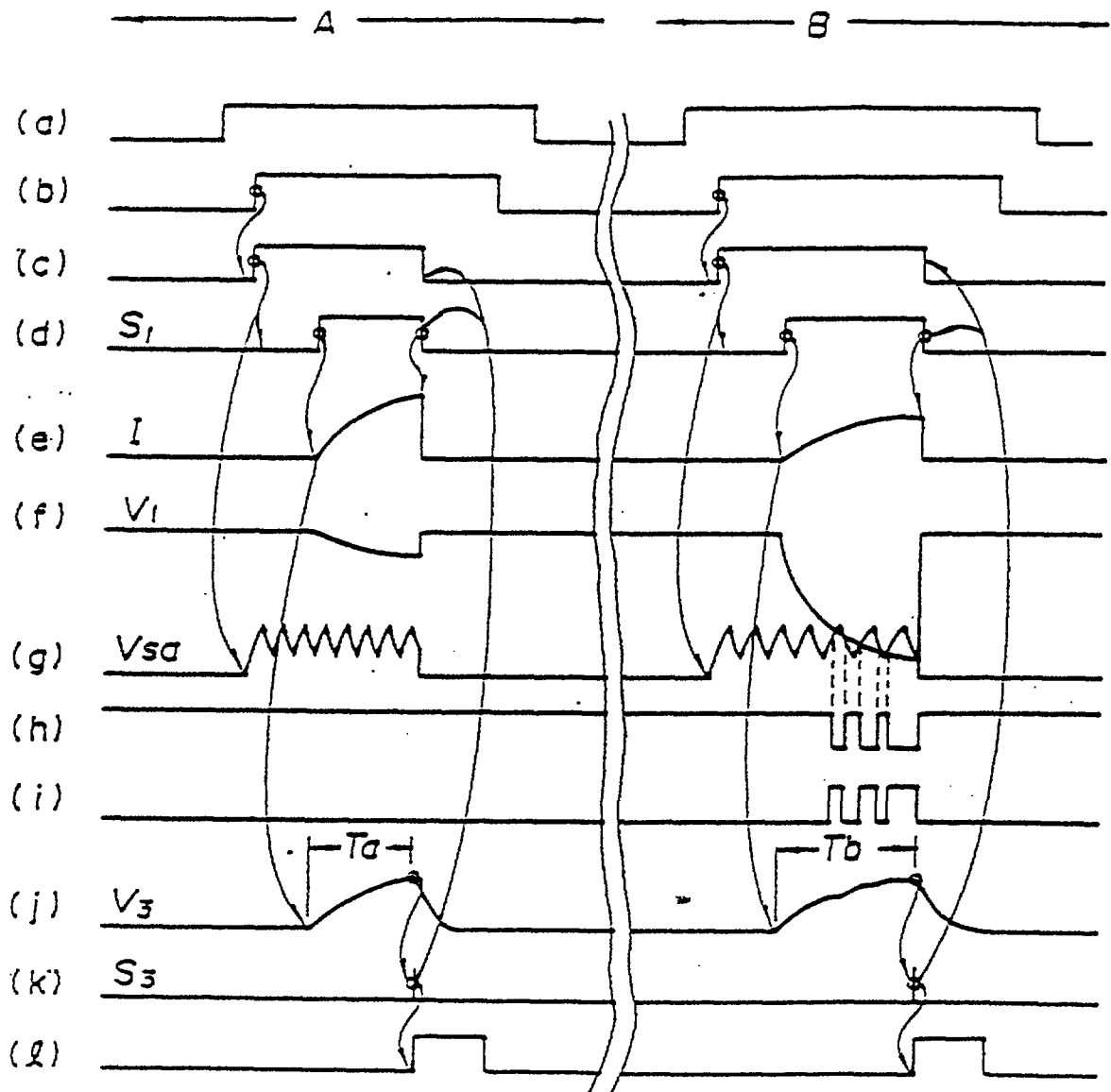
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FIG. 3

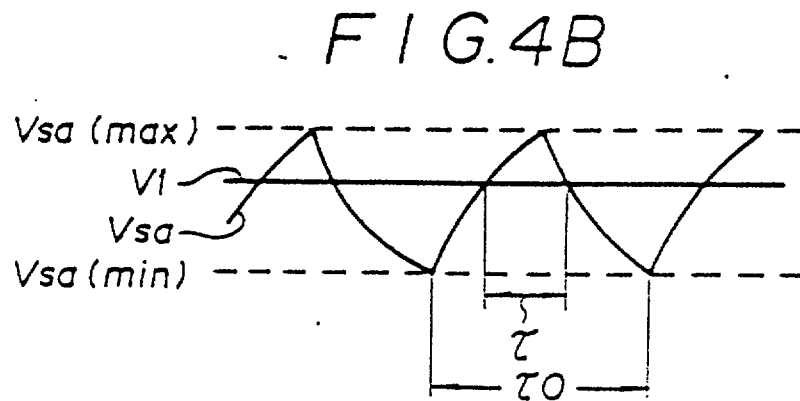
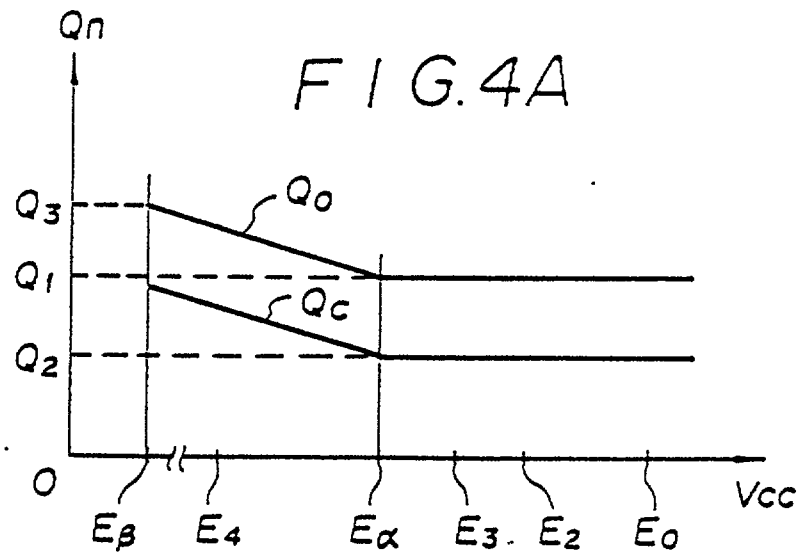


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FIG. 5

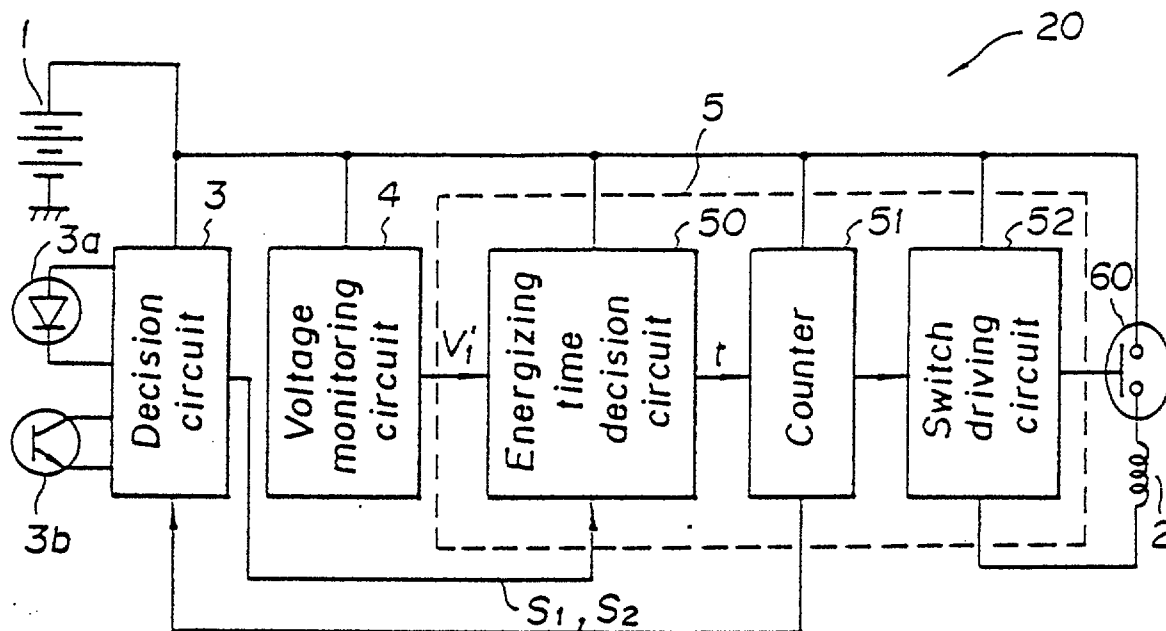
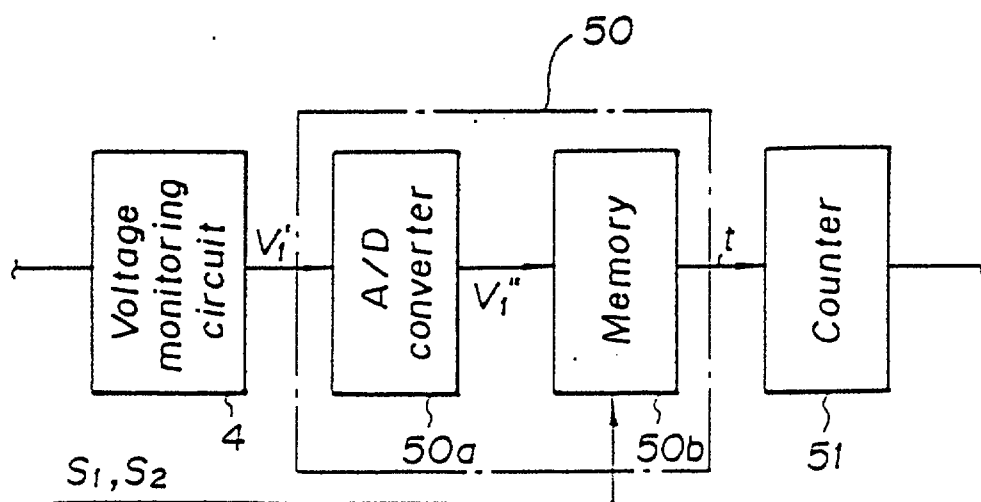


FIG. 6



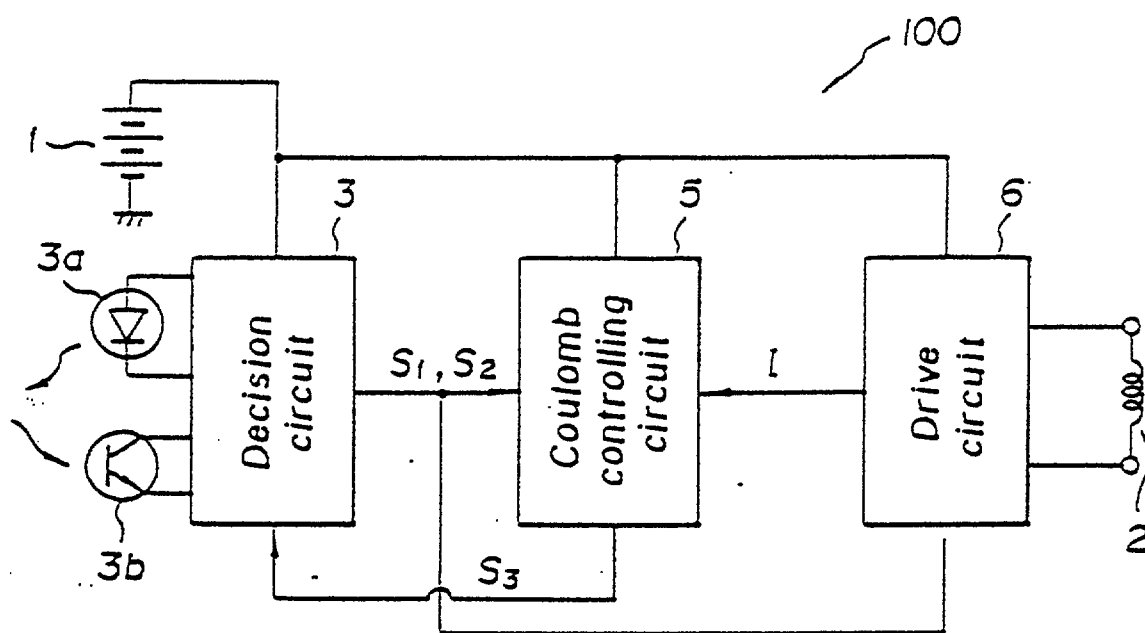
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FIG. 7



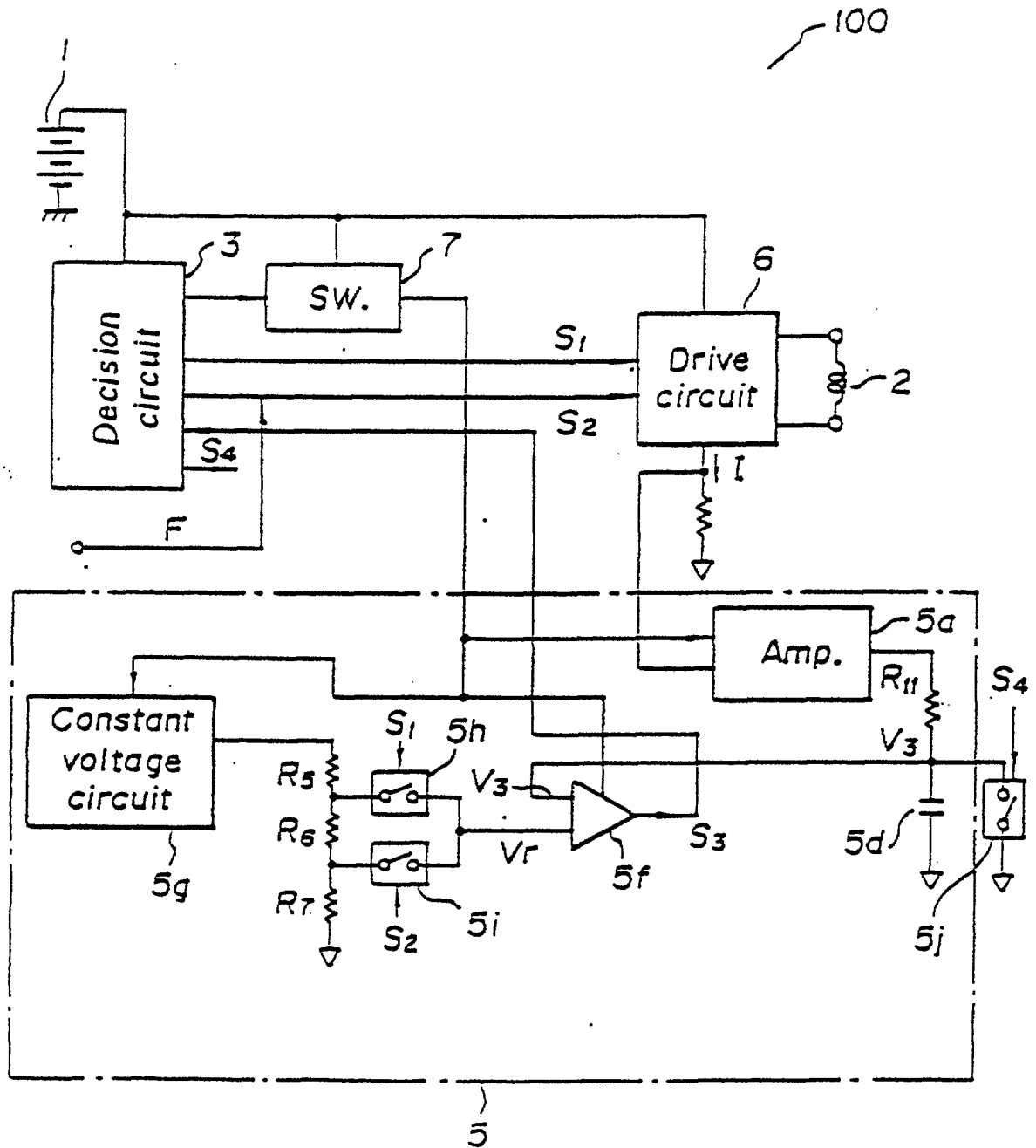
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FIG. 8



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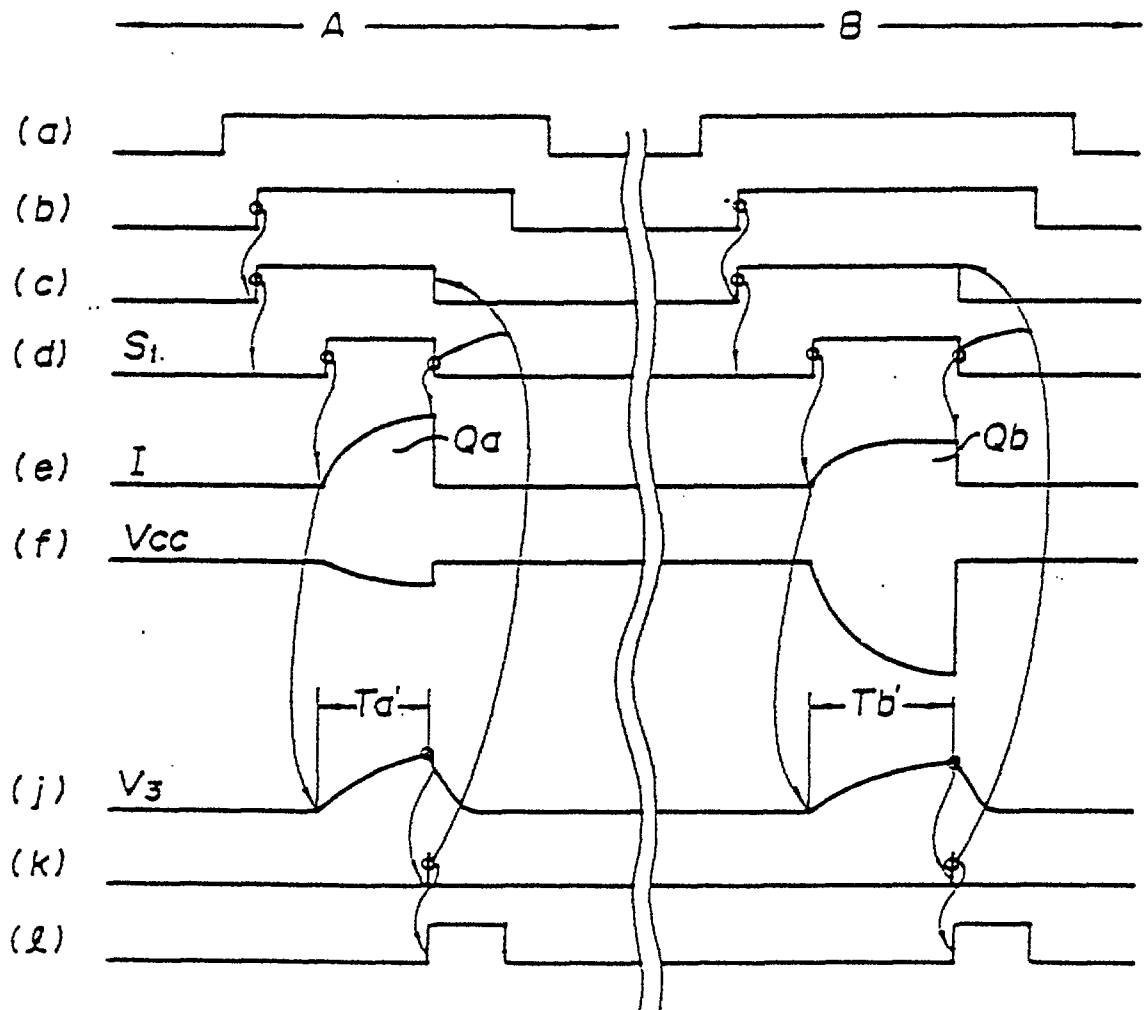
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FIG. 9



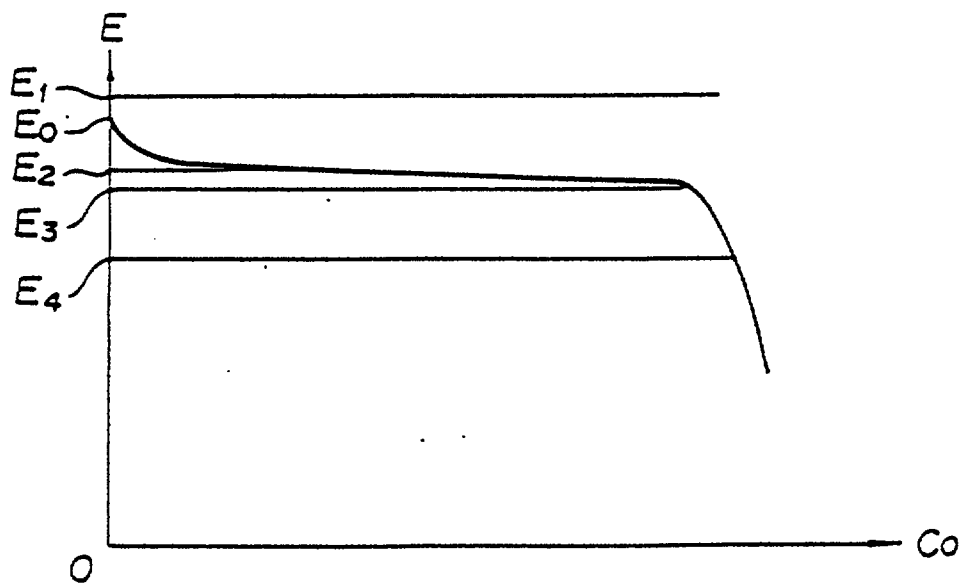
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FIG. 10



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FIG. 11

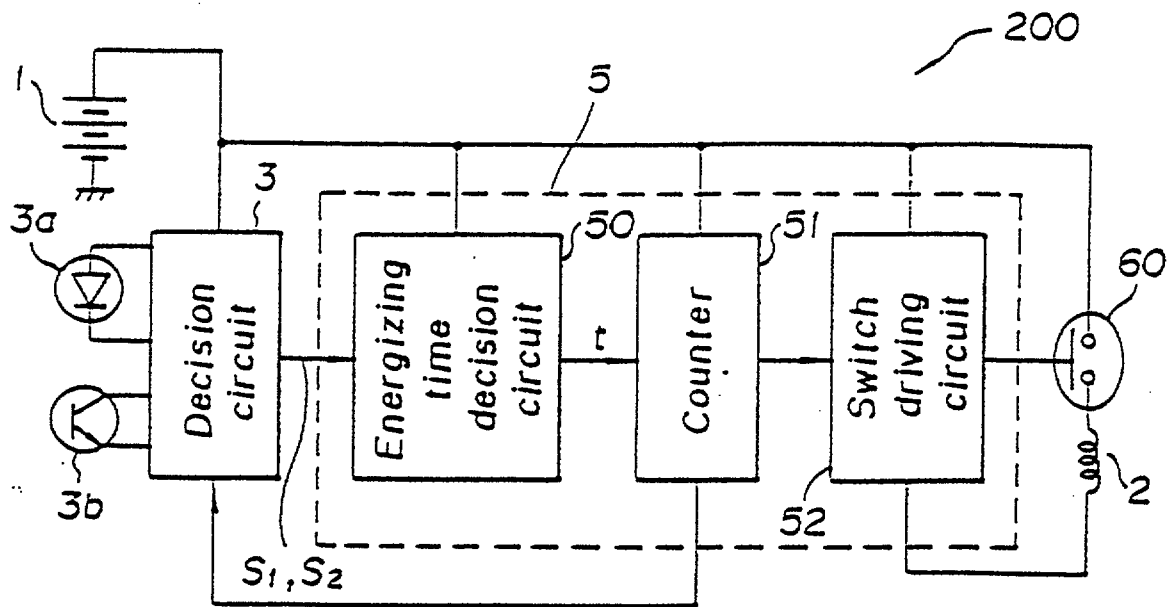
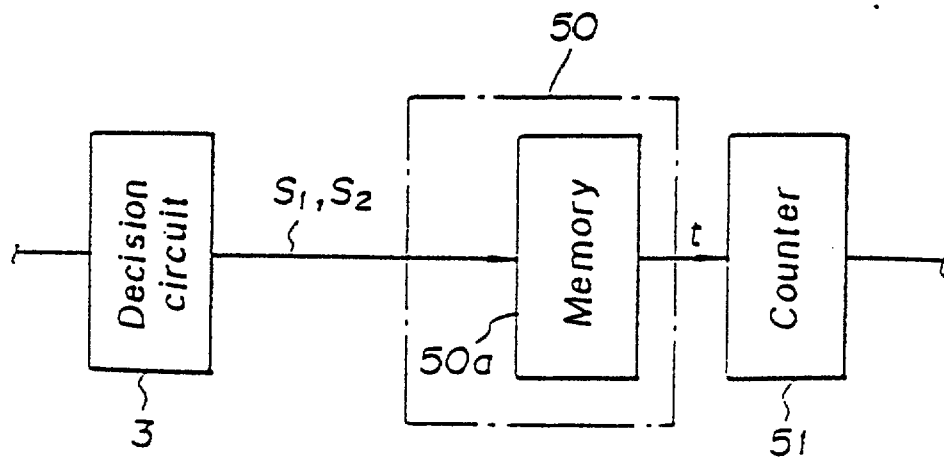


FIG. 12



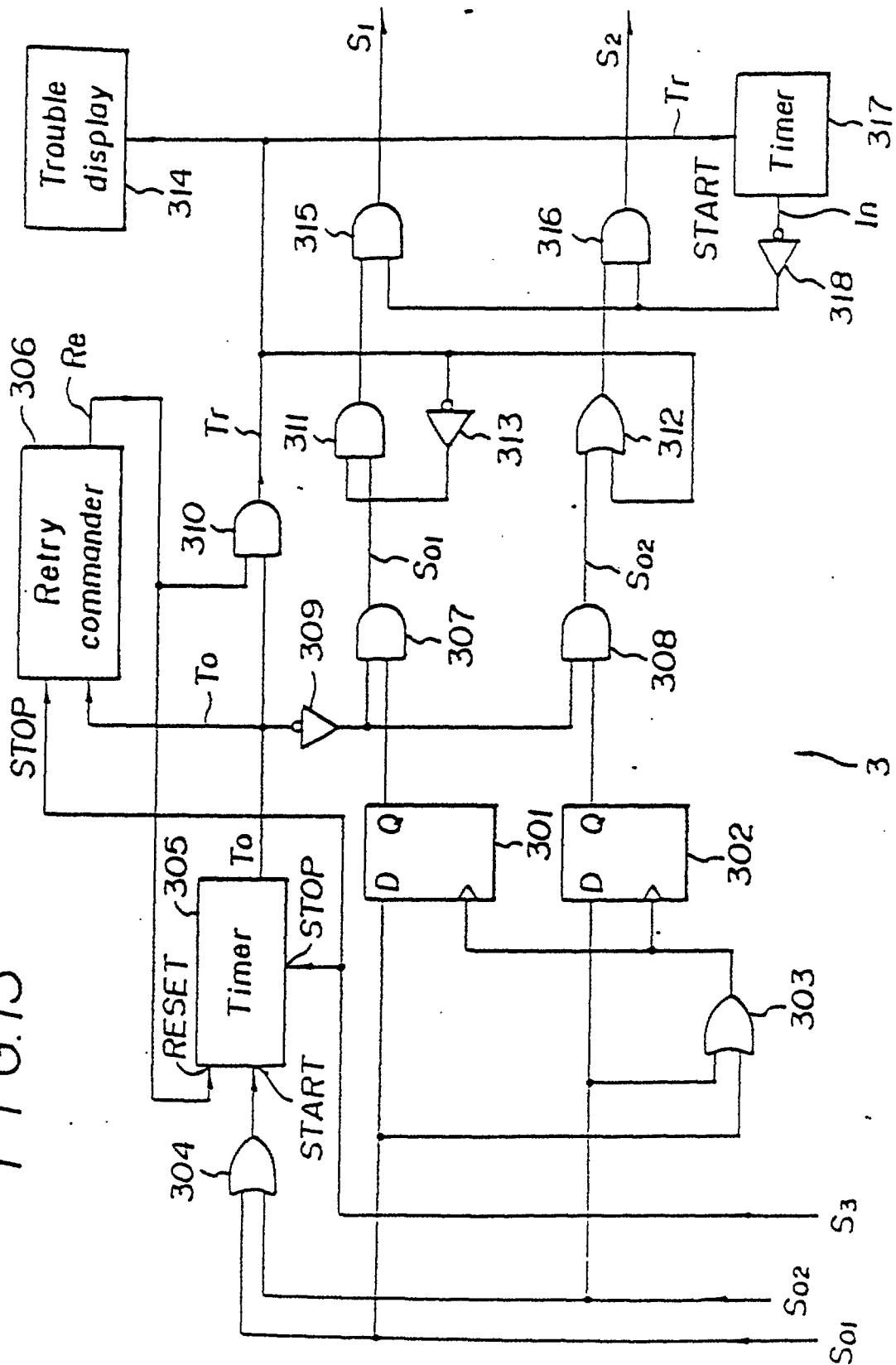
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FIG. 13



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FIG. 14

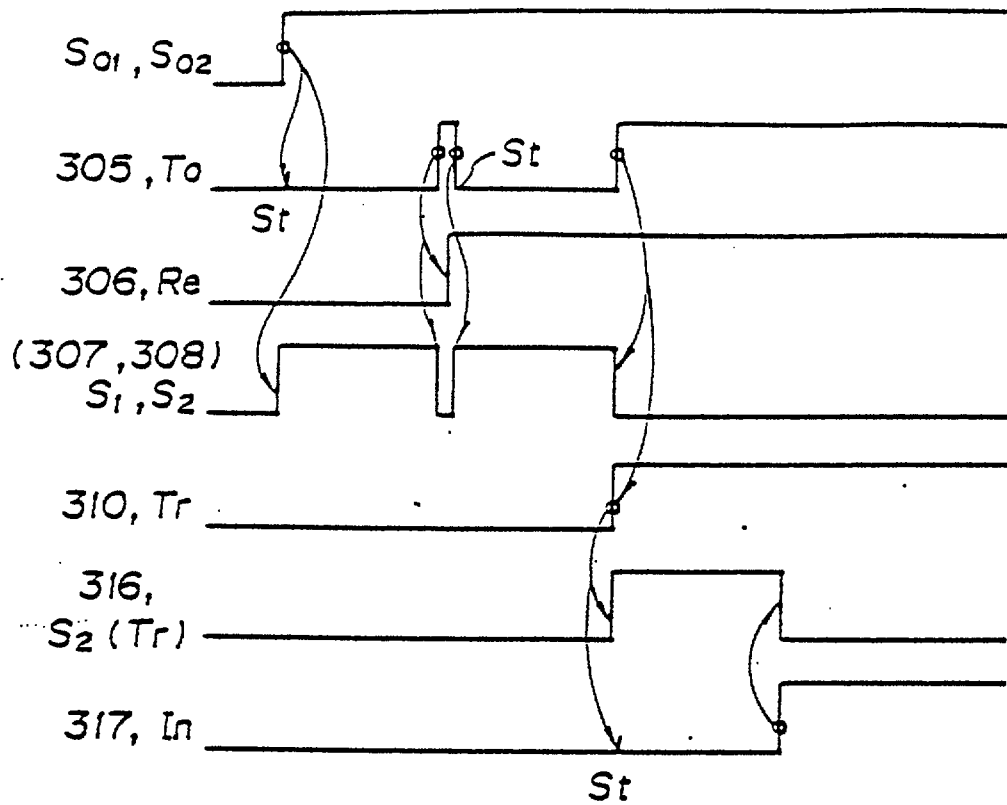


FIG. 15

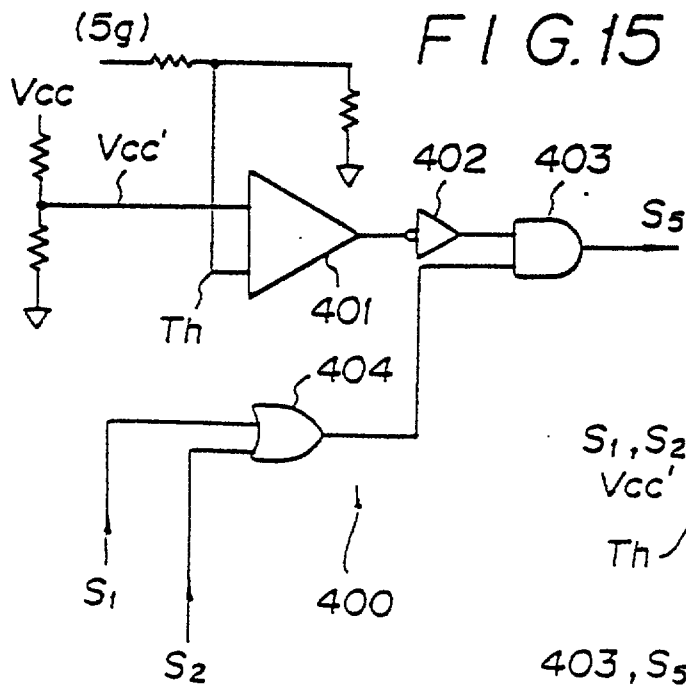
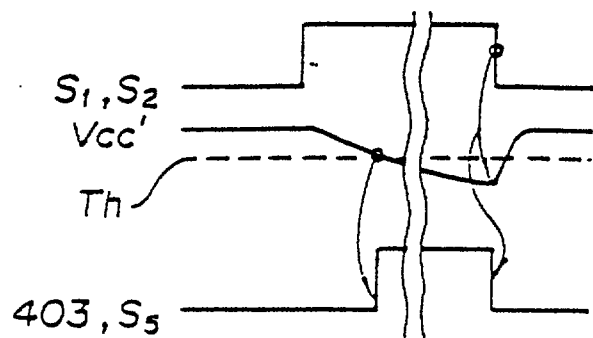


FIG. 16



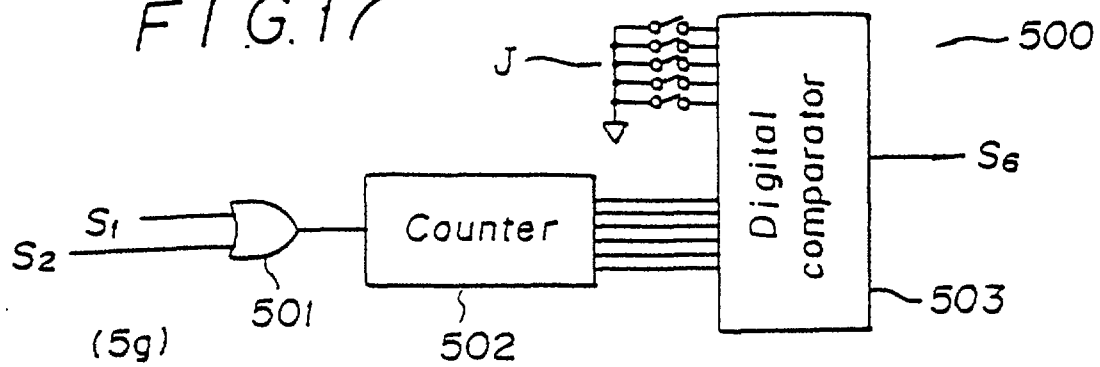
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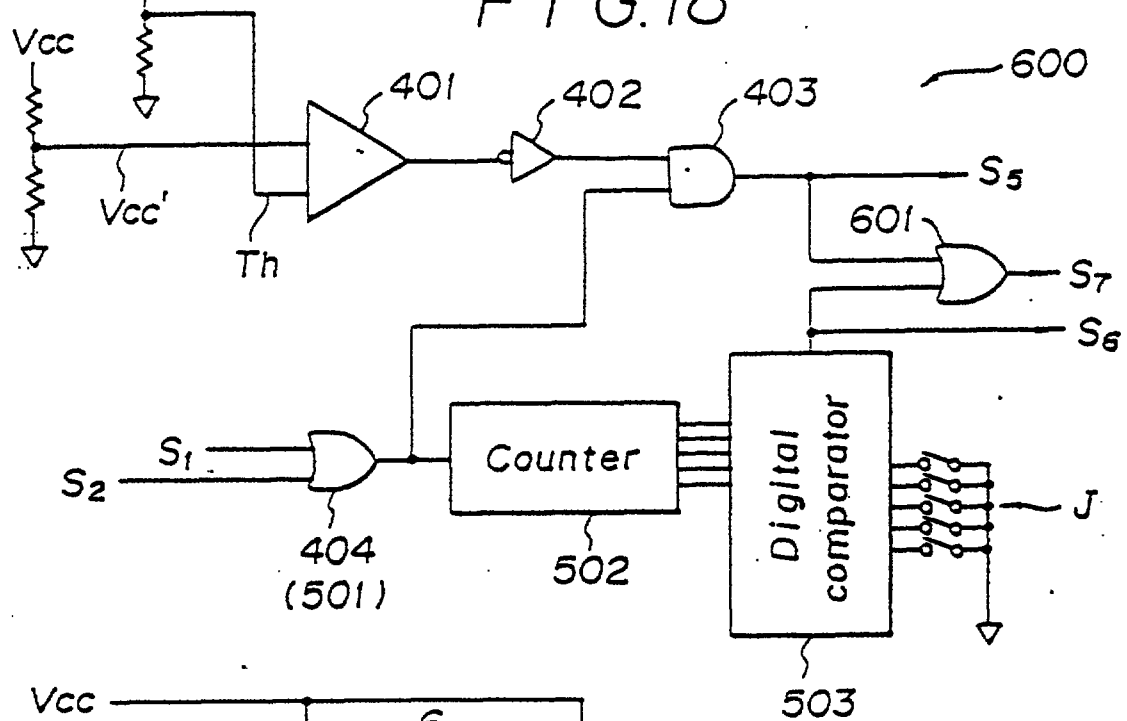
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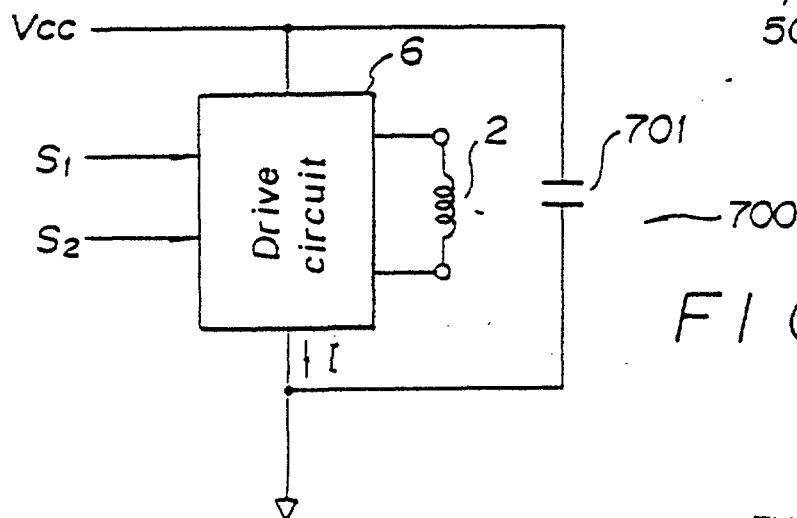
FIG. 17



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SOLENOID VALVE CONTROL CIRCUIT

Description

The present invention relates to a circuit for controlling the operation of a latching solenoid valve, and more particularly to a solenoid valve control circuit which employs a battery as a power supply.

Some washroom faucets have an automatic water supply control unit for automatically supplying water by actuating a faucet solenoid valve when the approach of a user to the faucet is detected, and for automatically stopping the water supply by actuating the solenoid valve again when the leaving of the user from the faucet is detected.

Generally, such solenoid valve comprises a plunger serving as a valve body and a latching solenoid for driving the plunger when it is energized. As shown in FIG. 4A of the accompanying drawings, it is empirically known that the solenoid valve has a certain characteristic between a power supply voltage V_{cc} applied to the solenoid and the quantity of electricity Q (i.e., all the electric current flowing through the solenoid, hereinafter referred to as an "electric quantity") through the solenoid. When the power supply voltage V_{cc} is low, the electric quantity Q_n which is required by the solenoid to drive the plunger is larger than the electric quantity Q_n that is required by the solenoid to drive the plunger when the voltage V_{cc} is sufficiently high. Stated otherwise, the electric quantity Q_n which is required and sufficient to drive the plunger has to be passed through the solenoid for a relatively long time when the power supply voltage V_{cc} is lower and for a relatively short time when the power supply voltage V_{cc} is higher.

Where a battery is employed as the power supply for the solenoid valve and the solenoid is to be energized for a constant period of time, a problem arises either when the voltage V_{cc} of the battery is higher because

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the battery is new or when the voltage V_{cc} of the battery is lower because the battery is old or deteriorated. More specifically, if the time for which the solenoid is to be energized is selected to be relatively short in view of new battery conditions, then the solenoid will not be sufficiently energized when the battery voltage V_{cc} becomes lower and the plunger will not be driven to a desired stroke. Conversely, if the time of energization of the solenoid is selected to be relatively long in view of old or deteriorated battery conditions, then the solenoid will be excessively energized when the battery voltage V_{cc} becomes higher, resulting in excessive electric power consumption and a shorter battery service life.

JP-A-62120006 discloses a circuit for driving a magnet to actuate printing elements of a daisy wheel so that printing pressure is kept constant for a set time, in which the current supplied to the magnet is controlled by the width of a load driving pulse dependent on power source voltage. This circuit does not, however, relate to battery powered latching solenoids for opening and closing valves.

The present invention has been made in view of the aforesaid problems with conventional latching solenoid valve control circuits.

It is an object of the present invention to provide a latching solenoid valve control circuit which can energize such a solenoid under optimum conditions irrespective of the voltage of a battery applied to the solenoid, so that the electric power from the battery will efficiently be consumed and the service life of the battery will be increased.

To accomplish the above object, there is provided in accordance with the present invention a solenoid valve control circuit for operatively connecting a battery to a solenoid to energize the solenoid to actuate a valve, the control circuit including coulomb controlling means for controllably supplying an electric quantity to the solenoid as detailed in claim 1.

The above and further objects, details and advantages of the present invention will become apparent from the following detailed description of preferred embodiments thereof, given by way of example only, when read in conjunction

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with the accompanying drawings.

FIG. 1 is a block diagram of a solenoid valve control circuit according to a first embodiment of the present invention;

FIG. 2 is a circuit diagram, partly shown in block form, illustrating the solenoid valve control circuit in greater detail;

FIG. 3 is a timing chart of output signals or operating conditions of circuit elements in the circuit shown in FIG. 2;

FIG. 4A is a graph showing the relationship between a power supply voltage and an electric quantity required by a solenoid;

FIG. 4B is a graph showing the relationship between a voltage produced by dividing the power supply voltage, and a sawtooth voltage;

FIG. 5 is a block diagram of a solenoid valve control circuit according to a first modification;

FIG. 6 is a block diagram showing some of the blocks of FIG. 5 in detail;

FIG. 7 is a block diagram illustrating a decision circuit in the solenoid valve control circuit shown in each of FIGS. 1 and 6;

FIG. 8 is a timing chart of output conditions of circuit elements in the circuit shown in FIG. 7 ;

FIG. 9 is a block diagram of a portion of a solenoid valve control circuit according to a second modification;

FIG. 10 is a timing chart of output conditions of circuit elements in the circuit shown in FIG. 9 ;

FIG. 11 is a block diagram of a portion of a solenoid valve control circuit according to a third modification; and

FIG. 12 is a block diagram of a portion of a solenoid valve control circuit according to a fourth modification.

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FIG. 1 shows a solenoid valve control circuit 10 according to a first embodiment of the present invention. The control circuit 10 in its entirety constitutes part of an automatic faucet unit (not shown). The control circuit 10 comprises a valve operation decision circuit 3 for determining valve operation, a voltage monitoring circuit 4 for monitoring a power supply voltage, a coulomb controlling circuit 5 for controlling the electric quantity to be supplied to a latching solenoid 2 of a solenoid valve (not shown), and a drive circuit 6 for driving the solenoid 2. The control circuit 10 controllably drives the latching solenoid 2 with electric power supplied from a battery 1 which is employed as the power supply for the control circuit 10. The solenoid 2 may have either a single winding (in which case the opening or closing of the solenoid valve is determined by the direction in which an electric current flows through the solenoid 2) or double windings (i.e., a winding for opening the solenoid valve and a winding for closing the solenoid valve). The power supply voltage V_{cc} is applied to the decision circuit 3 at all times. The decision circuit 3 is associated with an infrared-radiation

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light-emitting diode 3a which is intermittently energized to emit infrared radiation by the battery 1, and a phototransistor 3b which detects reflected light to detect whether a user moves toward or away from the automatic faucet device. Dependent on a detected signal from the phototransistor 3b, the decision circuit 3 applies valve opening/closing signals S1, S2 each of which can selectively take ON and OFF states (i.e., "high" and "low") to the drive circuit 6.

The automatic faucet unit with the control circuit 10 may be incorporated in various devices. Where the automatic faucet unit is assembled in a washroom faucet, both the signals S1, S2 are OFF when no user is present at the faucet. When an approaching user is detected, only the signal S1 is turned ON and the signal S2 remains OFF. As described later on, the signal S1 is turned OFF after the solenoid 2 has been energized with a suitable electric quantity. Thereafter, when the leaving of the user is detected, only the signal S2 is turned ON and the signal S1 remains OFF. After the solenoid 2 has been energized with a suitable electric quantity, the signal S2 is turned off. Therefore, the signal S1 is a solenoid valve opening signal, and the signal S2 is a solenoid valve closing signal. The light-emitting diode 3a and the phototransistor 3b are located at a suitable position near the faucet.

The power supply voltage monitoring circuit 4 monitors the voltage V_{cc} of the battery 1 and applies a signal dependent on the magnitude of the voltage V_{cc} to the coulomb controlling circuit 5.

When either one of the signals S1, S2 is turned ON, the solenoid valve drive circuit 6 supplies the solenoid 2 with an electric current I of a prescribed polarity to drive a plunger (not shown) serving as a valve body in a given direction. As shown in FIG. 4A, the electric quantity $Q_n = Q_o$ which is required to open the valve is greater than the electric quantity $Q_n = Q_c$ which is required to close

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the valve. In each of the opening and closing of the valve, the electric quantity required by the solenoid 2 to drive the plunger when the voltage V_{cc} of the battery 1 is low is greater than the electric quantity required by the solenoid 2 to drive the plunger when the battery voltage V_{cc} is sufficiently high. The horizontal axis of FIG. 4A represents the battery voltage V_{cc} , and the vertical axis the electric quantity Q_n required by the solenoid 2 to drive the plunger. Reference characters $E\alpha$, $E\beta$, $Q3$ will be described later with reference to FIG. 4A, and reference characters $E0$ through $E4$ will be described later with reference to FIG. 10. Generally, the entire electric charge quantity Q (= total electric quantity) passing through the solenoid is expressed by:

$$Q = \int I dt$$

where I is the electric current flowing through the solenoid and t is the time for which the solenoid is energized.

The coulomb controlling circuit 5 applies a detected signal $S3$ of a "high" level to the decision circuit 3 when the electric quantity Q supplied to the solenoid 2 reaches a prescribed value (= $Q_n = Q_0$ or Q_c). The solenoid valve opening/closing signals $S1$, $S2$ are also supplied to the coulomb controlling circuit 5, which varies output conditions for the detected signal $S3$ based on the signals $S1$, $S2$.

In response to the detected signal $S3$ from the coulomb controlling circuit 5, the decision circuit 3 turns OFF the one of the signals $S1$, $S2$ which is ON at the time, whereupon the drive circuit 6 de-energizes the solenoid 2.

FIG. 2 shows the solenoid valve control circuit 10, particularly the voltage monitoring circuit 4 and the coulomb controlling circuit 5, in detail. The decision circuit 3 comprises a plurality of logic circuits, for example, and each time it detects the approach or leaving of a user, it turns on a power supply switch 7 to apply the power supply voltage V_{cc} to the voltage monitoring circuit 4 and the coulomb controlling circuit 5.

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The drive circuit 6 is in the form of a bridge circuit comprising four power transistors, for example. The solenoid 2 is connected between the two output terminals of the bridge circuit. One of the two input terminals of the bridge circuit is connected to the positive terminal of the battery 1, whereas the other input terminal of the bridge circuit is grounded through a resistor. The signals S1, S2 are supplied to a pair of coacting power transistors which form opposite sides of the bridge circuit. While the solenoid 2 is being energized, part of the current I flowing through the solenoid 2 is supplied to a current amplifying circuit 5a of the coulomb controlling circuit 5 (Actually, a voltage signal similar to the solenoid current I is supplied to the amplifying circuit 5a).

The current supplied to the amplifying circuit 5a is supplied as a charging current i through resistors R1, R2 to a monitoring capacitor 5d.

Feedback signals are applied from those terminals of the resistors R1, R2 which are closer to the capacitor 5d than to the amplifying circuit 5a through switches 5b, 5c. The switches 5b, 5c are mutually exclusively closed by an output signal from the voltage monitoring signal 4. While only the switch 5b is closed, the current gain of the amplifying circuit 5a is maintained at k1, and while only the switch 5c is closed, the current gain of the amplifying circuit 5a is maintained at k2. k represents a prescribed gain determined by the circuit arrangement, and the current gains k1, k2 are selected such that $k1 = k/R1$ and $k2 = k/(R1 + R2)$, and hence $k1 > k2$. Therefore, as described later on, the average current gain of the amplifying circuit 5a is varied by the closing and opening of the switches 5b, 5c dependent on variations in the power supply voltage Vcc.

The charging current i which flows while only the switch 5b is closed is indicated by:

$$i = k1 \cdot I = (k/R1) \cdot I = k \cdot I/R1.$$

The charging current i which flows while only the switch 5c is closed is indicated by:

$$i = k_2 \cdot I = (k/(R_1 + R_2)) \cdot I = k \cdot I/(R_1 + R_2).$$

When the power supply switch 7 is turned ON, a sawtooth oscillator 4a of the voltage monitoring circuit 4 starts operating to supply a sawtooth voltage V_{sa} as a reference voltage to a comparator 4b. The sawtooth oscillator 4a may be replaced with a triangle generator. When the power supply switch 7 is turned ON, the power supply voltage V_{cc} is divided by resistors R_3 , R_4 , and a divided voltage V_1 is applied to the comparator 4b. The comparator 4b compares the applied voltage V_1 with the reference voltage V_{sa} . While $V_1 > V_{sa}$, the comparator 4b issues an output signal of a "high" level, and while $V_1 < V_{sa}$, the comparator 4b issues an output signal of a "low" level. The output signal from the comparator 4b is applied directly to one of the switches 5b of the coulomb controlling circuit 5 and via an inverter 5e to the other switch 5c. The switches 5b, 5c are closed only when they are supplied with a high-level signal, and hence they are exclusively or alternatively closed. More specifically, while $V_1 > V_{sa}$, the switch 5b is closed and the amplifying circuit 5a has the current gain k_1 , and while $V_1 < V_{sa}$, the switch 5c is closed and the amplifying circuit 5a has the current gain k_2 during which time the charging current i is lower. Denoted at F in FIG. 2 is an input line for closing the valve through a manual override.

As long as the current I flows through the solenoid 2, the capacitor 5d is continuously charged and a voltage V_3 at the input terminal of the capacitor 5d progressively rises. The voltage V_3 is applied as an input voltage to a comparator 5f which is supplied with a reference voltage V_r . While $V_3 < V_r$, the comparator 5f issues an output signal of a "low" level, and when $V_3 > V_r$, the comparator 5f issues an output signal of a "high" level. The high-level signal from the comparator 5f is sent as the de-energizing signal S_3 to

the decision circuit 3. The reference voltage V_r is determined according to the electric quantity Q_n required by the solenoid 2, and thus has different values when the valve is to be opened (i.e., when the signal S_1 is turned ON) and when the valve is to be closed (i.e., when the signal S_2 is turned ON). The reference voltage V_r is selected to be equal to the voltage V_3 across the capacitor 5d when the required electric quantity $Q_n (= Q_o, Q_c)$ has flowed through the solenoid 2 in the case where the power supply voltage V_{cc} is sufficiently high. The reference voltage V_r is produced by dividing, with resistors R_5, R_6, R_7 and switches $5h, 5i$, an output voltage from a constant voltage circuit or reference voltage generator 5g to which the power supply voltage V_{cc} is applied through the power supply switch 7. The switches $5h, 5i$ are closed respectively by the signals S_1, S_2 .

As described above with reference to FIG. 4A, the electric quantity $Q_n (= Q_o)$ required by the solenoid 2 to open the valve is greater than the electric quantity $Q_n (= Q_c)$ required by the solenoid 2 to close the valve. Therefore, when opening the valve, the switch $5h$ is closed by the signal S_1 to supply a relatively high divided voltage V_r as a reference voltage to the comparator 5f. When closing the valve, the switch $5i$ is closed by the signal S_2 to supply a relatively low divided voltage V_r as a reference voltage to the comparator 5f.

Regardless of whether the valve is opened or closed, the voltage V_3 across the capacitor 5d becomes equal to the reference voltage V_r when the electric quantity Q passing through the solenoid 2 reaches the required electric quantity Q_n . At this time, the comparator 5f sends the high-level de-energizing signal S_3 to the decision circuit 3.

At the same time as the decision circuit 3 receives the signal S_3 , it turns OFF the one of the signals S_1, S_2 which is ON at the time, opens the power supply switch 7, and

This is the replacement sheet

Date: 23 AUG 1999

applies an output signal S4 of a "high" level to a discharging switch 5j. The energization of the solenoid 2 is stopped, the circuits 4, 5 are de-energized, and the capacitor 5d is discharged, readying the control circuit 10 for a next cycle of operation.

As enclosed by the broken lines in FIG. 2, the voltage monitoring circuit 4 is constructed from the circuit elements 4a, 4b and the resistors R3, R4, and the coulomb controlling circuit 5 is constructed from the circuit elements 5a through 5j and the resistors R1, R2, R5, R6, R7.

FIG. 3 shows a timing chart of output signals or operating conditions of the circuit elements illustrated in FIG. 2. Those output signals shown in a lefthand area A in FIG. 3 are produced when the voltage Vcc of the battery 1 is sufficiently high, and those output signals shown in a righthand area B in FIG. 3 are generated when the battery voltage Vcc is lower. FIG. 3 only illustrates the output signals in the areas A, B for opening the valve. The output signals produced for closing the valve are similar and are not shown.

The charts of FIG. 3 represent the following conditions:

- (a) The operating condition of the decision circuit 3, i.e., the manner in which the circuit 3 detects the approach of a user.
- (b) The length of a processing time required to open the valve.
- (c) The opening and closing condition of the power supply switch 7.
- (d) The ON/OFF condition of the valve opening signal S1, i.e., the driving condition of the drive circuit 6. The drive circuit 6 is energized about 1 msec. after the power supply switch 7 is closed as shown at (c), and de-energized substantially at the same time that the power supply switch 7 is opened.

This is the replacement sheet

Date: 23 AUG 1999

- (e) The current I flowing through the solenoid 2.
- (f) The battery voltage V_{cc} . In the area B, since the internal resistance of the battery 1 is high, the voltage V_{cc} considerably drops when the solenoid 2 is energized.
- (g) The output voltage V_{sa} from the sawtooth generator 4a. The waveform and peak value of the voltage V_{sa} remain unchanged in the areas A, B.
- (h) The output condition of the comparator 4b, which indirectly represents the opening and closing condition of the switch 5b.
- (i) The opening and closing condition of the switch 5c, which is a reversal of the condition of (h).

With respect to the above charts (f), (g), (h), and (i), while the divided voltage V_1 is higher than the sawtooth voltage V_{sa} , only the switch 5b is closed, and while the divided voltage V_1 is lower than the voltage V_{sa} , only the switch 5c is closed.

- (j) The voltage V_3 for charging the capacitor 5d.
- (k) The output condition of the comparator 5f, i.e., the output condition of the de-energizing signal S_3 .
- (l) The time required for the decision circuit 3 to end the energization of the solenoid 2, i.e., the time in which the signal S_4 is rendered "high" in level to close the discharging switch 5j for a time long enough to discharge the capacitor 5d.

In the area A, the switch 5b remains continuously closed since $V_1 > V_{sa}$ at all times. Therefore, while the solenoid 2 is being energized, the charging current $i = k_1 \cdot I$ flows into the capacitor 5d.

In the area B, the switches 5b, 5c are exclusively closed based on the magnitude relationship between the sawtooth voltage V_{sa} and the divided voltage V_1 . As described above, the current gain of the amplifying circuit 5a is k_1 when the switch 5b is closed and it is k_2 when the switch 5c is closed. Therefore, the average gain k_{10} of the amplifying circuit 5a in the area B can be determined as follows:

FIG. 4B is a graph showing, at an enlarged scale, the charts (f) and (g) in overlapping relationship in the area B of FIG. 3. The reference characters $V_{sa}(\max)$ and $V_{sa}(\min)$ represent maximum and minimum values of the sawtooth voltage V_{sa} , and τ_0 indicates the cyclic period of the sawtooth voltage V_{sa} . If the period in which $V_1 < V_{sa}$ within one cycle of the voltage V_{sa} is τ ($0 \leq \tau \leq \tau_0$), then the average gain k_{10} of the amplifying circuit 5a can be expressed by:

$$k_{10} = (1 - (\tau/\tau_0)) \cdot k_1 + (\tau/\tau_0) \cdot k_2$$

Since $0 \leq \tau \leq \tau_0$ and $k_1 > k_2$ as described above,

$$k_1 \geq k_{10} \geq k_2$$

Particularly, when $V_1 \geq V_{sa}(\max)$, since $\tau = 0$,

$$k_{10} = k_1.$$

When $V_1 \leq V_{sa}(\min)$, since $\tau = \tau_0$,

$$k_{10} = k_2$$

Within the range of $V_{sa}(\min) \leq V_1 \leq V_{sa}(\max)$, because the period τ is in inverse proportion to the divided voltage V_1 , the average gain k_{10} is proportional to the divided voltage V_1 . In the area B, therefore, the average gain k_{10} is proportional to the power supply voltage V_{cc} , and hence as the voltage V_{cc} is lowered, so is the average gain k_{10} .

When the power supply voltage V_{cc} is relatively high, i.e., in the range of $V_{cc} > E\alpha$, in FIG. 4A, the electric quantity Q_0 required by the solenoid 2 to open the valve is of a substantially constant value Q_1 . When the power supply voltage V_{cc} is relatively low, i.e., $V_{cc} = E\beta$, the electric quantity Q_0 required by the solenoid to open the valve is of a value Q_3 . When the power supply voltage V_{cc} is in the range of $E\beta \leq V_{cc} \leq E\alpha$, $Q_1 \leq Q_0 \leq Q_3$. The

This is the replacement sheet

Date: 21 AUG 1999

range $E\beta \leq V_{cc} \leq E\alpha$ corresponds to the area B in FIG. 3.

The control circuit 10 is arranged such that when the power supply voltage V_{cc} is $E\alpha$ and $E\beta$, the divided voltage V_1 is equal to the maximum value $V_{sa}(\max)$ and the minimum value $V_{sa}(\min)$, respectively, of the sawtooth voltage V_{sa} . The values of the resistors R_1 , R_2 , the value of the reference voltage V_r supplied to the comparator 5f, and the capacitance of the capacitor 5d are selected such that when $V_{cc} = E\alpha$, the electric quantity Q supplied to the solenoid 2 is $Q = Q_1$ and when $V_{cc} = E\beta$, $Q = Q_3$. Therefore, $Q = Q_1$ when $V_{cc} > E\alpha$. Since the average gain k_{10} is proportional to the power supply voltage V_{cc} when $E\beta \leq V_{cc} \leq E\alpha$, as described above, the electric quantity Q supplied to the solenoid 2 is controlled so as to be substantially equal to Q_0 in FIG. 4A.

The aforesaid description has been directed to the opening of the valve. For closing the valve, the electric quantity Q supplied to the solenoid 2 in the area B is controlled so as to be equal to Q_c in FIG. 4A since only the reference voltage V_r supplied to the comparator 5f is lower.

As is apparent from the above description, the electric quantity Q supplied to the solenoid 2 is controlled so as to be dependent on the power supply voltage V_{cc} by the solenoid valve drive circuit 10. More specifically, the electric quantity Q is controlled so as to be equal to Q_0 ,

Q_c shown in FIG. 4A. Therefore, the solenoid 2 is energized in an optimum fashion regardless of whether the battery voltage V_{cc} is high or low. As a consequence, the electric power from the battery 1 is efficiently consumed, and the service life of the battery 1 is prolonged.

FIGS. 5 and 6 show a solenoid valve control circuit 20 according to a first modification of the present invention. Those components in FIGS. 5 and 6 which are identical to those of the control circuit 10 of the first embodiment are denoted by identical reference numerals, and will not be described.

This is the replacement sheet

Date: 23 AUG 1999

The control circuit 20 has a coulomb controlling circuit 5 comprising an energizing time determining circuit 50, a counter 51, and a switch driving circuit 52. The energizing time determining circuit 50 receives an analog output $V1'$ from the voltage monitoring circuit 4 and determines a time t for which the solenoid 2 is to be energized, based on the analog output $V1'$ and the valve opening/closing signals $S1$, $S2$ from the decision circuit 3. The counter 51 counts the determined energizing time t . While the counter 51 is counting the energizing time t , the switch driving circuit 52 closes a switch 60 to energize the solenoid 2. The switch 60 comprises a directional element such as a bridge circuit or the like for energizing the solenoid 2. The analog output $V1'$ from the voltage monitoring circuit 4 is produced by dividing the power supply voltage V_{cc} at a prescribed ratio.

As shown in FIG. 6, the energizing time determining circuit 50 comprises an A/D converter 50a for converting the analog output $V1'$ from the voltage monitoring circuit 4 into a digital signal $V1''$, and a memory 50b for determining an energizing time t in response to the digital signal $V1''$ and the valve opening/closing signals $S1$, $S2$. The memory 50b has two memory maps which can be selected by the signals $S1$, $S2$, respectively. Each of the memory maps stores data on required energizing times t based on the characteristics of the required electric quantity Q and the time-base current characteristics of the solenoid 2. The digital signal $V1''$ is applied as an address signal to the memory 50b to read data on the required energizing time t from the memory map which has been selected by the signal $S1$ or $S2$.

The electric quantity Q supplied to the solenoid valve 2 can be controlled so as to be of a magnitude dependent on the power supply voltage V_{cc} by the solenoid valve control circuit 20. Accordingly, the solenoid 2 is energized in an optimum fashion regardless of whether the

battery voltage V_{cc} is high or low. As a consequence, the electric power from the battery 1 is efficiently consumed, and the service life of the battery 1 is prolonged.

The circuit components 50, 51 of the control circuit 20 may be replaced with a PWM (Pulse Width Modulation) circuit responsive to the output from the power supply voltage monitoring circuit for producing pulses of a duration inversely proportional to the power supply voltage V_{cc} , and an output signal from the PWM circuit may be supplied to the switch driving circuit 52. In this case, the PWM circuit doubles as a timer circuit. Thus, a pulse generator with the pulse duration variable by the output from the power supply voltage monitoring circuit may be used as a timer.

FIG. 7 shows one detailed circuit arrangement for the decision circuit 3, and FIG. 8 is a timing chart showing output conditions of circuit components in the circuit 3.

The circuit 3 normally generates the valve opening/closing signals S_1 , S_2 based on signals S_{01} , S_{02} which serve as origins of the signals S_1 , S_2 . The signals S_{01} , S_{02} have

This is the replacement sheet

Date:

21 Aug 1999

waveforms as shown in the chart (d) in FIG. 3. When the de-energizing signal S3 is generated, these signals S01, S02 are changed to a "low" level by a non-illustrated logic circuit.

If no de-energizing signal S3 is produced due for example to a failure of the coulomb controlling circuit 5 even when the signal S1 or S2 is generated, then the circuit 3 temporarily stops the issuance of the signals S1, S2. Thereafter, the circuit 3 produces the signals S1, S2 again. If a de-energizing signal S3 is still not produced even by the regenerated signals S1, S2, the circuit 3 forcibly closes the valve and stops its controlling operation on the solenoid 2.

More specifically, the origin signals S01, S02 go high in level when the approach/leaving of a user is detected. The origin signals S01, S02 are applied respectively to D input terminals of F/F (flip-flop) circuits 301, 302 which serve as latch circuits. The signals S01, S02 are also applied to an OR gate 303, the output signal of which is applied to a CLK input terminal of the F/Fs 301, 302. Therefore, when either one of the origin signals S01, S02 goes high, both the F/Fs 301, 302 are operated, and a high-level output signal is issued from the Q output terminal of one of the F/Fs to which the high-level signal has been applied. Specifically, when the signal S01 goes high, the high-level output signal is issued only from the Q terminal of the F/F 301. When the signal S02 goes high, the high-level output signal is issued only from the Q terminal of the F/F 302. The output condition of the Q terminals of the F/Fs 301, 302 is latched until the signals S01, S02 go high again after they have gone low. The F/Fs 301, 302 are thus triggered by positive-going edges of the signals applied to their CLK input terminals.

The signals S01, S02 are also applied to an OR gate 304, the output of which is applied to a START terminal of a

This is the replacement sheet

Date: 23 AUG 1999

timer 305. Therefore, the output signal from the OR gate 304 goes high when at least one of the signals S01, S02 goes high, starting the timer 305. The output signal from the timer 305 is normally low in level. When the timer 305 reaches a time-out condition after it has counted the output signal from the OR gate 304 for a prescribed period of time, the timer 305 continuously issues a signal To of a high level. When a retry signal Re of a high level from a retry commander 306 is applied to a RESET terminal of the timer 305 under this condition, the output signal from the timer 305 goes low and starts counting the output signal from the OR gate 304. Times for which the timer 305 counts the input signal in response to signals applied to the START and RESET terminals thereof are equal to each other. These counting times are selected to be longer than the energizing time Tb shown in FIG. 3 at (j).

The output signal from the timer 305 which is normally low is applied to input terminals of AND gates 307, 308 through an inverter 309 to enable the AND gates 307, 308. The other input terminals of the AND gates 307, 308 are supplied with the output signals from the F/Fs 301, 302. The de-energizing signal S3 is applied to the STOP terminals of the timer 305 and the retry commander 306 for stopping the operation of the timer 305 and the retry commander 306. Therefore, insofar as the de-energizing signal S3 is normally generated, the timer 305 does not produce a high-level output signal. Normally, the output signals from the AND gates 307, 308 are thus equal to the origin signals S01, S02, respectively.

The high-level time-out signal To from the timer 305 is applied to the retry commander 306. Simultaneously in response to the time-out signal To, the retry commander 306 applies the high-level retry signal Re to the RESET terminal of the timer 305 and an input terminal of an AND gate 310. The output terminal of the AND gate 310 thus issues a

failure signal Tr of a high level

only when the timer 305 issues the time-out signal To after the retry signal Re has been issued. The retry command 306 may comprise a latch circuit.

The output signal from the AND gate 310 is supplied through an inverter 313 to an input terminal of an AND gate 311 and directly to an input terminal of an OR gate 312. The other input terminals of the AND gate 311 and the OR gate 312 are supplied with the signals $S01$, $S02$ from the AND gates 307, 308, respectively. Since the output signal from the AND gate 310 is low in level under normal condition, the output signal from the AND gate 311 is equal to the signals $S01$, $S02$ under normal condition.

The output signal from the AND gate 310 is sent to a trouble display circuit 314. When the failure signal Tr is issued from the AND gate 310, the trouble display circuit 314 indicates a failure condition through a pilot lamp or the like to show that the control circuit is suffering a failure somewhere therein.

The output signal from the AND gate 310 is also applied to a START terminal of a timer 317. The timer 317 normally continues to issue a low-level output signal. When the high-level failure signal Tr is applied to the START terminal of the timer 317, the timer 317 counts a prescribed period of time, and then continuously issues an output inhibit signal In of a high level. The time interval which is counted by the timer 317 is selected to be longer than the time counted by the timer 305.

The output signal from the timer 317 is applied via an inverter 318 to input terminals of AND gates 315, 316, the other input terminals of which are supplied with the output signals from the AND gate 311 and the OR gate 312. Normally, the output signal from the timer 317 is low in level, and the output signals from the AND gates 315, 316 are the same as the origin signals $S01$, $S02$, respectively,

This is the replacement sheet

Date:

27 AUG 1999

under normal condition. The output signals from the AND gates 315, 316 are supplied as the valve opening/closing signals S1, S2 to the coulomb controlling circuit 5 and the solenoid valve drive circuit 6, respectively.

Operation of the control circuit 3 shown in FIG. 7 will hereinafter be described with reference to FIG. 8. The timing chart of FIG. 8 shows the output conditions of the circuit elements indicated by the corresponding reference characters, and illustrates a failure condition of the control circuit 3 due to trouble of the coulomb controlling circuit 5, for example. As described above, the origin signals S01, S02 are generated by the non-illustrated logic circuit. Indicated at 316, S2(Tr) is a valve closing override signal produced by the failure signal Tr, and indicates that the signal functions in the same manner as the signal S2. Denoted at St in FIG. 8 is a time at which the timers 305, 317 start counting time.

When either the origin signal S01 or S02 goes high in level, the corresponding one of the valve opening/closing signals S1, S2 goes high, starting to energize the solenoid 2. At the same time, the START terminal of the timer 305 is supplied with a high-level signal through the OR gate 304 to start counting a prescribed period of time ($> T_b$).

Normally, the de-energizing signal S3 is generated before the timer 305 reaches a time-out condition, the origin signals S01, S02 go low, and the timer 305 and the retry commander 306 stop their operation. These conditions are not illustrated in FIG. 8.

In the event that no de-energizing signal S3 is produced upon elapse of the energizing time, e.g., T_b , for some reason, the timer 305 reaches a time-out condition. The timer 305 continuously issues a high-level time-out signal To. Therefore, one of the input terminals of each of the AND gates 307, 308 is supplied with a low-level signal from the inverter 309, with the result that the output signals

This is the replacement sheet

Date: 23 AUG 1999

from the AND gates 307, 308 go low again. The conditions of the origin signals S01, S02 are maintained by the Q output signals from the F/Fs 301, 302.

The time-out signal To is sent to the retry commander 306 to enable the latter to issue a retry signal Re after it has closed the discharging switch 5j for a prescribed period of time with a delay circuit (not shown). The retry signal Re is applied to the RESET terminal of the timer 305, which then issues a low-level signal and restarts counting a prescribed period of time ($T_b <$). Since the output signal from the timer 305 goes low, the AND gates 307, 308 are enabled again to issue the condition of the origin signals S01, S02 which are held in the F/Fs 301, 302. While the retry signal Re is also applied to the AND gate 310, the output signal from the timer 305 remains low. The signals from the AND gates 307, 308 are finally issued as the valve opening/closing signals S1, S2 from the AND gates 315, 316, respectively. This condition is indicated by a second "high" state of the chart represented by (307, 308) S1, S2 in FIG. 8, i.e., a retry condition.

After the signals S1, S2 have been issued again, the origin signals S01, S02 go low if the de-energizing signal S3 is produced before the time-out condition of the timer 305, and the operation of the timer 305 and the retry commander 306 is stopped. This condition is not illustrated in FIG. 8.

If no de-energizing signal S3 is produced upon elapse of the energizing time, e.g., T_b , for some reason, then the timer 305 reaches a time-out condition. The timer 305 continues to issue a high-level time-out signal To again. Therefore, the output signals from the AND gates 307, 308 go low, thus inhibiting the transmission of the origin signals S01, S02 past the AND gates 307, 308. As a result, the output of the valve opening/closing signals S1, S2 is inhibited.

Since the retry signal Re is maintained at the high level at this time, the high-level failure signal Tr is issued from the AND gate 310.

The failure signal Tr is sent to the trouble display circuit 314, which then continuously indicates the failure condition.

The failure signal Tr is also applied to the START terminal of the timer 317 to enable the latter to start counting a prescribed period of time. Since the output signal from the timer 317 is low until it reaches a time-out condition, a high-level signal is applied to one input terminal of the AND gate 316 to enable the latter.

The failure signal Tr is also fed to the OR gate 312. Therefore, the output signal from the OR gate 312 goes high, and is issued as the valve closing signal S2 (Tr) caused by the failure signal Tr. The solenoid valve drive circuit 6 closes the valve in response to the signal S2 (Tr).

When the timer 317 has completed the counting of the prescribed time, it issues a high-level output inhibit signal In to disable the AND gates 315, 316, so that the issuance of the valve closing signal S2 (Tr) is inhibited. The timer 317 subsequently continues to issue the output inhibit signal In to inhibit the issuance of the valve opening/closing signals S1, S2.

Even after the forced closing of the valve with the override signal S2 (Tr) has been brought to an end, the failure signal Tr and the output inhibit signal In are maintained to inhibit the solenoid 2 from being energized and to indicate the failure.

With the aforesaid arrangement of the decision circuit 3, any wasteful consumption of the electric energy stored in the battery, which would otherwise be caused by some failure of the control circuit, can be avoided. Even if no de-energizing signal S3 is obtained within a

This is the replacement sheet

Date: 23 AUG 1999

prescribed period of time, the valve opening/closing signals S1, S2 are automatically rendered low, thus effectively preventing a reverse latching phenomenon in which if the energizing time is long, the valve which has once been opened is closed again because of solenoid characteristics exhibited when closing the solenoid.

Since the circuit 3 informs the operator of a failure condition, the operator can immediately find such a failure of the control circuit. In addition, the valve is forcibly closed when the circuit 3 determines that the control circuit suffers a failure. Accordingly, the control circuit is associated with an effective fail-safe system.

The circuit 3 does not regard a single time-out condition of the timer 305 as a failure, but tries to energize the solenoid again through the retry commander 306 should such a time-out condition occur. This prevents the control circuit from being de-energized by a single extrinsic error which may be caused by noise or the like.

A solenoid valve control circuit 400 according to a second modification will be described with reference to FIGS. 9 and 10. Circuit elements 401, 402, 403, 404 illustrated in FIG. 15 are added to the control circuit 10, described above for detecting a drop in the battery voltage Vcc.

A voltage produced by dividing the output voltage from the reference voltage generator 5g at a prescribed ratio is applied as a reference voltage Th to a comparator 401, the reference voltage Th providing a threshold value. The battery voltage Vcc is divided into an input voltage Vcc' which is applied to the comparator 401. When the input voltage Vcc' is higher than the threshold voltage Th, the comparator 401 issues a high-level signal to one input terminal of an AND gate 403 through an inverter 402.

The valve opening/closing signals S1, S2 are applied to an OR gate 404, the output signal of which is

This is the replacement sheet

Date: 23 AUG 1999

applied to the other input terminal of the AND gate 403. Thus, while either the signal S1 or S2 is high in level, the AND gate 403 is enabled to issue an output signal. That is, the AND gate 403 can issue an output signal only when the solenoid 2 is energized.

If the voltage V_{cc} drops lower than the threshold voltage Th while either the signal S1 or S2 is high and the solenoid 2 is being energized, the output signal from the comparator 401 goes low. The low-level signal from the comparator 401 is applied through an inverter 402 as a high-level signal to the AND gate 403. Consequently, the AND gate 403 issues a signal S5 of a high level which represents that the battery voltage V_{cc} drops lower than a prescribed voltage level.

FIG. 10 shows the output condition of the voltage drop signal S5. The voltage drop signal S5 is delivered to a non-illustrated circuit so as to be processed thereby in a predetermined manner.

For example, the signal S5 is sent to a latch circuit (not shown) which produces an output signal to enable a liquid crystal display, for example, to display the reduction in the battery voltage.

The signal S5 may be employed to perform the same function as the failure signal Tr shown in FIGS. 7 and 8.

A drop in the battery voltage V_{cc} when there is no load on the battery can be detected even by dispensing with the OR gate 404 and the AND gate 403. It is in practice preferable, however, to detect any drop in the voltage V_{cc} when the battery is loaded by energizing the solenoid 2 as illustrated. While only one threshold Th is employed in the above modification, two threshold values may be established, with the higher threshold value used for warning the operator about a voltage drop and the lower threshold value for de-energizing the entire control system.

FIG. 11 illustrates a solenoid valve control circuit 500 according to a third modification of the present in-

vention. Circuit components 501, 502, 503 shown in FIG. 11 are added to the control circuit 10 for determining that the battery is used up when the solenoid 2 is energized a number of times in excess of a predetermined number.

The solenoid opening/closing signals S1, S2 are applied to an OR gate 501, the output signal of which is applied to a counter 502 to count the number of times which the solenoid 2 is energized. The count is then applied as a digital signal to a digital comparator 503.

A reference count applied to the digital comparator 503 is set to a prescribed value (= an integer) through a jumper switch J. The reference count is selected to be a number of times the solenoid 2 is energized to use up the electric energy stored in the battery. The digital comparator 503 issues an output signal S6 of a high level when the count exceeds the reference count.

The signal S6 is a signal which statistically or indirectly represents that the battery voltage Vcc drops below a prescribed value. The voltage drop signal S6 is sent to a certain circuit (not shown) so as to be processed thereby. The signal S6 is practically equivalent to the voltage drop signal S5 described above, and the manner of utilizing the signal S6 is also the same as the manner of utilizing the signal S5.

A solenoid valve control circuit 600 in accordance with a fourth modification of the present invention is shown in FIG. 12. Circuit elements 401, 402, 403, 404 (or 501), 502, 503 shown in FIG. 12 are added to the control circuit 10. Those circuit elements in FIG. 12 which are identical to those of the control circuits 400 and 500 will not be described below.

The control circuit 600 simultaneously performs the functions of the control circuits 400, 500. However, the signals S5, S6 are applied to an OR gate 601, which produces an output signal S7 of a high level when the signal S5 or S6

This is the replacement sheet

Date: 21 AUG 1999

goes high. The signal S7 is applied to a certain circuit and processed thereby.

The signal S7 is produced when the solenoid 2 has been energized a number of times in excess of a predetermined number or when the battery voltage V_{cc} drops below a prescribed value. By using the signal S7 as a battery consumption signal, the battery can reliably be replaced with a new one before the battery power is completely used up.

The aforesaid modifications of the invention may be combined in various combinations.

This is the replacement sheet.

Date: 23 AUG 1999

Claims

1. A solenoid control circuit (10;20) for operatively connecting a battery (1) to a solenoid (2) to energize the solenoid (2), said control circuit including:

coulomb controlling means (4,5) for supplying a controllable electric charge quantity (Q) to the solenoid (2), said electric charge quantity (Q) corresponding to the voltage (Vcc) of the battery (1);

characterised in that:

said solenoid is a latching solenoid (2) having a plunger for opening and closing a valve, and in that said electric charge quantity (Q) is controlled to the value required (Qn, Qo, Qc) to energize said latching solenoid (2) to move the solenoid plunger for opening and closing the valve.

2. A solenoid valve control circuit (10) according to claim 1, further comprising:

a decision circuit (3) for producing an energizing signal (S1, S2) indicating that said battery (1) is to be connected to said solenoid (2) under a prescribed condition; and

a solenoid valve drive circuit (6) responsive to said energizing signal (S1, S2) for operatively connecting said battery (1) to said solenoid (2) to energize said solenoid (2), and

wherein said coulomb controlling means (4, 5) comprises:

a power supply voltage monitoring circuit (4) for monitoring the voltage (Vcc) of said battery (1) and producing a signal (f; g) corresponding to the battery voltage (Vcc); and

a coulomb controlling circuit (5) for monitoring the electric quantity (Q) supplied from said battery (1) to said solenoid (2) and for producing a de-energizing signal (S3) based on the signal (f; g) from said power supply voltage monitoring circuit (4) when the electric quantity (Q) supplied to said solenoid (2) is equal to said required electric quantity (Qn) corresponding to said battery voltage (Vcc).

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23 AUG 1999

3. A solenoid valve control circuit (10) according to claim 2, wherein said coulomb controlling circuit (5) comprises:

an amplifying circuit (5a, 5b, 5c, R1, R2) connected to said solenoid (2) for amplifying an electric current (I) to be supplied to the solenoid (2);

a capacitor (5d) chargeable to a prescribed charge level (C.V3) in response to the amplified current (k1.I, k2.I) from said amplifying circuit (5a, 5b, 5c, R1, R2); and

a comparator (5f) for comparing a voltage (V3) across said capacitor (5d) with a reference voltage (Vr) and producing said de-energizing signal (S3) when the voltage (V3) across said capacitor (5d) is equal to said reference voltage (Vr); and

said amplifying circuit (5a) being responsive to said signal (f; g) corresponding to the battery voltage from said power supply voltage monitoring circuit (4) for amplifying said electric current to be supplied to said solenoid (2) at a gain (k10) proportional to said battery voltage (Vcc).

4. A solenoid valve control circuit (10) according to claim 2 or 3, wherein said amplifying circuit (5a, 5b, 5c, R1, R2) amplifies said electric current (I) at a constant gain (k1) when said battery voltage (Vcc) is relatively high,

said reference voltage (Vr) of said comparator (5f) being set to be equal to the voltage (V3) across said capacitor (5d) when said required electric quantity ($Q_n = Q_1, Q_2$) is supplied to said solenoid (2) in case said battery voltage (Vcc) is relatively high.

5. A solenoid valve control circuit (10) according to claim 2, 3 or 4, wherein said de-energizing signal (S3) from said coulomb controlling circuit (5) is supplied to said decision circuit (3), said decision circuit (3) being responsive to said de-energizing signal (S3) for stopping the generation of said energizing signal (S1, S2).

This is the replacement sheet



Date: 23 AUG 1999

6. A solenoid valve control circuit (20) according to claim 1, further comprising:

a decision circuit (3) for producing an energizing signal (S1, S2) indicating that said battery (1) is to be connected to said solenoid (2) under a prescribed condition, and

wherein said coulomb controlling means (4, 5, 60) comprises:

a power supply voltage monitoring circuit (4) for monitoring the voltage (Vcc) of said battery (1) and producing a signal (V1') corresponding to the battery voltage (Vcc);

an energizing time decision circuit (50) for determining an energizing time (t) in which said solenoid (2) is to be energized, in response to said energizing signal (S1, S2) from said decision circuit (3) and said signal (V1') corresponding to said battery voltage from said power supply voltage monitoring circuit (4); and

a drive circuit (51, 52, 60) for connecting said battery (1) to said solenoid (2) to energize said solenoid (2) for said determined energizing time (t).



7. A solenoid valve control circuit 7 according to any preceding claim wherein said decision circuit (3) comprises a timer circuit (305) for producing a time-out signal (T_o) to stop the generation of said energizing signal (S_1 , S_2) when said de-energizing signal (S_3) is not produced upon elapse of a predetermined period of time ($> T_b$) after said energizing signal (S_1 , S_2) has been produced.
8. A solenoid valve control circuit 7 according to claim 7, wherein said decision circuit (3) further comprises a retry commander (306) for producing a retry signal (Re) to generate said energizing signal (S_1 , S_2) once more when said time-out signal (T_o) is produced by said timer circuit (305).
9. A solenoid valve control circuit 7 according to claim 8, wherein said decision circuit (3) further comprises a failure determining circuit (310 - 318) for producing a failure signal (Tr) to stop controlling said solenoid (2) when said de-energizing signal (S_3) is not produced upon elapse of a predetermined period of time ($> T_b$) after said energizing signal (S_1 , S_2) has been produced again based on said retry signal (Re).
10. A solenoid valve control circuit 7 according to claim 9, wherein said failure determining circuit (310 - 318) comprises a valve closing override circuit (312, 316 - 318) for forcibly closing said valve, and a trouble display circuit (314) for indicating a failure condition.
11. A solenoid valve control circuit 7 according to any of claims 2 to 7, wherein said decision circuit (3) further comprises a failure determining circuit (304 - 318) for producing a failure signal (Tr) to stop con-

Revised and amended sheet



23 AUG 1999

trolling said solenoid (2) when said de-energizing signal (53) is not produced upon elapse of a predetermined period of time after said energizing signal (S1, S2) has been produced.

12. A solenoid valve control circuit (400) according to any preceding claim, further comprising:
 - a voltage drop detecting circuit (401, 402, 403, 404) for detecting a drop in the voltage (V_{cc}) of said battery (1) below a predetermined value (V_{th}) and for producing a voltage drop signal (S5) indicative of the detected voltage drop.
13. A solenoid valve control circuit (500) according to any preceding claim, further comprising a counting circuit (501, 502, 503) for detecting that the number of times said solenoid (2) is energized by said battery (1) exceeds a predetermined number and for producing a voltage drop signal (S5) indicative of the detected number of times.



This is the replacement sheet

Date:

21 Aug 1999

117

FIG. 1

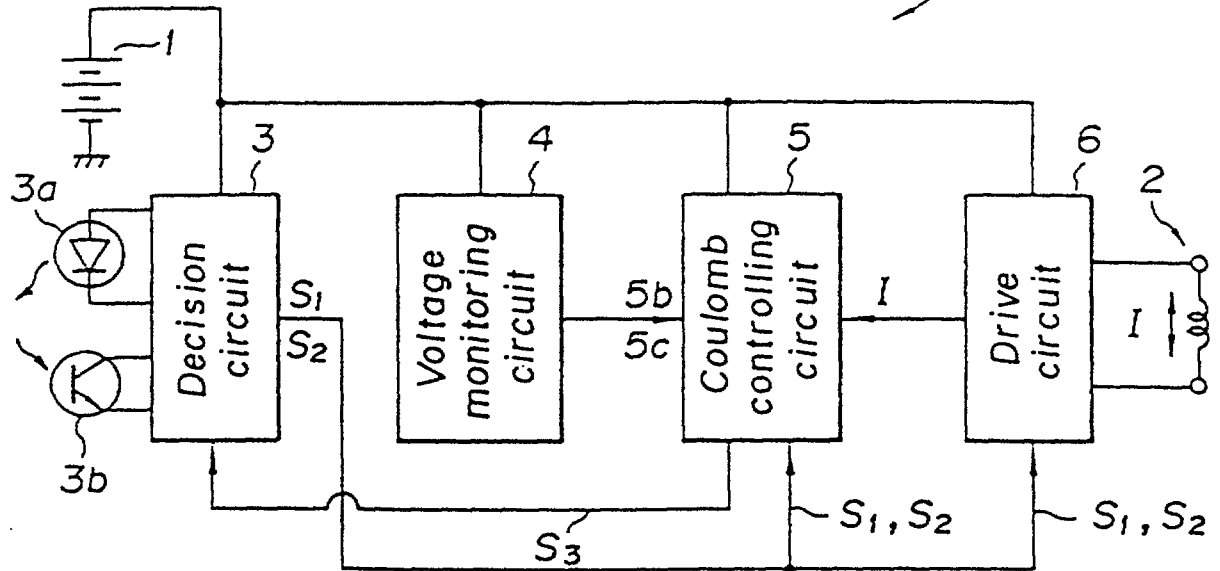


FIG. 4A

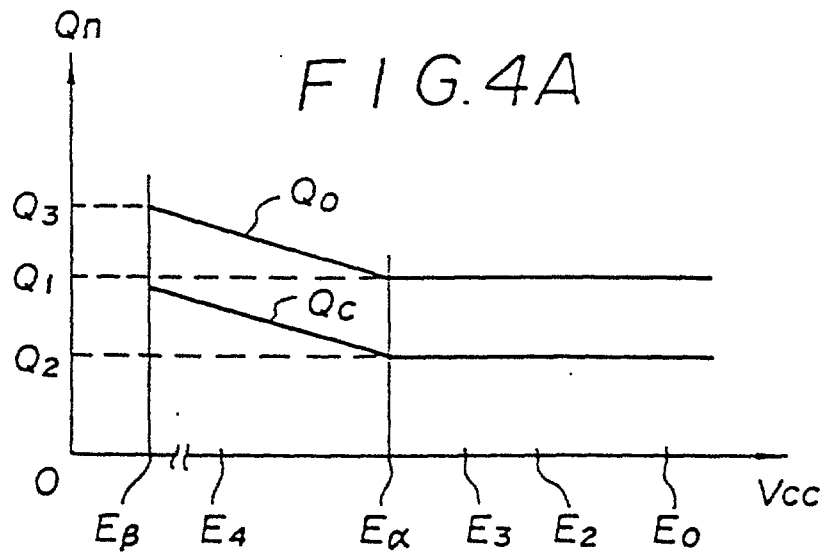


FIG. 4B

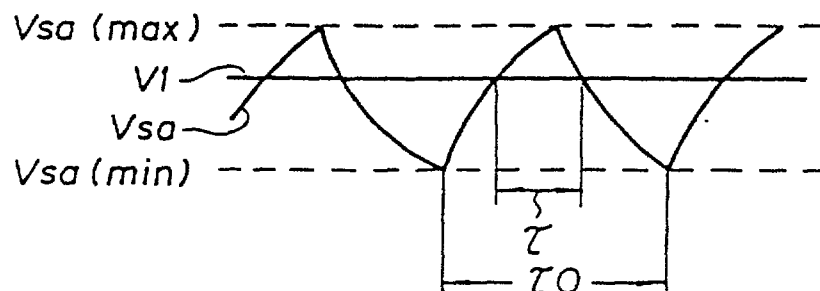
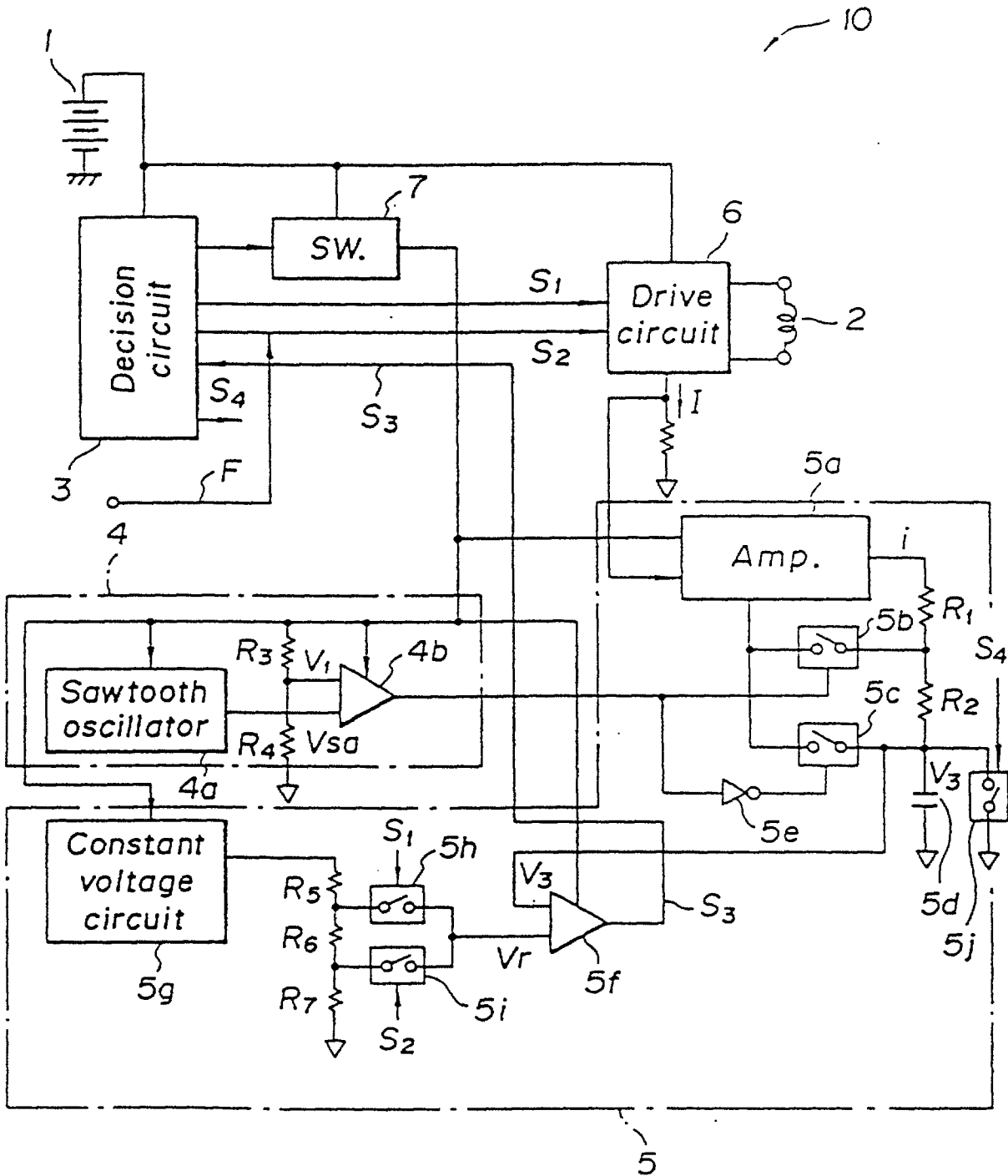
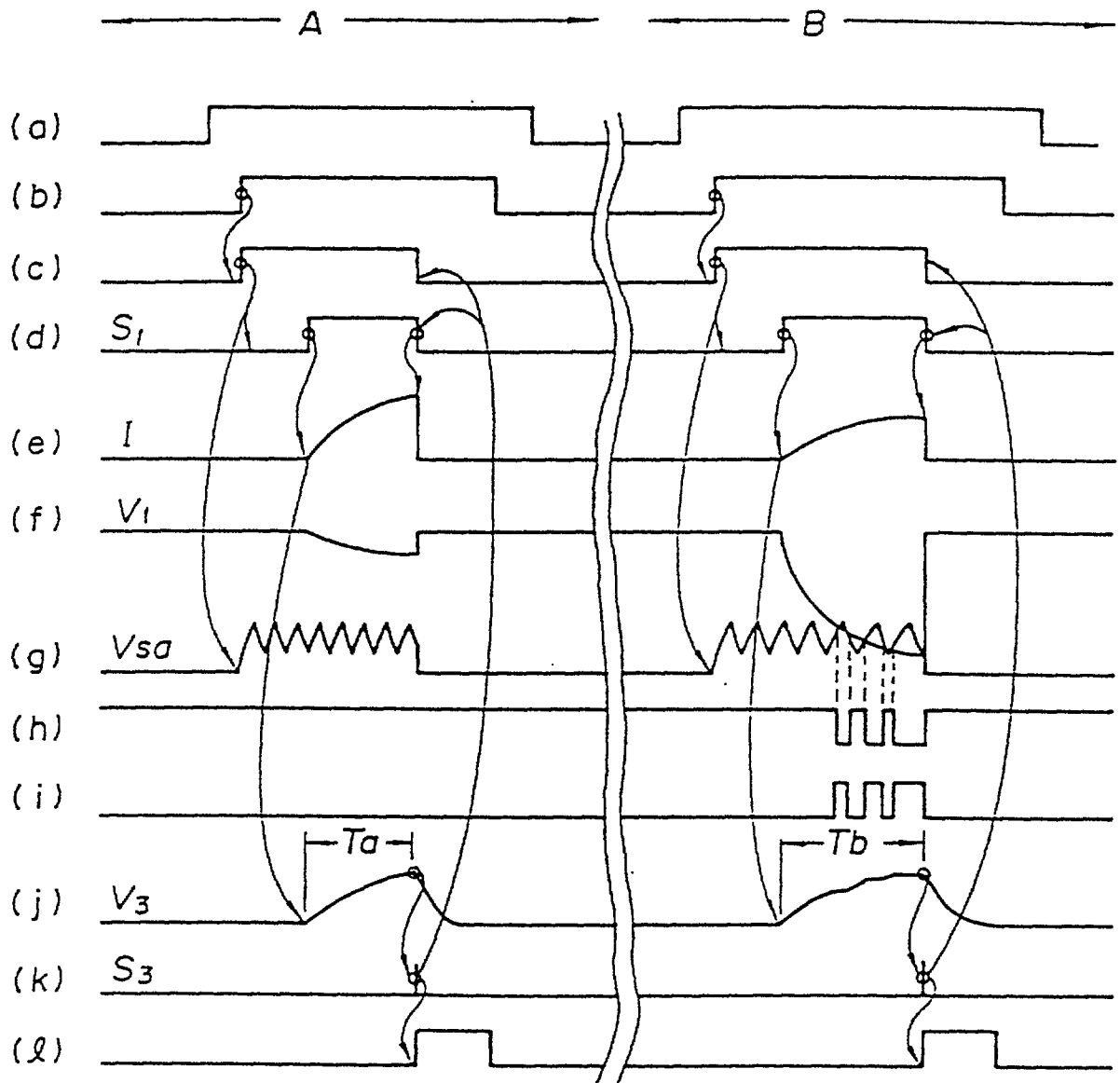


FIG. 2



3/7

FIG. 3



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Date:

21 Aug 1999

417

FIG. 5

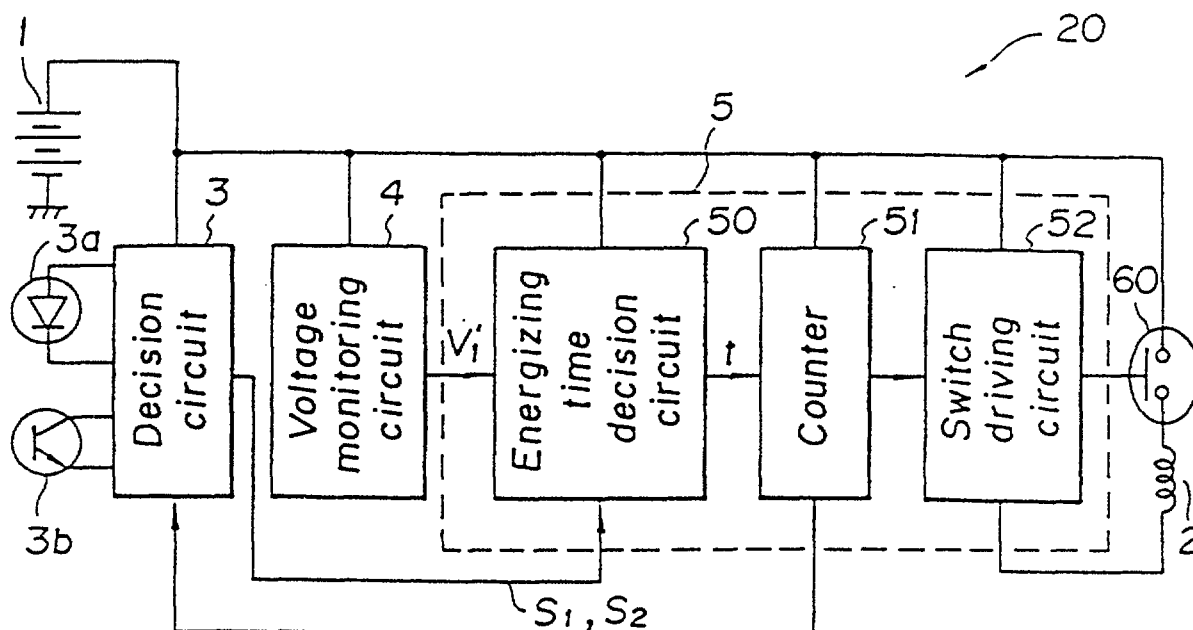
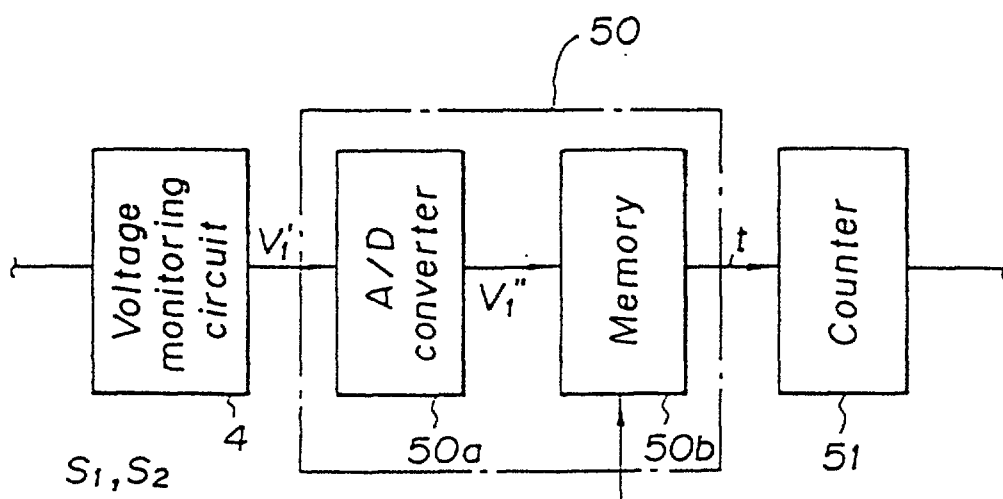


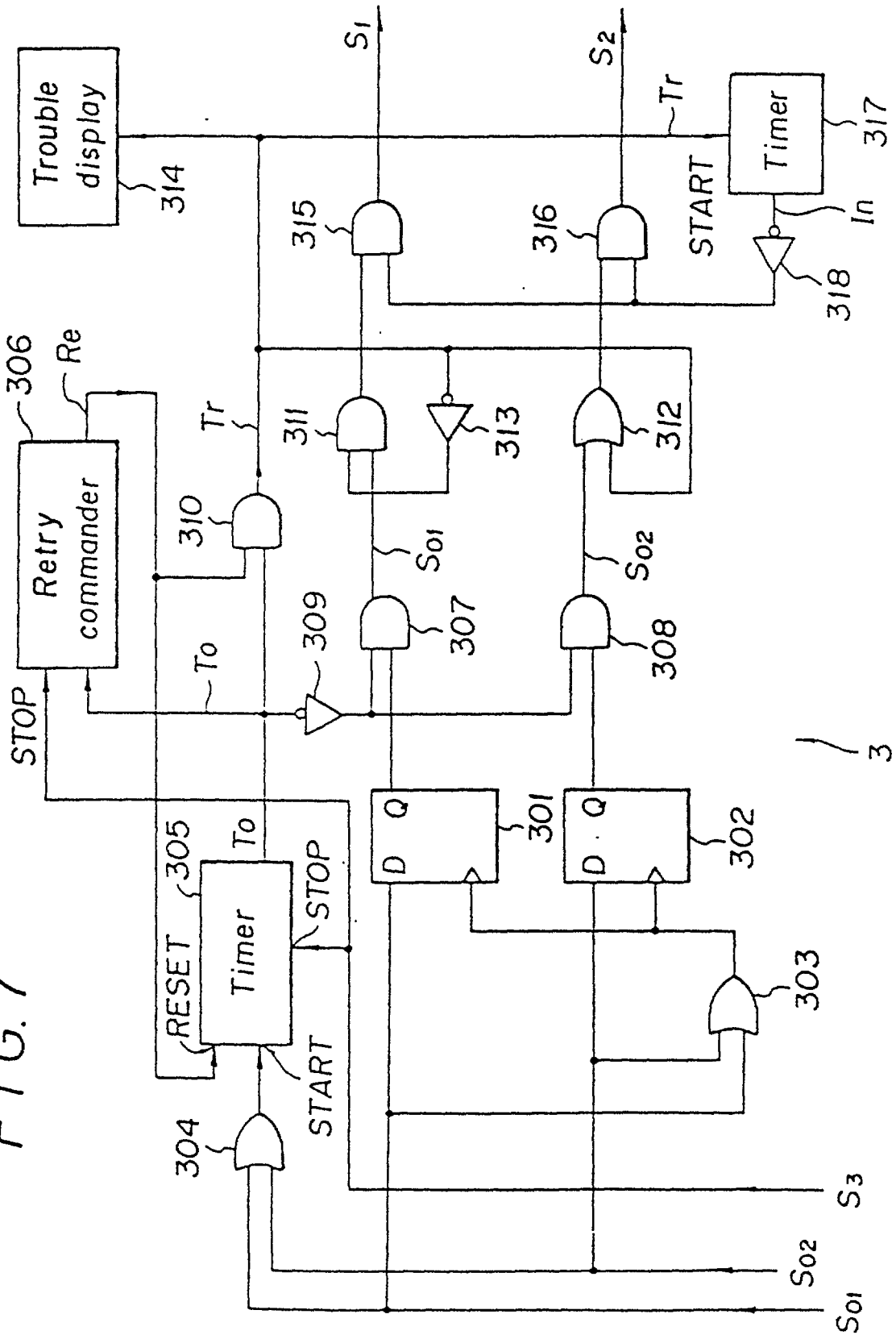
FIG. 6



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23 AUG 1999

FIG. 7



6/7

FIG. 8

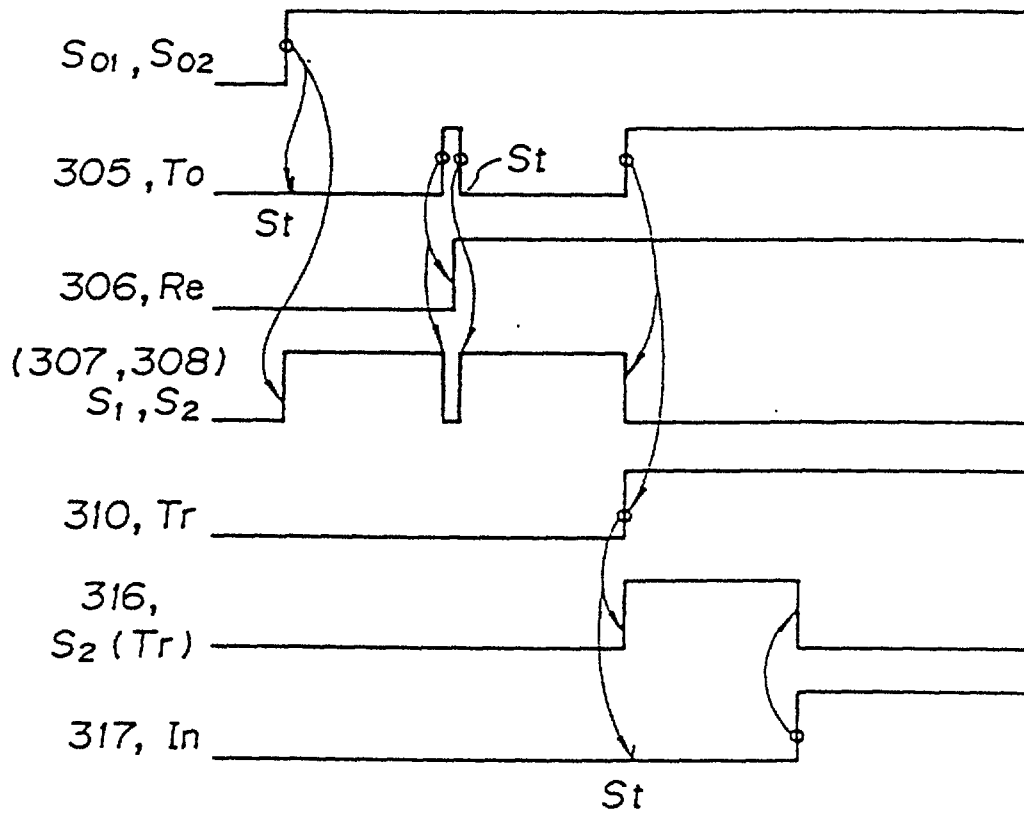


FIG. 9

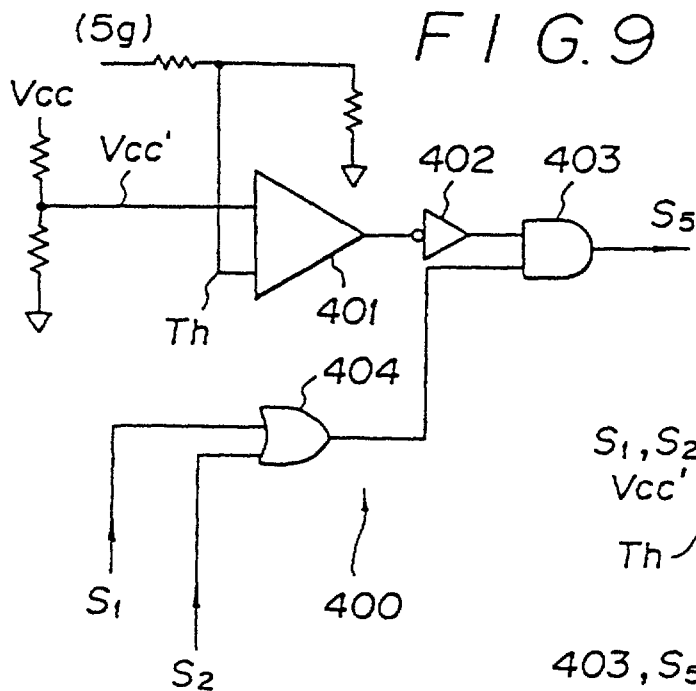
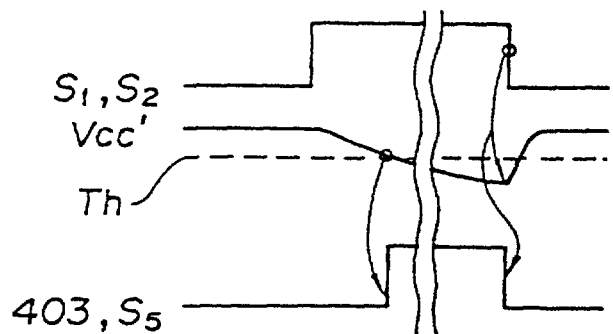


FIG. 10



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2000 AUG 10

FIG. 11

Diagram illustrating a digital circuit (FIG. 11) for generating a sequence of numbers. The circuit includes an AND gate (501) receiving inputs S_1 and S_2 (labeled 5g). The output of the AND gate is connected to a Counter (502). The Counter outputs are connected to a Digital comparator (503). The Digital comparator has a feedback input J connected to its output S_6 . The entire circuit is labeled 500.

Date: 23 AUG 1999