

CLAIMS:

1. A method of forming a Light Emitting Diode (LED) precursor comprising:
 - (a) forming a first semiconducting layer on a substrate, forming the first
5 semiconducting layer comprising:
 - forming a first semiconducting sublayer comprising a Group III-nitride having a first in-plane lattice constant on a surface of the substrate; and
 - forming a strained sublayer comprising a Group III-nitride on the first
10 semiconducting sublayer on an opposite side of the first semiconducting sublayer to the substrate, wherein the strained sublayer at the interface between the strained sublayer and the first semiconducting sublayer is under compressive strain such that an in-plane lattice constant of the strained sublayer at the interface is the first in-plane lattice constant;
 - (b) selectively removing a portion of the first semiconducting layer to expose a bulk
15 semiconducting layer surface of the first semiconducting layer such that the first semiconductor layer defines a mesa structure extending from the bulk semiconducting layer surface;
 - (c) heating the strained sublayer to a strain relaxing temperature, wherein the strained sublayer relaxes through plastic deformation to form a strain relaxed sublayer,
20 wherein the mesa structure has a mesa surface formed from a portion of the strain relaxed sublayer having a second in-plane lattice constant which is larger than the first in-plane lattice constant;
 - (d) forming a monolithic LED structure on the first semiconducting layer such that the monolithic LED structure covers the mesa surface and the bulk semiconducting
25 surface, the monolithic LED structure comprising a plurality of Group III-nitride layers, the monolithic LED structure having:
 - a first monolithic LED structure portion provided over the mesa surface; and
 - a second monolithic LED structure portion encircling the first monolithic LED structure portion and having an inclined sidewall surface relative to the mesa surface.
- 30 2. A method according to claim 1, wherein selectively removing a portion of the first semiconducting layer includes removing a portion of the strained sublayer through a thickness of the strained sublayer and a corresponding portion of the first semiconducting sublayer, such that the bulk semiconducting layer surface is formed in the first
35 semiconducting sublayer.

- 3 A method according to claim 1 or claim 2, wherein the strained sublayer comprises $\text{In}_x\text{Ga}_{1-x}\text{N}$, where $0 < X \leq 1$.
- 5 4. A method according to claim 3, wherein the strained sublayer comprises a plurality of layers, alternating between a first strain layer comprising GaN and a second strain layer comprising $\text{In}_x\text{Ga}_{1-x}\text{N}$, where $0 < X \leq 1$.
- 10 5. A method according to claim 3 or claim 4, wherein In content (X) of the strained sublayer decreases in the thickness direction away from the first semiconducting sublayer.
6. A method according to any preceding claim, wherein the monolithic LED structure comprises:
- 15 a second semiconducting layer provided over the mesa surface and the bulk semiconducting layer surface of the first semiconducting layer;
- 20 an active layer comprising a plurality of Group III nitride layers provided on the second semiconducting layer;
- 20 a p-type semiconducting layer comprising a Group III nitride formed on the active layer.
7. A method according to claim 6, wherein the second semiconducting layer comprises GaN, or $\text{In}_Y\text{Ga}_{1-Y}\text{N}$, where $0 < Y \leq 1$.
- 25 8. A method according to claim 6 or claim 7, wherein the active layer is configured to output light having a wavelength of at least 500 nm.
9. A method according to any of claims 6 to 8, wherein the active layer comprises at least one quantum well layer comprising $\text{In}_Z\text{Ga}_{1-Z}\text{N}$ having a third in-plane lattice constant which is at least equal to the second in-plane lattice constant, where $0 < Z \leq 1$.
- 30 10. A method according to any of claims 6 to 9, wherein
- 35 a potential barrier is provided between a first portion of the p-type semiconducting layer covering the mesa surface and a second portion of the p-type semiconducting layer covering the bulk semiconducting surface, the potential barrier surrounding the first portion of the p-type semiconducting layer covering the mesa surface.

11. A method according to any preceding claim, wherein the strain relaxing temperature is at least 800 °C.
- 5 12. A Light Emitting Diode (LED) precursor comprising:
a first semiconducting layer comprising Group III-nitrides, the first semiconducting layer including a mesa structure extending from a major surface of the first semiconducting layer to define a growth surface including a bulk semiconductor surface and a mesa surface, wherein the first semiconducting layer comprises:
- 10 a first semiconducting sublayer comprising a Group III-nitride having a first in-plane lattice constant; and
a strain relaxed sublayer comprising a Group III-nitride provided across the first semiconducting sublayer, wherein the strain relaxed sublayer provides the mesa surface of the mesa structure, the mesa surface having a second in-plane
- 15 lattice constant which is larger than the first in-plane lattice constant; and
a monolithic LED structure provided on the growth surface of the first semiconducting layer such that the monolithic LED structure covers the mesa surface and the bulk semiconducting surface, the monolithic LED structure comprising a plurality of Group III-nitride layers, the monolithic LED structure having:
- 20 a first monolithic LED structure portion provided over the mesa surface; and
a second monolithic LED structure portion encircling the first monolithic LED structure portion and having an inclined sidewall surface relative to the mesa surface.
13. A method of forming a LED array precursor comprising:
- 25 (a) forming a first semiconducting layer on a substrate, forming the first semiconducting layer comprising:
forming a first semiconducting sublayer comprising a Group III-nitride having a first in-plane lattice constant on a surface of the substrate; and
forming a strained sublayer comprising a Group III-nitride on the first
- 30 semiconducting sublayer on an opposite side of the first semiconducting sublayer to the substrate, wherein the strained sublayer at the interface between the strained sublayer and the first semiconducting sublayer is under compressive strain such that an in-plane lattice constant of the strained sublayer at the interface is the first in-plane lattice constant;

(b) selectively removing a portion of the first semiconducting layer to expose a bulk semiconducting layer surface of the first semiconducting layer such that the first semiconductor layer defines a plurality of mesa structures each extending from the bulk semiconducting layer surface,

5 (c) heating the strained sublayer to a strain relaxing temperature, wherein the strained sublayer relaxes through plastic deformation to form a strain relaxed sublayer wherein each mesa structure has a mesa surface formed from a portion of the strain relaxed sublayer having a second in-plane lattice constant which is larger than the first in-plane lattice constant;

10 (d) forming a monolithic LED structure on the first semiconducting layer such that the monolithic LED structure covers the mesa surfaces and the bulk semiconducting surface, the monolithic LED structure comprising a plurality of Group III-nitride layers, the monolithic LED structure having:

a plurality of first monolithic LED structure portions, each first monolithic LED
15 structure portion provided over a respective mesa surface; and
a plurality of second monolithic LED structure portions, each second monolithic LED structure portion encircling a first monolithic LED structure portion and having an inclined sidewall surface relative to the respective mesa surface.

20 14. A LED array precursor comprising:

a first semiconducting layer including a plurality of mesa structures, each mesa structure extending from a major surface of the first semiconducting layer to define a growth surface including a bulk semiconductor surface and a plurality of mesa surfaces, wherein the first semiconducting layer comprises:

25 a first semiconducting sublayer comprising a Group III-nitride having a first in-plane lattice constant; and

a strain relaxed sublayer comprising a Group III-nitride provided across the first semiconducting sublayer, wherein the strain relaxed sublayer provides the mesa surface of each mesa structure, the mesa surface having a second in-plane
30 lattice constant which is larger than the first in-plane lattice constant; and

a monolithic LED structure provided on the growth surface of the first semiconducting layer such that the monolithic LED structure covers each mesa surface and the bulk semiconducting surface, the monolithic LED structure comprising a plurality of Group III-nitride layers, the monolithic LED structure having:

a plurality of first monolithic LED structure portions, each first monolithic LED structure portion provided over a respective mesa surface; and

5 a plurality of second monolithic LED structure portions, each second monolithic LED structure portion encircling a first monolithic LED structure portion and having an inclined sidewall surface relative to the respective mesa surface.