INTEGRATED CIRCUITS HAVING PLACE-EFFICIENT CAPACITORS AND METHODS FOR FABRICATING THE SAME

ABSTRACT OF THE INVENTION

Integrated circuits having place-efficient capacitors and methods for fabricating the same are provided. A dielectric layer is formed overlying a conductive feature on a semiconductor substrate. A via opening is formed into the dielectric layer to expose a portion of the conductive feature. A partial opening is etched into the dielectric layer and positioned over the conductive feature. Etch resistant particles are deposited overlying the dielectric layer and in the partial opening. The dielectric layer is further etched using the etch resistant particles as an etch mask to extend the partial opening. A first conductive layer is formed overlying the extended partial opening and electrically contacting the conductive feature. A capacitor insulating layer is formed overlying the first conductive layer. A second conductive layer is formed overlying the insulating layer.

Figure 1