

PATENT SPECIFICATION

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(54) ELECTRONIC TIMEPIECE

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese company of 3—4, 4-Chome, Ginza, Chuo-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electronic timepieces.

According to the present invention there is provided an electronic timepiece comprising an oscillator circuit for producing a relatively high frequency standard time signal, a divider circuit having a plurality of divider stages for dividing the frequency of the standard time signal to produce signals from which a display of a time indication is produced, and varying means for selectively varying the dividing ratio of the divider circuit by changing the phase of an output signal from at least one divider stage.

Said varying means may include an exclusive OR gate. Alternatively said varying means may include an integrating circuit.

An electronic timepiece may include a signal-composing circuit arranged so that the phase of said output signal from said at least one divider stage is delayed in synchronism therewith.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:—

Figure 1 illustrates, in block diagram form, a conventional electronic timepiece;

Figure 2 illustrates, in block diagram form, a divider circuit of an electronic timepiece according to the present invention;

Figure 3 is a circuit diagram of a signal-composing circuit which forms part of the electronic timepiece of Figure 2;

Figure 4 illustrates graphically the operation of the signal-composing circuit of Figure 3;

Figure 5 illustrates graphically the waveform of output signals that can be obtained from the signal-composing circuit of Figure 3;

Figure 6 illustrates a practical way of effecting frequency regulation in an electronic time-

piece according to the present invention;

Figure 7 illustrates another embodiment of an electronic timepiece according to the present invention;

Figure 8 illustrates a further embodiment of an electronic timepiece according to the present invention;

Figure 9 illustrates graphically the operation of the electronic timepiece of Figure 8;

Figure 10 illustrates a yet further embodiment of an electronic timepiece according to the present invention;

Figure 11 illustrates graphically the operation of the electronic timepiece of Figure 10; and

Figure 12 is a circuit diagram of an exclusive OR gate for use with an electronic timepiece according to the present invention.

A conventional electronic timepiece is illustrated in Figure 1 and comprises an oscillator circuit 1 for generating a standard time signal, a divider circuit 2 for producing from the relative high frequency standard time signal a relatively low frequency signal, for example, having a frequency of 1 Hz, and a display device 3 driven by outputs of the divider circuit to display a time indication. The oscillator circuit 1 and/or the divider circuit 2 may be of C—MOS integrated circuitry. A quartz crystal oscillator 4 is used as a time standard in the oscillator circuit 1 since it has a relatively high stability. However, in mass produced quartz crystal oscillators, a substantial deviation of the actual frequency of vibration from a predetermined frequency of vibration occurs. Thus it is necessary to tune the quartz crystal vibrator so that the actual frequency vibration substantially coincides with the predetermined frequency of vibration. A rough tuning is effected by altering the shape or size of the quartz crystal vibrator itself or the electrodes thereof. The actual frequency vibration is made substantially equal to the predetermined frequency vibration by a trimmer capacitor 5. Conventionally the trimmer capacitor 5 is such that it can vary the actual frequency of vibration of the quartz crystal vibrator by up to 1Hz assuming that the desired frequency vibra-

12

tion is 32.76 KHz. Accordingly, if the actual frequency of vibration of the vibrator is not within 0.5 HZ of the desired frequency of 32.768KHz, the quartz crystal vibrator cannot be sufficiently accurately tuned for it to be of use in an electronic timepiece. However, to tune quartz crystal vibrators within a range of 0.5Hz is difficult and costly from a manufacturing point of view.

The present invention seeks to avoid these disadvantages of known electronic timepieces by varying the division ratio of the divider circuit so that tuning of the quartz crystal vibrator can be avoided. It is, therefore, possible in principal to change the effective frequency of the quartz crystal vibrator by between 0% and 50%.

Figure 2 shows a divider circuit of an electronic timepiece according to the present invention, the divider circuit being of the master-slave type and having $n+k$ divider stages $F_1, F_2, \dots, F_{k+n}$. An output signal ϕ_{i-1} from the divider stage F_{i-1} , that is to say the output signal which, in a conventional divider circuit, is the input signal to the divider stage F_i is phase advanced by 180° by means of a phase advancing circuit 6, which produces an output signal ϕ_{i-1}^* . The number of times the phase advancing operation is performed within a predetermined period of time is determined by an output signal C_{out} of a signal-composing circuit 7 which selectively feeds output signals ϕ_k to ϕ_{k+n} from divider stages F_k to F_{k+n} respectively to the phase advancing circuit 6 under the control of a selection control input signal C_{in} .

Figure 3 is a circuit diagram of the signal-composing circuit 7, the input signal C_{in} consisting of input signals $C_{in1}, C_{in2}, \dots, C_{inn}$. Figure 4 illustrates graphically the operation of the signal-composing circuit 7. The phase advancing operation is performed in the phase advancing circuit 6 by an exclusive OR gate (hereinafter referred to as "EX-OR"). An output signal C_{out} , i.e. any of the output signals ϕ_k to ϕ_{k+n} is, in theory, inevitably synchronous with the output signal ϕ_{i-1} from the divider stage F_{i-1} at time T_i . However, in practice, there is a time retardation T_D proportional to the number of divider stages following the divider stage F_i . Namely, if the time retardation per divider stage is τ_D , then for the output signal ϕ_{k+i} , the time retardation T_D is:

$$(k-i+1) \cdot \tau_D,$$

the time retardation is the signal-composing circuit 7 being ignored. Due to the time retardation T_D , the phase advancing operation is performed with the timing shown in Figure 4. Namely, the phase is advanced by 180° with each rise or fall of the output signal C_{out} of the signal-composing circuit 7. Accordingly,

if the frequency of the output signal ϕ_{i-1} is f , a change in frequency of

$$\frac{1}{2f}$$

is observed on the output side of the divider.

The number of times the phase advancing operation is performed is determined by the signal-composing circuit 7. When the input signal C_{in} is HIGH, the output signals ϕ_k to ϕ_{k+n} of the divider stages F_k to F_{k+n} are passed to the phase advancing circuit but not when the input signal C_{in} is LOW. Assuming that each of the divider stages F_k to F_{k+n} are one half divider circuits, only the output signal ϕ_{k+n} of the divider stage F_{k+n} is passed for a period T_B by the signal-composing circuit 7 so that the output signal C_{out} is composed of one cycle of the output signal ϕ_{k+n} occurring within the period T_B . The frequency changes, therefore:

$$\frac{1}{2f} \times 2$$

Similarly, when the output signal ϕ_{k+n-1} from the divider stage F_{k+n-1} is passed by the signal-composing circuit 7, the output signal C_{out} is composed of the two cycles of the output signal ϕ_{k+n-1} within the period T_B so that the frequency change is:

$$\frac{1}{2f} \times 4$$

Thus when the output signal ϕ_k from the divider stage F_k is passed by the signal composing circuit 7, the output signal is composed of n cycles of the output signal ϕ_k within the period T_B so that the frequency changes:

$$\frac{1}{2f} \times 2^{(n+1)}$$

Thus a frequency change between 0 and 1

$$\frac{1}{2f} \times 2^{(n+1)}$$

can be selected successively at intervals of

$$\frac{1}{2f} \times 2$$

within the period T_B . As an example, Figure 5 shows the output signals C_{out} from the signal-composing circuit 7 when

the output signal ϕ_{k+1} and ϕ_{k+2} from the divider stages F_{k+1} and F_{k+2} respectively are passed thereby.

For example, assuming that the frequency of the phase-advanced signal is 8.192 KHz, the advance of timing will be:

$$\frac{1}{2 \times 8.192 \times 10^{-3}} = 60 \text{ (}\mu\text{sec)}$$

and this is equivalent to 5.2 seconds per day ($60 \mu\text{sec} \times 86400$). This corresponds to a half period. Further assuming that the period of the output signals ϕ_k , ϕ_{k+1} and ϕ_{k+2} of the respective divider stages F_k , F_{k+1} and F_{k+2} are one second, two seconds and four seconds respectively, results show in the following table are obtained. Thus it is possible to regulate the effective frequency of the quartz crystal vibrator to alter the rate of the electronic timepiece by nearly 20 seconds per day.

step	passing signal	Amount of advance (second/day)
1	0	0
2	ϕ_{k+2}	about 2.6
3	ϕ_{k+1}	„ 5.2
4	$\phi_{k+1} + \phi_{k+2}$	„ 7.8
5	ϕ_k	„ 10.4
6	$\phi_k + \phi_{k+2}$	„ 13.0
7	$\phi_k + \phi_{k+1}$	„ 15.6
8	$\phi_k + \phi_{k+1} + \phi_{k+2}$	„ 18.2

Thus assuming that a standard time signal having an effective frequency of 32.768 KHz is desired, a deviation from this of nearly 7.7 Hz (0.023%) can be corrected. After rough regulation by selecting the output signals ϕ_k to ϕ_h to be applied to the signal composing circuit, the rate of the watch may be brought to within less than 2.6 seconds per day of the desired rate and fine tuning is then effected by means of a trimmer capacitor such as that shown in Figure 1.

Figure 6 illustrates a practical way of frequency regulation using the input signal C_m in an electronic timepiece according to the present invention by selection between rails (+) and rails (-) using bonding wires of pads 9 for the input signal C_m mounted on an integrated circuit chip 8.

As mentioned above, it is possible to make a larger variation in the effective divisional ratio of the divider circuit by suitably selecting the frequency of the output signals ϕ_k to ϕ_{k+n} from the divider stages F_k to F_{k+n} . Further, if the interval between steps of variation is reduced it may not be necessary to provide a trimmer capacitor for fine tuning.

Generally, in a divider circuit composed of C-MOS circuitry, the current consumption is

in proportion to the operating frequency. Therefore, if the phase advancing circuit 6 is provided between divider stages operating at a relatively high frequency or indeed directly following the oscillator circuit, there will be an increase in current consumption. Further, when the time retardation T_D of the divider circuit approaches a half period of the operating signal, as seen in Figure 4, an instability is introduced by virtue of change in the supply voltage or the variation of characteristics of circuit components, e.g. transistors etc. In the case of C-MOS circuitry, particularly operating the supply voltage of 1.5 volts, there is a relatively large change in time retardation T_D caused by change of supply voltage or the variation of the characteristics of circuit components e.g. transistors. Accordingly, in the case of a time standard frequency of 32.768 KHz, the phase advancing circuit 6 is best placed between and behind the 8 KHz signal (which is a signal two stages after the one half divider circuit from the point of view of limited increase in current consumption).

The phase control according to the present invention is also available for the data input of the divider circuit. Figure 7 illustrates such an arrangement in a master-slave type divider

having a master 10 and a slave 11.

It will be appreciated that the phase advancing circuit may be replaced by a phase delay circuit which delays the phase of an input signal from one of the divider stages by 180° . If means are provided for performing both a phase advancing operation and phase retarding operation, it becomes possible to regulate the amount of advance or delay determined by the frequency of the quartz crystal vibrator, to zero.

Referring now to Figure 8, an impulse-shaped waveform having a time width T_D (Figure 9) is eliminated by using a transmission gate 12 having an equivalent resistor R and a CR integrating circuit including a capacitor 13. Consequently, a phase delay of 180° is obtained. Since the transmission gate 12 is OFF when a signal S is HIGH by the advance-delay control signal S_{ad} , an integration is not performed so that the output signal ϕ_{i-1}^* is phase advanced by 180° relative to the output signal ϕ_{i-1} . When signal S is LOW, an integration is performed and the output signal ϕ_{i-1}^* is phase delayed by 180° relative to the output signal ϕ_{i-1} . The impulse-shaped wave form can be eliminated stably by suitably selecting the values of the time retardation T_D , the equivalent resistor R to the transmission gate 12 determining the time constant of integration, and the capacitor 13. The integration can be performed by using the output resistor of an inverter which forms the output signal ϕ_{i-1}^* . In this case, since both the phase advance and phase delay operations need not be synchronised with the output signal ϕ_{i-1} , the construction is relatively simple.

Referring now to Figure 10, by applying the output signal C_{out} having a given time retardation to a flip-flop circuit 14, an output signal Q synchronous with the output signal ϕ_{i-1} is obtained. Either this output signal Q or the output signal C_{out} is passed through a selecting circuit 15 by a selecting signal S_{sc} to cause its phase to be advanced or delayed. The passage of the output signal Q causes a phase delay of 180° and the passage of the output signal C_{out} causes a phase advance of 180° , this arrangement being shown in Figure 11.

The present invention relies basically upon altering the effective division ratio of a divider circuit by advancing or delaying by 180° the phase of an output signal from one of the divider stages of the divider circuit. This can be accomplished relatively simply by using an exclusive OR gate of integrated C—MOS circuitry as shown in Figure 12. The phase advancing circuit need not operate

synchronously with the input signals thereto in the sense that the time retardation of the divider circuit it utilized positively, and therefore this phase advancing circuit is relatively simple and may be composed of a single exclusive OR gate.

It is this possible to regulate precisely the output frequency of a divider circuit over a relative wide range. Thus the manufacturing cost of the quartz crystal vibrator of the oscillator circuit can be reduced to half or less. Further, similarly from the viewpoint of the current consumption, since it is possible to select and fix the smallest circuit constant, the oscillator circuit of low current consumption and high stability can be provided.

Since the phase of the output signal of a divider stage is varied by positively utilizing the time retardation present the circuitry used in the present invention is relatively simple. Therefore, to reduce costs monolithic C—MOS integrated circuitry can be used and this is particularly advantageous in the case of electronic wristwatches.

WHAT WE CLAIM IS:—

1. An electronic timepiece comprising an oscillator circuit for producing a relatively high frequency standard time signal, a divider circuit having a plurality of divider stages for dividing the frequency of the standard time signal to produce signals from which a display of a time indication is produced, and varying means for selectively varying the dividing ratio of the divider circuit by changing the phase of an output signal from at least one divider stage.
2. An electronic timepiece as claimed in claim 1 in which said varying means includes an exclusive OR gate.
3. An electronic timepiece as claimed in claim 1 in which said varying means includes an integrating circuit.
4. An electronic timepiece as claimed in any preceding claim including a signal-composing circuit arranged so that the phase of said output signal from said at least one divider stage is delayed in synchronism with a signal from the signal-composing circuit.
5. An electronic timepiece substantially as herein described with reference to and as shown in Figs 2 to 12 of the accompanying drawings.

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3. An electronic timepiece as claimed in claim 1 in which said varying means includes an integrating circuit.

4. An electronic timepiece as claimed in any preceding claim including a signal-composing circuit arranged so that the phase of said output signal from said at least one divider stage is delayed in synchronism with a signal from the signal-composing circuit.

5. An electronic timepiece substantially as herein described with reference to and as shown in Figs 2 to 12 of the accompanying drawings.

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