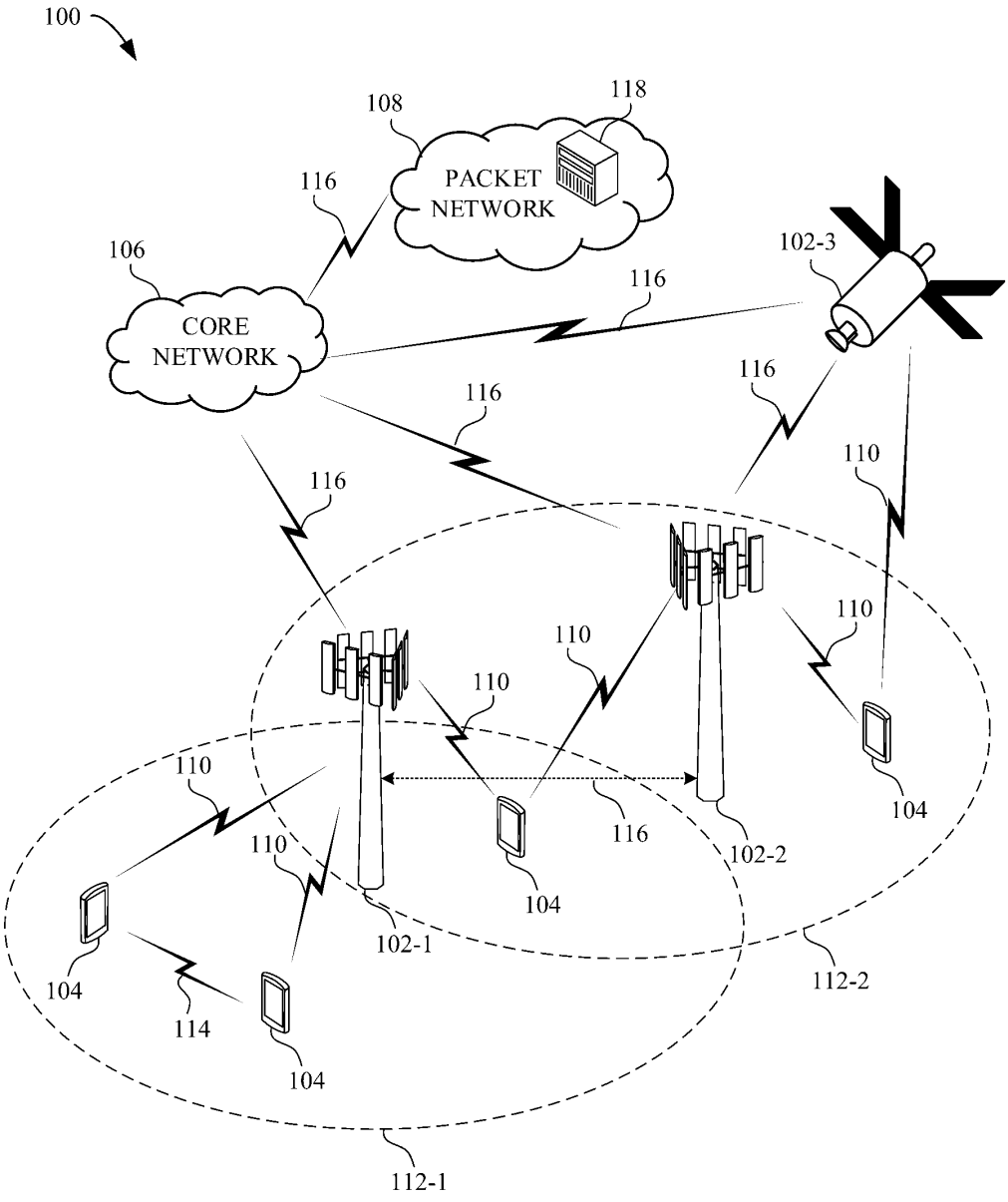

100
108
118
PACKET NETWORK
116
106
CORE NETWORK
102-3
116
116
116
116
110
110
110
110
110
110
110
104
104
104
104
102-1
102-2
116
114
112-1
112-2

FIG. 1

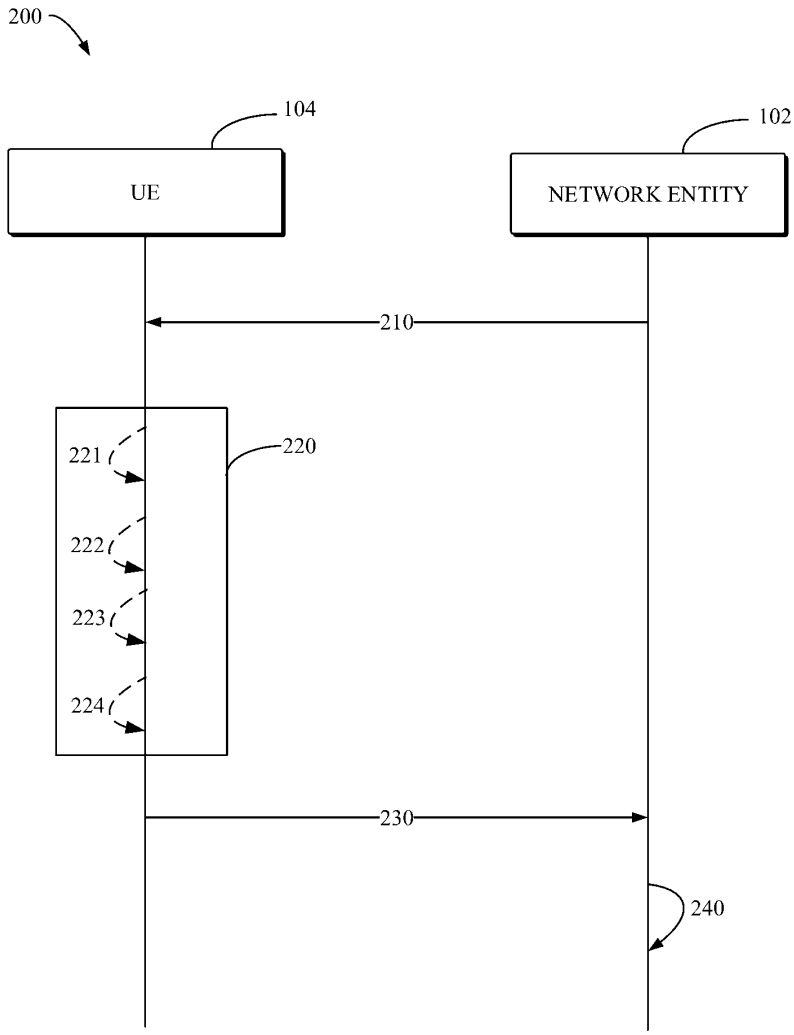


FIG. 2

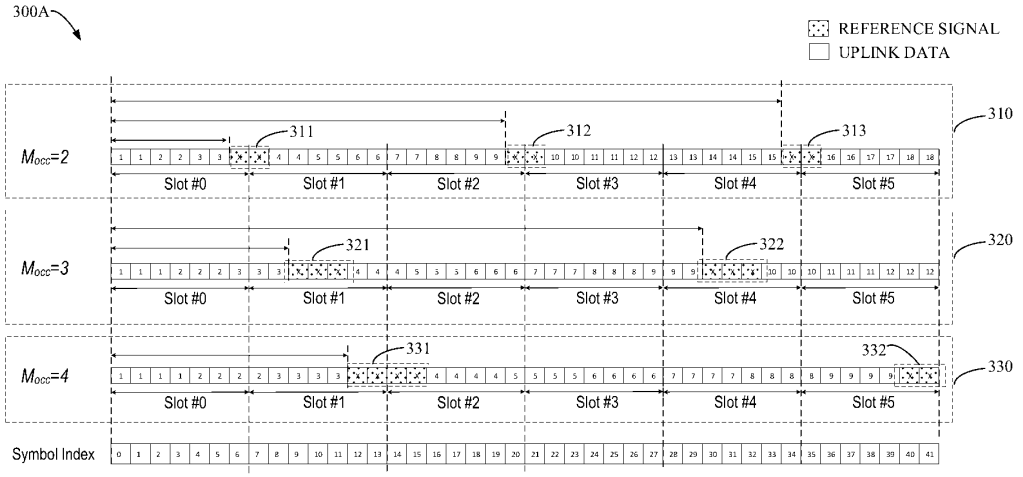

300A
REFERENCE SIGNAL
UPLINK DATA
310
311
312
313
M_{occ}=2
Slot #0
Slot #1
Slot #2
Slot #3
Slot #4
Slot #5
320
321
322
M_{occ}=3
330
331
332
M_{occ}=4
Symbol Index

FIG. 3A

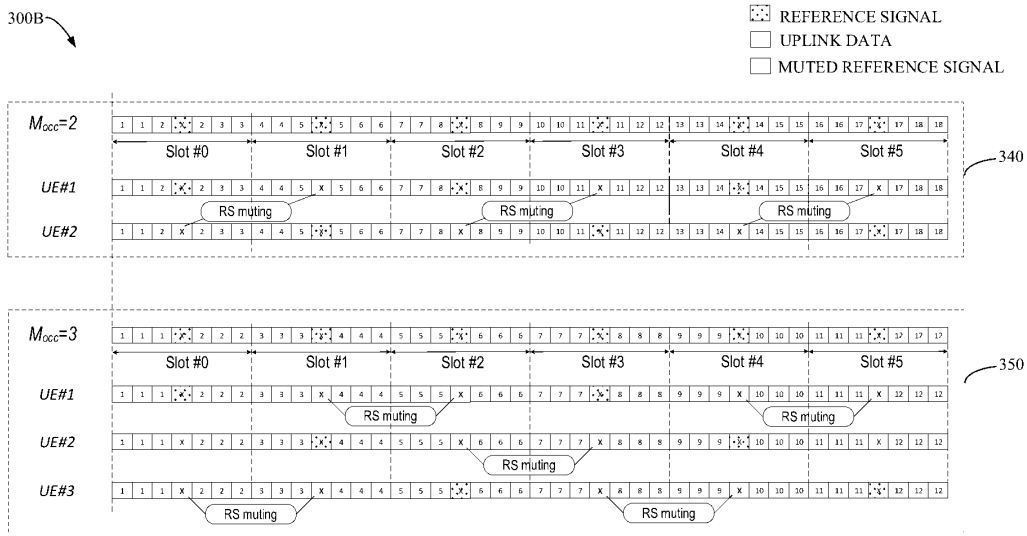

300B
REFERENCE SIGNAL
UPLINK DATA
MUTED REFERENCE SIGNAL
M_{occ}=2
Slot #0
Slot #1
Slot #2
Slot #3
Slot #4
Slot #5
340
UE#1
UE#2
RS muting
M_{occ}=3
350
UE#3

FIG. 3B

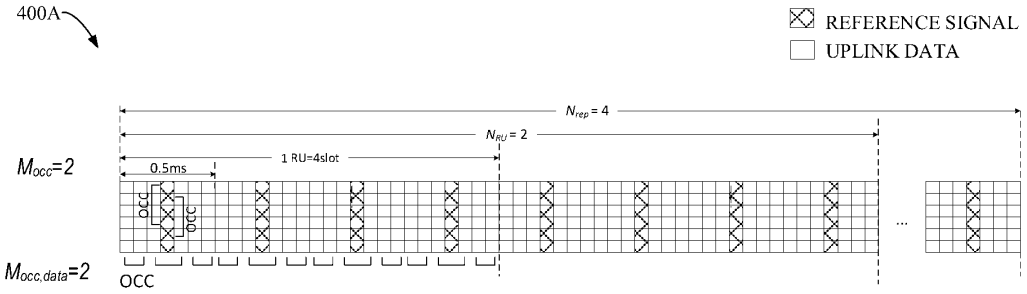


FIG. 4A

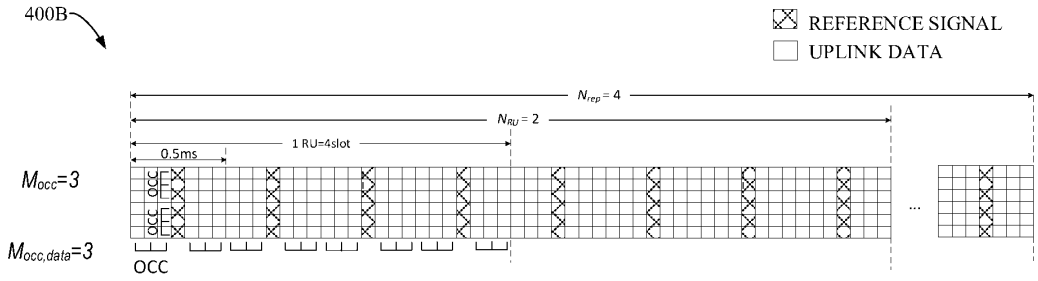


FIG. 4B

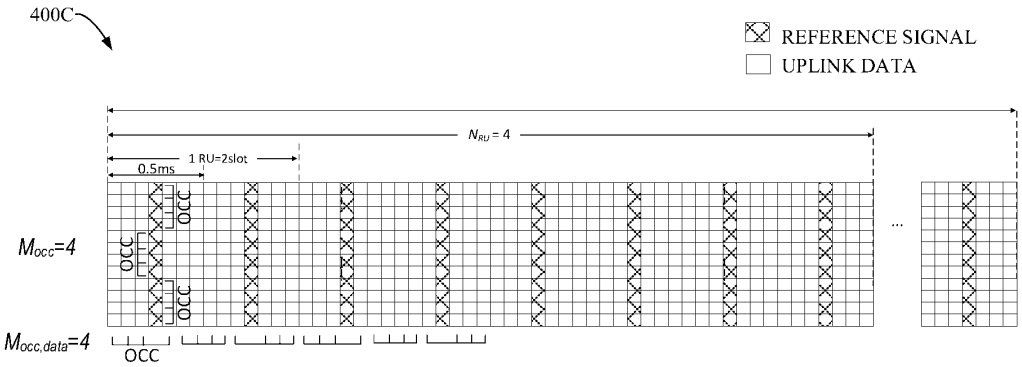


FIG. 4C

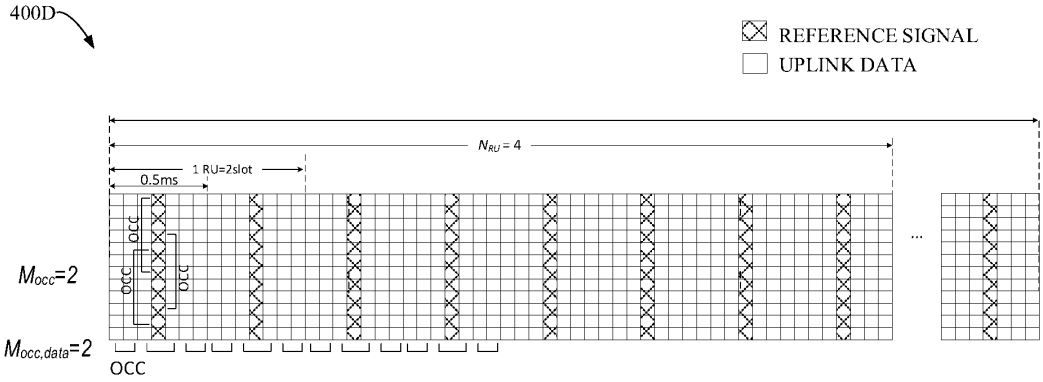

400D
REFERENCE SIGNAL
UPLINK DATA
N_{RU} = 4
1 RU=2slot
0.5ms
OCC
OCC
OCC
M_{occ}=2
$M_{occ,data}$=2
OCC

FIG. 4D

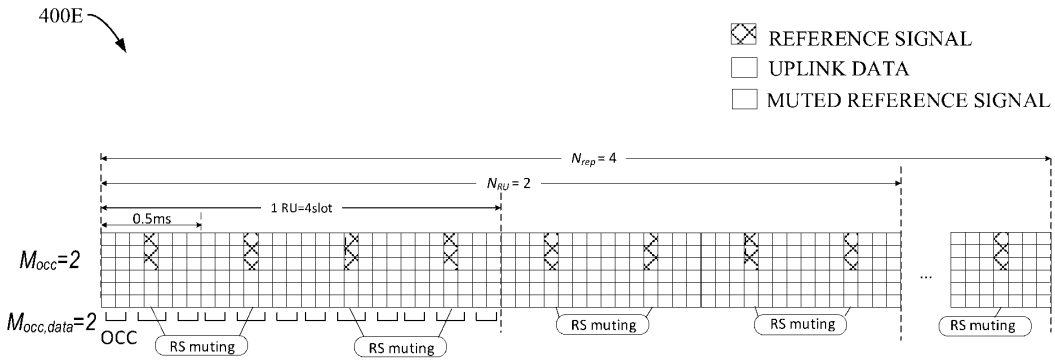

400E
REFERENCE SIGNAL
UPLINK DATA
MUTED REFERENCE SIGNAL
N_{rep} = 4
N_{RU} = 2
1 RU=4slot
0.5ms
M_{occ}=2
$M_{occ,data}$=2
OCC
RS muting
RS muting
RS muting
RS muting
RS muting

FIG. 4E

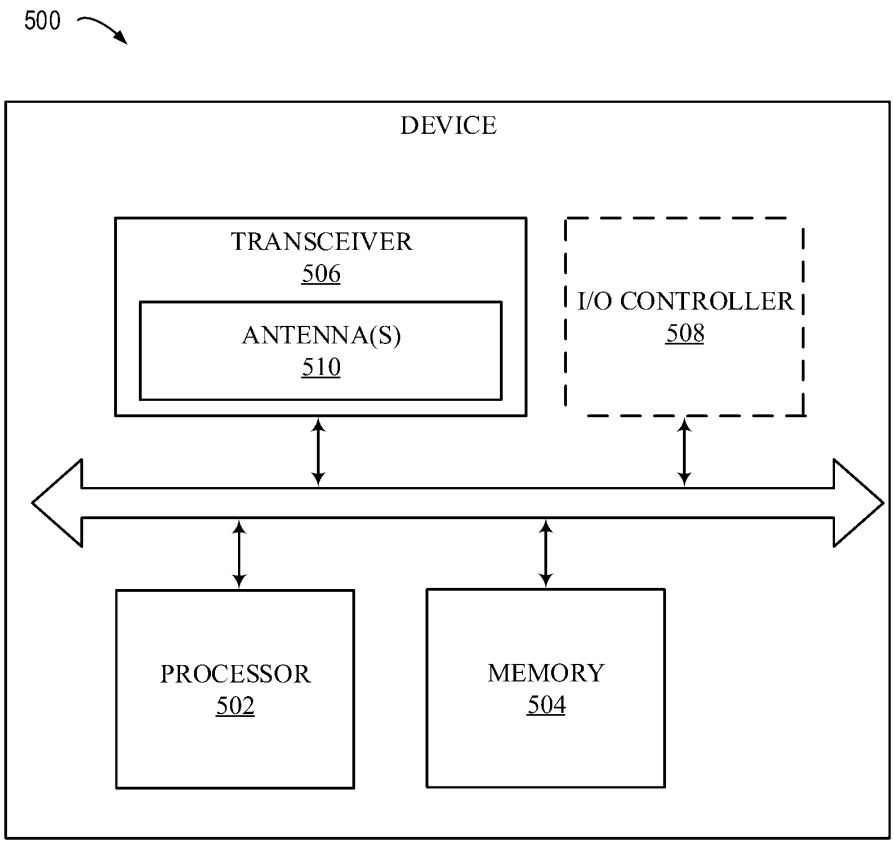

500
DEVICE
TRANSCEIVER
506
ANTENNA(S)
510
I/O CONTROLLER
508
PROCESSOR
502
MEMORY
504

FIG. 5

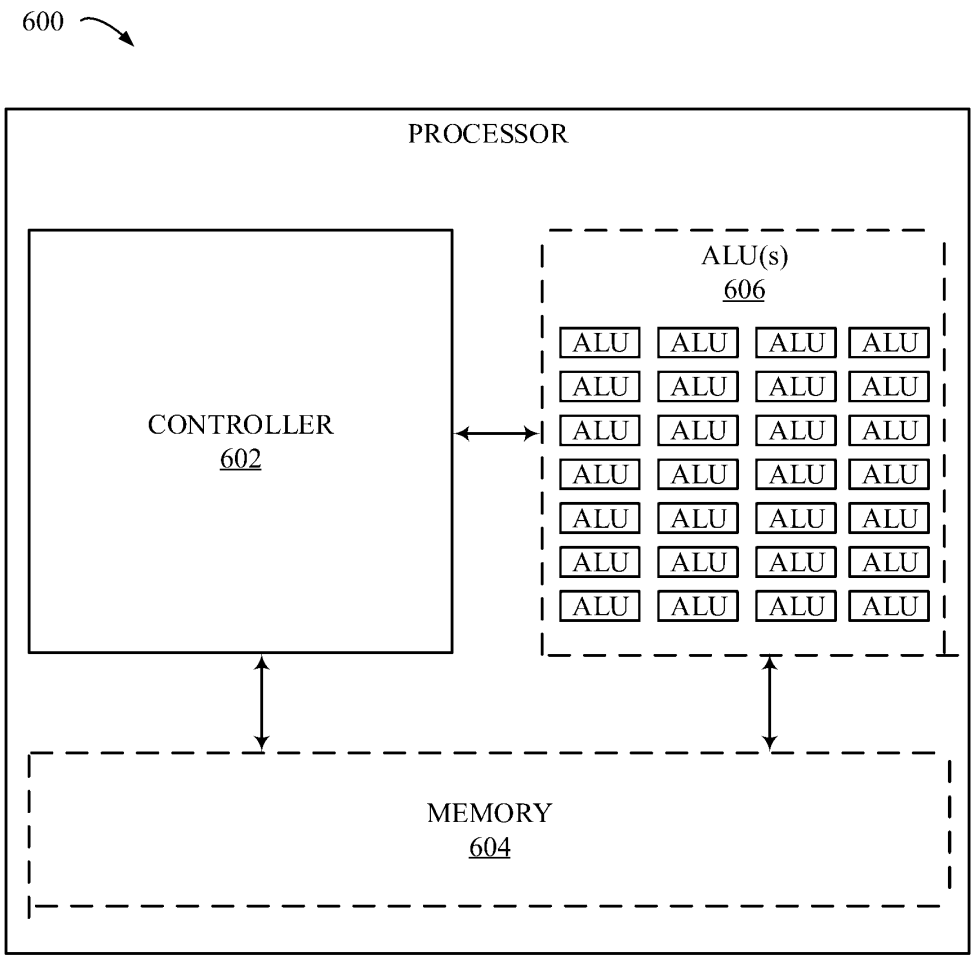


FIG. 6

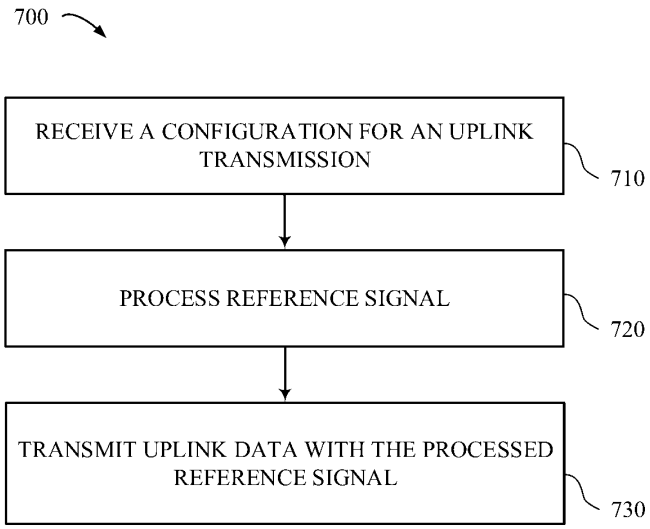

700
RECEIVE A CONFIGURATION FOR AN UPLINK TRANSMISSION
710
PROCESS REFERENCE SIGNAL
720
TRANSMIT UPLINK DATA WITH THE PROCESSED REFERENCE SIGNAL
730

FIG. 7

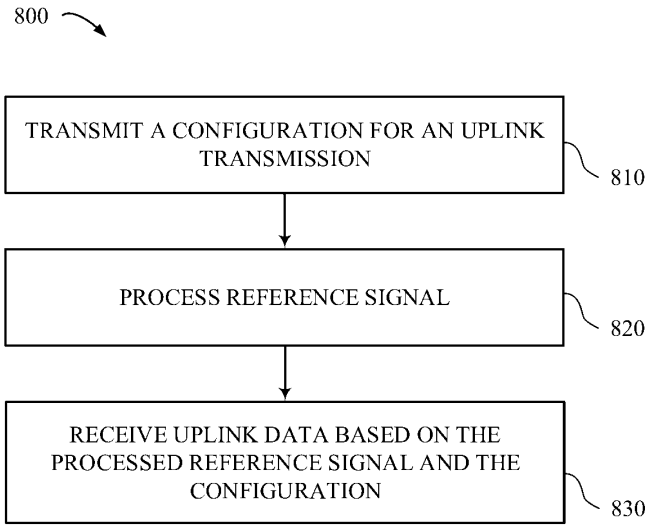

800
TRANSMIT A CONFIGURATION FOR AN UPLINK TRANSMISSION
810
PROCESS REFERENCE SIGNAL
820
RECEIVE UPLINK DATA BASED ON THE PROCESSED REFERENCE SIGNAL AND THE CONFIGURATION
830

FIG. 8