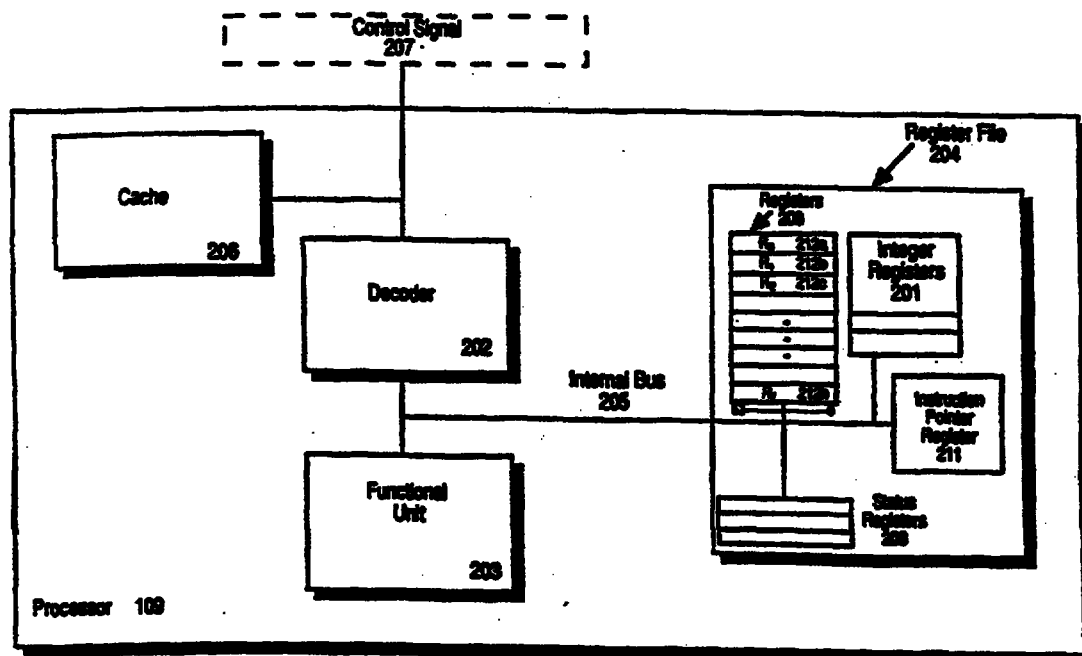


INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : G06F 7/52, 9/30		A1	(11) International Publication Number: WO 96/17293
			(43) International Publication Date: 6 June 1996 (06.06.96)
(21) International Application Number: PCT/US95/15681		(81) Designated States: AL, AM, AT, AT (Utility model), AU, BB, BG, BR, BY, CA, CH, CN, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, <u>SG</u> , SI, SK, SK (Utility model), TJ, TM, TT, UA, UG, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG), ARIPO patent (KE, LS, MW, SD, SZ, UG).	
(22) International Filing Date: 1 December 1995 (01.12.95)			
(30) Priority Data: 08/349,559 1 December 1994 (01.12.94) US			
(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).			
(72) Inventors: PELEG, Alexander; 38 Hannah Street, Carmelia, Haifa (IL). YAARI, Yaakov; 17/2 Soerot Hanadin, Hanadin, Haifa (IL). MITTAL, Millind; 1149 Hillside Boulevard, South San Francisco, CA 94080 (US). MENNEMEIER, Larry, M.; P.O. Box 587, Boulder Creek, CA 95006 (US). EITAN, Benny; 25 Stephen Weiss, Haifa (IL).			
(74) Agents: DE VOS, Daniel, M. et al.; Blakely, Sokoloff, Taylor & Zafman, 12400 Wilshire Boulevard, 7th floor, Los Angeles, CA 90025-1026 (US).		Published With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments. ① PCT A1 + SR ② Iper + Annexes ③ Replacement	

(54) Title: A MICROPROCESSOR HAVING A MULTIPLY OPERATION



(57) Abstract

A processor (109) includes a decoder (202) being coupled to receive a control signal (207). The control signal has a first source address, a second source address, a destination address, and an operation field. The first source address corresponds to a first location. The second address corresponds to a second location. The destination address corresponds to a third location. The operation field indicates that a type of packed data multiply operation is to be performed. The processor further includes a circuit (203) being coupled to the decoder. The circuit is for multiplying a first packed data being stored at the first location with a second packed data being stored at the second location. The circuit is further for communicating a corresponding result packed data to the third location.