ABSTRACT

A METHOD TO FABRICATE A DOUBLE-POLYSILICON GATE STRUCTURE FOR A SUB-QUARTER MICRON SELF-ALIGNED-TITANIUM SILICIDE PROCESS

This invention relates to the fabrication of integrated circuit devices and more particularly to a method for minimizing the localized mechanical stress problems that can occur when silicided polysilicon gates are used to fabricate narrow channel CMOS devices. The invention addresses the avoidance of typical stress-induced problems in polysilicon gates, such as non-uniform silicide (including ' bowing' , thinning edges, etc.) and voids, which are becoming increasingly worse as gate lengths continue to be reduced. The key to this invention is to spread the highly detrimental mechanical stresses, in narrow silicided gates, over a larger vertical surface area. This is accomplished by using a thin/thick double polysilicon stack for the gate, whereby, the lower thin polysilicon gate layer is not silicided and the upper thick polysilicon layer is subsequently silicided. An insulating layer is used to prevent silicidation of the lower thin polysilicon gate, during silicidation of active source-drain regions. The same insulating layer is also used to avoid another cause of mechanical stress, by protecting the surface grain boundaries of the lower thin polysilicon gate layer from being ' stuffed' with polymer during the dry etching used for spacer formation. The tall stacked gate structure allows the silicide-induced stresses to be more safely located farther away from the active devices.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)