CLAIMS

1. A synapse memory system comprising:

a plurality of synapse memory cells provided at cross points of a plurality of axon lines and a plurality of dendrite lines, each synapse memory cell comprising a plurality of analog memory devices each including a plurality of resolution steps, each synapse memory cell being configured to store a weight value according to an output level of a write signal, the weight value to be stored in each synapse memory cell being one value of at least three different values, the plurality of analog memory devices each including the plurality of resolution steps being combined to constitute each synapse memory cell expressed by an exponential scale using the plurality of resolution steps of all of the synapse memory cells; a write portion configured to write the weight value to each synapse memory cell, the write portion comprising a write driver and an output controller, the write driver being configured to output the write signal to a subject synapse memory cell, the subject synapse memory cell being one of the synapse memory cells, the subject synapse memory cell being selected to store the weight value, the output controller being configured to control the output level of the write signal of the write driver;

and read drivers configured to read the weight value stored in the synapse memory cells.

2. The synapse memory system according to claim 1, wherein dynamic ranges of the plurality of analog memory devices are combined to obtain a dynamic range of each synapse memory cell as a whole.

3. The synapse memory system according to claim 2, wherein each of the plurality of analog memory devices is assigned with a different magnitude.

4. The synapse memory system according to any one of the preceding claims, wherein the plurality of synapse memory cells are arranged such that long sides of the plurality of analog memory devices included in each synapse memory cell are parallel to each other.

5. The synapse memory system according to claim 4, wherein aspect ratio of each synapse memory cell is smaller than aspect ratio of each analog memory device.

6. The synapse memory system according to claim 4, wherein aspect ratio of each synapse memory cell is almost 1:1.

7. The synapse memory system according to any one of the preceding claims, wherein each analog memory device comprises a non-volatile random access memory (NVRAM).

8. The synapse memory system according to any one of the preceding claims, wherein each analog memory device comprises a magnetoresistive random access memory (MRAM).

9. A method for operating a synapse memory system, the synapse memory system comprising:

a plurality of synapse memory cells provided at cross points of a plurality of axon lines and a plurality of dendrite lines, each synapse memory cell comprising a plurality of analog memory devices each including a plurality of resolution steps, wherein the plurality of analog memory devices each including the plurality of resolution steps is combined to constitute each synapse memory cell expressed by an exponential scale using the plurality of resolution steps of all of the synapse memory cells; a write portion comprising a write driver and an output controller;

and a set of read drivers;

the method comprising:

storing, by a synapse memory cell of the system, a weight value according to an output level of a write signal, the weight value stored being one value of at least three different values;

writing, by the write portion, the weight value in the synapse memory cell, the writing comprising:

outputting, by the write driver, the write signal to the synapse memory cell selected to store the weight value, and controlling, by the output controller, the output level of the write signal of the write driver;

and reading, by the read drivers, the weight value stored in the synapse memory cells.

10. The method of claim 9, further comprising combining dynamic ranges of the plurality of analog memory devices to obtain a dynamic range of each synapse memory cell as a whole.

11. The method of claim 10, further comprising assigning each of the plurality of analog memory devices with a different magnitude.

12. The method of any one of claims 9 to 11, further comprising arranging the plurality of synapse memory cells such that long sides of the plurality of analog memory devices included in each synapse memory cell are parallel to each other.

13. The method of claim 12, wherein an aspect ratio of each synapse memory cell is smaller than aspect ratio of each analog memory device.

14. The method of claim 12, wherein the aspect ratio of each synapse memory cell is almost 1:1.

15. The method of any one of claims 9 to 14, wherein each analog memory device comprises a non-volatile random access memory (NVRAM).

16. The method of any one of claims 9 to 14, wherein each analog memory device comprises a magnetoresistive random access memory (MRAM).