

A SEMICONDUCTOR PACKAGE AND METHOD FOR FORMING SAME

Field of the Invention

5 This invention relates to package for a semiconductor die, and more particularly to a package having a perimeter which is not substantially greater than that of the semiconductor die.

Background of the Invention

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 Ever increasing pressure on reducing the size of packaged semiconductor devices has led to the development of several different types of semiconductor packages wherein a die is inverted and directly attached to a substrate to increase the density of external connections that are provided within the perimeter of the package.

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 One such package is known as a Tape Automated Bonding package, which comprises a flexible substrate having a central opening. Around the central opening a pattern of runners extend inwardly. The runners also have corresponding outer portions that are made available for interconnection to, for example, a printed circuit board

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(PCB). An inverted die is mounted over the central opening, and through the central opening the inwardly extending inner portions of the runners are soldered to the enlarged pads on the die.

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 With this package a relatively high density of runners can be formed on the flexible substrate to provide a higher density of external connections. However, the opening under the die limits the available area for runners within the perimeter of the die.

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Consequently, the density of runners is limited which limits the density of external connections. In addition, the pads on the die are enlarged for soldering to the inner portions of the runners. The number of enlarged pads that can be accommodated on the die also limits the density of external connections.

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 Another type of semiconductor package comprises a rigid substrate, such as a PCB, with a pattern of runners and an inverted centrally mounted die having pads that are bonded to inner

portions of the runners. An advantage of this package is that the pads on the die do not need to be enlarged. This means a greater number of pads can be made available on the die, thereby increasing the density of external connections.

5 The absence of a central opening allows more area for runners within the perimeter of the die. However, commonly used PCB and flexible substrate manufacturing processes provide a lower density of runners on the PCB than on the flexible substrate, thus, limiting the density of the number of external connections that can be provided
10 on this type of package.

Brief Summary of the Invention

15 The present invention therefore seeks to provide a semiconductor package which overcomes, or at least reduces the above-mentioned problems of the prior art.

20 Accordingly, in one aspect, the invention provides a semiconductor package comprising: at least one semiconductor die having a perimeter, the at least one semiconductor die comprising: a plurality of die pads; a substantially flexible insulator comprising: a plurality of openings; at least one conductive layer having a perimeter which is not significantly greater than the perimeter of the
25 at least one semiconductor die, the at least one conductive layer comprising: a plurality of bond pads, wherein at least some of the plurality of bond pads are coupled to at least some of the plurality of die pads; a plurality of interconnecting locations, wherein at least some of the plurality of interconnecting locations are aligned with at least some of the plurality of openings; and a plurality of connectors, wherein at least some of the plurality of connectors are coupled
30 between at least some of the plurality of bond pads and at least some of the plurality of interconnecting locations; and a substantially rigid insulator disposed between the at least one semiconductor die and the substantially flexible insulator.

35 In another aspect, the invention provides a method for forming a semiconductor package, the method comprising the steps of: providing: at least one semiconductor die having a perimeter, the at least one semiconductor die comprising: a plurality of die pads; a

substantially flexible insulator comprising: a plurality of openings; at least one conductive layer having a perimeter which is not significantly greater than the perimeter of the at least one semiconductor die, the at least one conductive layer comprising: a plurality of bond pads a plurality of interconnecting locations; and a plurality of connectors coupled between at least some of the plurality of bond pads and at least some of the plurality of interconnecting locations; and curable insulating material; aligning the at least some of the plurality of die pads with the at least some of the plurality of bond pads; while maintaining the alignment in step (b), disposing the at least one semiconductor die on the substantially flexible insulator; bonding at least some of the plurality of die pads to at least some of the plurality bond pads; disposing the curable insulating material between the at least one semiconductor die and the substantially flexible insulator; curing the disposed curable insulating material.

Brief Description of the Drawings

An embodiment of the invention will now be more fully described, by way of example, with reference to the drawings of which:

FIG. 1 shows a side sectional view of a semiconductor package in accordance with the present invention; and

FIG. 2 shows a flowchart detailing the method of forming the semiconductor package in FIG. 1.

Detailed Description of the Drawings

In FIG. 1 a chip scale semiconductor package 2 has a semiconductor die 5 which is inverted or flipped. Chip scale packages are generally semiconductor packages where the perimeter of the package is less than 1.2 times the perimeter of a die within the package. The die 5 has pads 6 arranged in a predetermined pattern to provide inputs and outputs to circuitry thereon. Typically, the pads 6 and the circuitry are formed on a common surface of the die 5, however the pads 6 and the circuitry can be

formed on different surfaces of the die 5. Each of the pads 6 is formed by a layer of metallization, usually aluminum.

5 An additional layer of metallization 7 is formed on the pads 6 to prepare the pads 6 for thermocompression bonding. The layer of metallization 7 comprises a layer of gold on the aluminum pads 6. The layer of gold 7 or gold bump is formed on the pads 6 by mechanical gold stud bumping. The gold bumps can also be electroplated on the pads or formed by electroless gold plating. The thickness of the layer of gold 7 is approximately 15 to 25
10 micrometers.

A flexible substrate 9 has a pattern of interconnecting runners 12. The runners 12 are made of copper and are 18 micrometers thick. The flexible substrate 9 is made of polyimide which is an electrically insulator. An end of each of the interconnecting runners
15 12 forms bond locations 10 which are arranged to correspond with the pattern of the pads 6 on the die 5. The pads 6 are coupled mechanically, and are electrically connected to, the bond locations 10 by thermocompression bonding.

20 A layer of metallization 14 is formed on the bond locations 10 to prepare them for thermocompression bonding. The layer of metallization 14 comprise a layer of tin plating with a thickness of 0.5 to 1 micrometers on the bond locations. The layer of tin 14 is formed on the bond locations 10 by an electroless plating process, or alternatively by an electrolytic plating process.

25 A pattern of openings 15 in the flexible substrate 9 provide access to interconnecting locations 16 on the interconnecting runners 12-14.

Solder balls 20 attached to the interconnecting locations 16 through the openings 15 to form what is known as a ball grid array
30 BGA which is used to mount as well as to couple the semiconductor package 2 to connection points on a printed circuit board. The solder balls 20 are a eutectic composition of 63 percent tin and 37 percent lead, however, other proportions of tin and lead can also be used.

35 The solder balls 20 have are placed in the openings 10 by flux ball placement and attach to the interconnecting locations 16 by a reflow process.

An underfill 22 between the die 5 and the flexible substrate 9 to protect the die 5. In addition, the underfill 22 makes the semiconductor package 2 rigid. The underfill 22 is formed using epoxy resin which is dispensed on two edges of the die 5. Capillary action draws the epoxy resin from the edges between the die 5 and the substrate 9.

With additional reference now to FIG. 2, the process of forming the semiconductor package 2 starts with aligning the die 5 and the substrate 9 such that the pads 6 are aligned with the bonding locations 10 on the substrate 9. For proper alignment it is recommended that the equipment used have an accuracy of 5 micrometers.

Once aligned, the die 5 is placed on the substrate 9 with the pads 6 contacting the bonding locations 10. The die and the substrate are then pressed together at an elevated pressure and simultaneously heated to an elevated temperature. The pressure is approximately 1 kilogram force. Two heaters are used, one to heat the die 5 at 360 degrees Celsius, and another to heat the substrate 9 at 180 degrees Celsius. The heat and pressure are applied for a period of three seconds for thermocompression bonding to occur. During this period, the tin 14 on the copper runner 12-14 melts and reacts with the gold bumps 7 to form a strong gold-tin intermetallic joint.

After the bonding process, the epoxy resin underfill 22 is dispensed and subsequently cured. The package is then flipped over and the solder balls 20 are attached to the interconnecting locations 16. Finally, the completed semiconductor package is tested.

Thus, the present invention, as described, advantageously provides a semiconductor package having a higher density of external connections. This is accomplished by combining the higher density of runners on a flexible substrate with the higher density bonding of the die to the flexible substrate.

Hence, the present invention provides a semiconductor package which overcomes, or at least reduces the above-mentioned problems of the prior art.

It will be appreciated that although only one particular embodiment of the invention has been described in detail, various modifications and improvements can be made by a person skilled in the art without departing from the scope of the present invention.



Claims

1. A semiconductor package comprising:
 - at least one semiconductor die having a perimeter, the at least
 - 5 one semiconductor die comprising:
 - a plurality of die pads;
 - a substantially flexible insulator comprising:
 - a plurality of openings;
 - at least one conductive layer having a perimeter which is not
 - 10 significantly greater than the perimeter of the at least one semiconductor die, the at least one conductive layer comprising:
 - a plurality of bond pads, wherein at least some of the plurality of bond pads are coupled to at least some of the plurality of die pads;
 - 15 a plurality of interconnecting locations, wherein at least some of the plurality of interconnecting locations are aligned with at least some of the plurality of openings; and
 - a plurality of connectors, wherein at least some of the plurality of connectors are coupled between at least some of the
 - 20 plurality of bond pads and at least some of the plurality of interconnecting locations; and
 - a substantially rigid insulator disposed between the at least one semiconductor die and the substantially flexible insulator.
- 25 2. A semiconductor package in accordance with claim 1 wherein:
 - the at least one semiconductor die comprises at least one semiconductor die means for providing at least one circuit;
 - the plurality of die pads comprise a plurality of die pad means for connecting to the at least one circuit;
 - 30 the substantially flexible insulator comprises a substantially flexible insulating means for selectively insulating at least portions of the circuit;
 - the at least one conductive layer comprises at least one conductive layer means for providing the plurality of bond pads, the
 - 35 plurality of interconnecting locations and the plurality of connectors;



the plurality of bond pads comprise a plurality of bond pad means for bonding to the at least some of the plurality of die pad means;

5 the plurality of interconnecting locations comprise a plurality of interconnecting location means for connecting to the semiconductor package;

the plurality of connectors comprise a plurality of connector means for connecting at least some of the plurality of bond pad means to at least some of the plurality of interconnecting locations;
10 and

the substantially rigid insulator comprises a substantially rigid insulator means for insulating at least a portion of the at least one semiconductor die means from the at least a portion of the at least one conductive layer means, and for rigidizing the semiconductor
15 package.

3. A semiconductor package comprising:

at least one semiconductor die means for providing at least one circuit, the at least one semiconductor die means having a
20 plurality of pad means for connecting to the at least one circuit;

a substantially flexible insulating means for insulating at least portions of the at least one circuit, the substantially flexible insulating means having a plurality of openings;

at least one conductive layer means for providing a plurality
25 of bond pad means, a plurality of interconnecting location means, and a plurality of connector means within a perimeter which is not significantly greater than the perimeter of the at least one semiconductor die means, wherein at least some of the plurality of bond pad means are for bonding to at least some of the plurality of
30 die pad means, wherein at least some plurality of interconnecting location means are for connecting to the semiconductor package, and wherein at least some of the plurality of connector means are for coupling at least some of the plurality of bond pads to at least some of the plurality of interconnecting locations; and

35 a substantially rigid insulator means disposed between the at least one semiconductor die means and the substantially flexible insulator means, the substantially rigid insulator means for



insulating at least a portion of the at least one semiconductor die means from the at least a portion of the at least one conductive layer means, and for rigidizing the semiconductor package.

- 5 4. A semiconductor package in accordance with claim 3 wherein the perimeter of the at least one conductive layer means is not greater than 1.2 times the perimeter of the semiconductor die means.
- 10 5. A semiconductor package in accordance with claim 3 wherein each of the plurality of die pad means comprises at least one layer of conductive material.
- 15 6. A method for forming a semiconductor package, the method comprising the steps of:
- a) providing:
- at least one semiconductor die having a perimeter, the at least one semiconductor die comprising:
- a plurality of die pads;
- 20 a substantially flexible insulator comprising:
- a plurality of openings;
- at least one conductive layer having a perimeter which is not significantly greater than the perimeter of the at least one semiconductor die, the at least one conductive layer comprising:
- 25 a plurality of bond pads;
- a plurality of interconnecting locations; and
- a plurality of connectors coupled between at least some of the plurality of bond pads and at least some of the plurality of interconnecting locations; and
- 30 curable insulating material;
- b) aligning the at least some of the plurality of die pads with the at least some of the plurality of bond pads;
- c) while maintaining the alignment in step (b), disposing the at least one semiconductor die on the substantially flexible insulator;
- 35 d) bonding at least some of the plurality of die pads to at least some of the plurality bond pads;



- e) disposing the curable insulating material between the at least one semiconductor die and the substantially flexible insulator;
- f) curing the disposed curable insulating material.

- 5 7. A method in accordance with claim 6 wherein step (e) is performed before step (d).
8. A method in accordance with claim 6 wherein step (e) further comprises the steps of:
- 10 dispensing the curable insulating material along at least one side of the at least one semiconductor die; and
- distributing the curable insulating material between the at least one semiconductor die and the substantially flexible insulator by capillary action.
- 15 9. A method in accordance with claim 6 wherein step (d) comprises the steps of:
- compressing the at least one semiconductor die and the substantially flexible insulator together; and
- 20 applying heat to the at least one semiconductor die and the substantially flexible insulator.
10. A method in accordance with claim 9 wherein step (d) comprises the step of applying substantially more heat to the at
- 25 least one semiconductor die than to the substantially flexible insulator.
11. A method in accordance with claim 9 wherein step (d) comprises the step of applying substantially more heat to the
- 30 substantially flexible insulator than to the at least one semiconductor die.