

PATENT SPECIFICATION

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DRAWINGS ATTACHED

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(54) DIRECT-COUPLED PUSH-PULL AMPLIFIER

(71) We, RCA CORPORATION, (formerly RADIO CORPORATION OF AMERICA), a corporation organised under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention is directed to a push-pull amplifying stage which is direct coupled to a single-ended driving source.

A push-pull stage using this invention is useful as a power output stage in applications, such as operational amplifiers, servo-drivers, regulators and other direct coupled amplifier apparatus, which use cascade-connected amplifiers. In apparatus using cascade-connected, direct coupled amplifiers the direct current (d.c.) or quiescent voltage at the output electrode of one stage comprises the voltage which is applied to the next succeeding stage. In general, this d.c. voltage is offset from the amplifier reference, which may arbitrarily be considered as a ground or 0 volt reference. In direct coupled push-pull stages level shift means is generally employed to shift the level of this d.c. voltage to provide proper bias for a phase-splitting circuit which in turn operates a pair of push-pull output amplifying devices. This level shifting is carried out in a manner such that the d.c. voltage at the output terminal of the push-pull stage is zero volt. In addition, feedback means is often employed to provide d.c. stabilization as well as uniform frequency response throughout the range of interest.

One problem associated with the design of direct coupled push-pull stages of this type is that substantial signal attenuation or loss of signal occurs across the level shift means. To offset this signal attenuation the stage is designed to have a high gain. However, the dependency of gain on the value of load impedance and transconductance of the amplifying devices tends to restrict both the higher extreme of the power supply range

and the lower extreme of the load impedance range throughout which the stage can effect a constant gain. That is, lower values of load impedance require the amplifying devices to conduct more current to maintain a constant gain and consequently the thermal ratings of the devices restrict the maximum power supply values.

According to the invention, we provide a direct coupled, push-pull amplifier stage having a single-ended input and output connections; where the stage includes: (a) first and second amplifying devices connected in push-pull configuration to the output connection, (b) a phase-splitting circuit having an input and having a third amplifying device with an output connected to drive the first amplifying device (c) a level shift circuit including a first impedance coupling the input connection of the stage to the input of the phase-splitting circuit and (d) a feedback circuit including an impedance for coupling the output connection of the stage to the first impedance; and including the combination in which: the input of the third amplifying device is connected in parallel with the input of the second amplifying device; and the phase-splitting circuit includes a fourth amplifying device having an output arranged as a voltage follower connected to drive the inputs of both the second and third amplifying devices and having an input serving as the input of the phase splitting circuit, connected to the level shifting circuit.

This arrangement causes the phase-splitting circuit to present an input impedance which is high relative to the impedance of the level shifting circuit, so that signal attenuation is minimized to the point where constant gain can be achieved throughout an extremely wide range of load impedance values.

According to a particular version of the invention the level shifting circuit impedance includes first and second elements, such as first and second resistors, connected in series and disposed in a direct current path extending between the single-ended output point of the input stage and the input of the

fourth amplifying device. In this version of the invention, the impedance of the feedback circuit includes a third resistor, coupled between the output terminal and the juncture of the first and second impedance elements of the level shifting circuit. This arrangement additionally functions to clamp the end of the second resistor to a voltage differing from voltage supplied to the output point via the first and second amplifying devices by an amount sufficient to maintain a balanced bias condition for the pair of output amplifying devices. This clamping action enables the stage to maintain this balanced condition throughout a wide range of power supply values.

Direct coupled amplifier apparatus according to the present invention may be constructed either with discrete components or by means of integrated circuit processes. (As used herein, the term, integrated circuit, refers to those technologies by which an entire circuit can be formed, as by diffusion or by thin films, in or on one or more chips of material, such as silicon.) Direct coupled amplifiers are particularly suited for integrated circuit structures or devices since they employ no a.c. coupling elements such as transformers and capacitors, which elements are at the present time either impractical in the case of transformers, or not economically feasible, in the case of capacitors, to fabricate in integrated form. For this reason, the fact that all circuits used in the present invention are direct coupled to each other makes the amplifiers using the present invention useful when made in integrated form.

The push-pull amplifying stages of this invention are not limited in their application to use with any one particular type of amplifier apparatus. However, for the purpose of example and completeness of description, the sole FIGURE of the drawing includes a schematic diagram of a direct coupled amplifier with which the push-pull stage may be employed as a power output stage. The direct coupled amplifier apparatus is designed to have a very high gain and is particularly suited for operational amplifier applications.

Included in the operational amplifier apparatus are a pair of cascaded input stages 20 and 30 located to the left of a dashed line 10 and a push-pull power output stage 40 located to the right of the dashed line 10. Each of the stages 20 and 30 and 40 is connected between a pair of supply connections 11 and 12. The supply connection 11 is connected to a source of suitable operating potential, designated $+V_{cc}$; while the supply connection 12 is connected to another source of suitable operating potential, designated as $-V_{ee}$. The operating potential supplies V_{cc} and V_{ee} may comprise, for example, a three terminal supply

providing symmetrical positive (V_{cc}) and negative (V_{ee}) voltages relative to a suitable reference such as circuit ground. In addition, bypass capacitors (not shown) may be connected between the ground reference and the supply connections 11 and 12.

Each of the pair of input stages 20 and 30 (which do not of themselves embody the present invention) includes a pair of amplifying devices (e.g., the transistors 21 and 22 in stage 20) connected in a differential amplifier configuration. In each input stage, additional transistors such as 23 and 24 have their emitter electrodes 23e and 24e connected to the base electrodes 21b and 22b, respectively. The collector electrodes 23c and 24c are connected to the supply connection 11; while the base electrodes 23b and 24b are connected to input terminals 13 and 14, respectively.

The input terminals 13 and 14 are adapted to receive input signal voltage from a driving source 15. The driving source 15 is shown to have a further connection to a terminal 16 which is connected to a source of suitable reference potential, illustrated in the drawing as ground by the conventional symbol therefore. The source 15 may be any suitable source which is capable of driving the input terminals 13 and 14 in a differential mode.

In stage 30, the transistors 33 and 34 have their base electrodes 33b and 34b connected by way of direct coupling to the differential outputs of the stage 20. The emitter and collector circuits for the transistors 33 and 34 are similar to those for the transistors 23 and 24 in stage 20.

These additional transistors in each of the stages 20 and 30 provide improved high frequency response for each of the amplifier stages 20 and 30. In essence, the transistor 23, for example, provides an impedance transformation of the source impedance Z_s of the source 15, such that the Miller capacity C_m of transistor 21 is effectively in parallel

with $\frac{Z_s}{\beta}$ where β is the current amplification factor of transistor 23.

Since bandwidth is proportional to the product of source impedance and input capacitance, the bandwidth is effectively increased by a factor of β . It should be noted that since the collector electrodes of each of the transistors 23 and 24 and 33 and 34 are connected to the supply connection 11, none of these transistors has voltage gain, and hence there is substantially no Miller effect associated with any of them.

For the stages 20 and 30 there are provided current-determining transistors 60 and 70 and a bias arrangement for those transistors. The base electrodes 60b and 70b of transistors 60 and 70, respectively, share a common base circuit. This common base circuit includes a series connection of a temperature-

compensating diode and a resistance. The diode is illustrated as a transistor 65 having its base electrode 65b and its collector electrode 65c connected in common with the base electrodes 60b and 70b; and having its emitter electrode connected by way of resistance 61 to the supply connection 12. The series connection of the resistance 61 and the base-emitter junction of transistor 65 provides temperature compensation for transistors 60 and 70 in the well-known manner.

With the above described arrangement, an input signal voltage supplied by source 15 is amplified by the two stages 20 and 30 and appears at the single-ended output point 35 in stage 30. In addition to the amplified signal voltage, there is also a d.c. voltage at point 35 which is offset from the amplified reference or ground potential.

Stage 30 acts as a driving stage to provide single-ended drive from output point 35 to the push-pull power output stage 40. In push-pull stage 40, the signal voltage is translated from the driving point 35 via a level shift circuit 50 to a phase-splitting circuit 80 which is arranged to bias and operate a pair of amplifying devices 90 and 91 in a push-pull manner.

The level shift means 50 is connected between the driving point 35 and the V_{cc} supply connection 12 and is essentially a voltage divider providing a shift in d.c. voltage level between point 35 and an intermediate divider point 57. The upper portion of the divider includes a transistor 51 and resistors 52 and 53; while the lower portion includes a current source transistor 54. The transistor 51 is connected in the common collector configuration and arranged for class A operation. Transistor 51 has its base electrode 51b connected to the driving point 35, its collector electrode 51c connected to the supply connection 11 and its emitter electrode 51e connected by way of an impedance, including serially connected resistors 52 and 53, to the intermediate divider point 57. The current source transistor 54 is arranged to provide a substantially constant current flow through resistors 52 and 53 in order to effect a level shift in voltage between driving point 35 and divider point 57. To this end transistor 54 has its collector electrode 54c connected to divider point 57 and its emitter electrode 54e connected by way of an emitter resistor 55 to the supply connection 12. The base electrode 54b of current source transistor 54 may be connected in any suitable base circuit which operates transistor 54 as a substantially constant current source. In the illustrated circuit, the base electrode 54b is shown to share the previously mentioned common base circuit with current source transistor 60 and 70 in stages 20 and 30, respectively.

The signal voltage appearing at point 35 is translated to the intermediate divider point 57 and the translated voltage is applied to the phase-splitting circuit 80, which includes three transistors: 81, 82 and 83. The base-emitter junctions of the latter transistors are arranged in a circuit path across the lower portion of the level shifting voltage divider to clamp point 57 to a voltage which differs from the supply voltage V_{cc} by the base-emitter junction voltage drops of these transistors. Transistor 81 serves as a diode because both its collector electrode 81c and base electrode 81b are connected together (and also are connected to the collector electrode 54c); while its emitter electrode is connected to the base electrode 82b of emitter follower transistor 82. If desired, transistor 81 could be a diode connected for forward current flow in the same direction as the base-emitter junction of the transistor 81.

Emitter follower transistor 82 is arranged for class A operation and provides bias and signal voltage drive for phase-inverting transistor 83 and push-pull output transistor 91. To this end transistor 82 has its collector electrode 82c connected to circuit ground 16 and its emitter electrode 82e connected to the base electrode 83b of transistor 83 and the base electrode 91b of transistor 91. The emitter electrode 83e of phase-inverting transistor 83 is connected to the supply connection 12 and completes the clamping circuit for the divider point 57. The collector electrode 83c is connected to the supply connection 11 by way of collector resistor 84. The collector electrode 83c is further connected to the base electrode 85b of an impedance transforming transistor 85. The transistor 85 is arranged in a compound transistor connection with the push-pull output transistor 90. To this end the collector electrodes 85c and 90c are connected together to the supply connection 11; while emitter electrode 85e is connected to the base electrode 90b.

The push-pull output transistors 90 and 91 are arranged in circuit with an output terminal 92 in a single-ended fashion. The output terminal 92 is connected to the emitter electrode 90e of transistor 90 and the collector electrode 91c of transistor 91. To complete the circuit, the emitter electrode 91e of transistor 91 is connected to the supply connection 12. A feedback path including a resistance 93 is connected between the output terminal 92 and junction 56 between the resistors 52 and 53. A suitable load or utilization device 100 is connected between the output terminal 92 and the circuit ground connection 16.

In the illustrated example of the invention, it is preferred to operate the push-pull stage 40 in the class AB mode in order to minimize cross-over distortion. In addition, it is

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preferred that in the no signal or idle condition the d.c. voltage at output terminal 92 be the same as the reference potential 16 which, for the illustrated example, is ground or 0 volt. Thus, stage 40 is such that in the idle condition all the transistors are biased class A whereby transistors 90 and 91 conduct sufficient current to provide a d.c. voltage of 0 volt at output terminal 92. When signal voltage is applied, the phase-splitting circuit 80 splits the phase of the signal and applies out-of-phase signals to the push-pull transistors 90 and 91. For positive portions of the signal voltage, the transistor 91 is driven further into conduction to provide negative output voltage across the load at the same time the transistor 83 inverts the positive signal portions to drive the transistor 90 into cut off. For negative portions of the signal voltage, the transistor 91 is driven into cut off; while the transistor 83 inverts the negative signal portions to drive the transistor 90 further into conduction thereby providing positive output voltage across the load 100. For small amplitude signal voltage of either polarity, both transistors 90 and 91 are conducting to minimize cross-over distortion.

The phase-splitting circuit 80 including transistors 82 and 83 because their low input insertion loss (or high overall gain) enables the push-pull stage 40 to have a relatively constant closed loop gain throughout an extremely wide range of load impedance values. This range, is an integrated circuit by way of example, extends from values on the order of 200 ohms to values on the order of 10 kilohms or more. Moreover, the stage 40 is capable of maintaining this constant closed loop gain characteristic for power supply values on the order of ± 6 volts as well as for values on the order of ± 24 volts.

The circuit configuration of transistors 82 and 83 presents a relatively high impedance which compares favorably with the resistances of the level shifting resistors 52 and 53, so that signal attenuation or loss of signal voltage across resistors 52 and 53 is minimized to the point where the above-mentioned constant closed loop gain characteristic can be achieved. Transistor 83 not only provides the required inversion of signal voltage, but also provides by way of its base-emitter junction a V_{be} (base-emitter junction voltage drop) bias for output transistor 91. This type of bias in conjunction with transistor 82 provides a distinct advantage in input impedance over the type of phase-splitting circuit which utilizes a single phase-splitting transistor with a diode in its emitter circuit to provide bias for the output transistor. In the latter type circuit, the input impedance of the single transistor phase-splitter is $(1+\beta)$ times the emitter resistance of the transistor (r_e) in series with

the parallel combination of the diode forward impedance and the input impedance of common emitter transistor 91. Since this transistor and the diode are conducting essentially the same current, their impedances are essentially equal. Neglecting the input impedance of transistor 91, which is high relative to the diode's conduction impedance, the input impedance of the single transistor phase-splitter is $2(1+\beta)r_e$.

On the other hand, the impedance of the phase-splitter 80 in the present invention is $(1+\beta_{82})$ times r_{e82} appearing in series with the parallel combination of the input impedances of common emitter transistors 83 and 91. If transistors 83 and 91 are matched, then this can be written as $(1+\beta_{82})(r_{e82} + (1+\beta_{83})r_{e83/2})$. The factor of $1/2$ appears because the input impedances of transistors 83 and 91 are equal and appear in parallel. Furthermore, since the emitter current of transistor 82 is the sum of the base currents of transistors 83 and 91 and since a transistor's emitter impedance is inversely proportional to its emitter current, the emitter impedance of transistor 82 is equal to $(1+\beta_{83})r_{e83/2}$. Thus, the input impedance of the phase-splitter 80 is $(1+\beta_{82})(1+\beta_{83})r_{e83}$, which is a factor of $(1+\beta_{82})/2$ improvement over the single transistor phase-splitter. This factor of improvement is normally at least one order of magnitude and compares more favorably with the resistances of level shift resistors 52 and 53 such that less signal attenuation occurs thereacross and high resistor values (52 and 53) can be used. Since this input impedance is indeed a much larger value, the dissipation can be decreased by increasing resistor values.

The exemplary circuit illustrated in the drawing has been designed with a low enough dissipation so that power supply values from 6 volts to 24 volts do not cause an excession of thermal ratings. Moreover, this improvement in input impedance level has been accomplished by eliminating a diode and adding one transistor as compared to the single transistor phase-splitter. The minimization of signal attenuation is such that the open loop gain of stage 40 can be given a high enough value to enable the closed loop gain to approach a value equal to the ratio of feedback resistor 93 divided by level shift resistor 52. In essence, what this means is that an a.c. virtual ground is created at point 56 such that push-pull stage 40 itself acts like an operational amplifier. In addition, the level shift circuit 50 is designed so that there is also an effective d.c. ground at point 56, which together with the 0 volt d.c. condition at output terminal 92 insures that there is ideally no feedback current during the idle or no signal condition. If either of the supplies V_{ee} or V_{cc} drift, a slowly varying drift signal would be translated by the push-pull stage 40

and fed back negatively via resistor 93 in such a manner tending to d.c. stabilize the stage 40.

The clamping action of point 57 by the PN base emitter junctions of transistors 81, 82 and 83 maintains this point at a value of about 2 volts (assuming silicon type transistors) more positive than the V_{ee} supply voltage. The voltage at point 56 can move only a few millivots about this nominal value. It is these few millivots that determine cut off or saturation in transistors 90 and 91. If one of these transistors is turned on the other is turned off by virtue of the actuating signal inversion provided by transistor 83. The feedback resistor 93 senses the output condition and alters the voltage at point 57 until the transistors 90 and 91 are essentially in the same state of bias (nearly off except for a small idle current through each). It is due to the fact that only a few millivots change is required at the point 57 to create this balanced condition that the feedback resistor 93 can effect it over a wide range of supply values.

The illustrated embodiment of the invention is especially suitable for monolithic integrated circuit technology in that only transistors of the same conductivity type are employed. It should be noted that the illustrated NPN transistors could just as well be replaced with PNP transistors so long as the polarities of the supplies V_{ee} and V_{cc} are accordingly changed.

WHAT WE CLAIM IS:—

1. A direct coupled, push-pull amplifier stage having single-ended input and output connections; where the stage includes: (a) first and second amplifying devices connected in push-pull configuration to the output connection, (b) a phase-splitting circuit having an input and having a third amplifying device with an output connected to drive the first amplifying device (c) a level shift circuit including a first impedance coupling the input connection of the stage to the input of the phase-splitting circuit and (d) a feedback circuit including an impedance for coupling the output connection of the stage to the first impedance; and including the combination in which: the input of the third amplifying device is connected in parallel with the input of the second amplifying device; and the phase-splitting circuit includes a fourth amplifying device having an output arranged as a voltage follower connected to drive the inputs of both the second and third amplifying devices,

having an input, serving as the input of the phase splitting circuit connected to the level shifting circuit.

2. An amplifier stage as claimed in claim 1; wherein: each of the amplifying devices is a transistor; and all said transistors are the same conductivity type.

3. An amplifier stage as claimed in claim 2, wherein each of the transistors has a base, emitter and collector electrode, wherein the collector and emitter electrodes of the first and second transistors are connected in series between respective bias sources and the output connection wherein a collector impedance is connected in a series circuit with the collector and emitter electrodes of the third transistor and the collector electrode of the third transistor is coupled to the base electrode of the first transistor; and wherein the emitter electrode of the fourth transistor is direct coupled to the base electrodes of the second and third transistors; the base electrode of the fourth transistor is connected to the first impedance; and the collector electrode of the fourth transistor is connected to a point which provides bias and signal voltage drive for the second and third transistors.

4. An amplifier stage as claimed in claim 1, 2 or 3, wherein the first impedance of the level shifting circuit includes first and second series connected resistors and wherein said impedance of the feedback circuit includes a third resistor connected between the common connection of said first and second resistors and the stage output connection.

5. An amplifier stage as claimed in claim 1, 2, 3 or 4, wherein the level shift circuit includes an additional transistor having its base electrode connected to said input connection, its collector electrode connected to a bias voltage supply and its emitter electrode connected in series with the first impedance; and wherein the level shift circuit further includes a current source transistor which provides a current path connected in series with the first impedance and emitter electrode of the additional transistor.

6. A direct coupled, push-pull amplifier stage substantially as described with reference to the accompanying drawing.

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2. An amplifier stage as claimed in claim 1; wherein: each of the amplifying devices is a transistor; and all said transistors are the same conductivity type.

3. An amplifier stage as claimed in claim 2, wherein each of the transistors has a base, emitter and collector electrode, wherein the collector and emitter electrodes of the first and second transistors are connected in series between respective bias sources and the output connection wherein a collector impedance is connected in a series circuit with the collector and emitter electrodes of the third transistor and the collector electrode of the third transistor is coupled to the base electrode of the first transistor; and wherein the emitter electrode of the fourth transistor is direct coupled to the base electrodes of the second and third transistors; the base electrode of the fourth transistor is connected to the first impedance; and the collector electrode of the fourth transistor is connected to a point which provides bias and signal voltage drive for the second and third transistors.

4. An amplifier stage as claimed in claim 1, 2 or 3, wherein the first impedance of the level shifting circuit includes first and second series connected resistors and wherein said impedance of the feedback circuit includes a third resistor connected between the common connection of said first and second resistors and the stage output connection.

5. An amplifier stage as claimed in claim 1, 2, 3 or 4, wherein the level shift circuit includes an additional transistor having its base electrode connected to said input connection, its collector electrode connected to a bias voltage supply and its emitter electrode connected in series with the first impedance; and wherein the level shift circuit further includes a current source transistor which provides a current path connected in series with the first impedance and emitter electrode of the additional transistor.

6. A direct coupled, push-pull amplifier stage substantially as described with reference to the accompanying drawing.

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