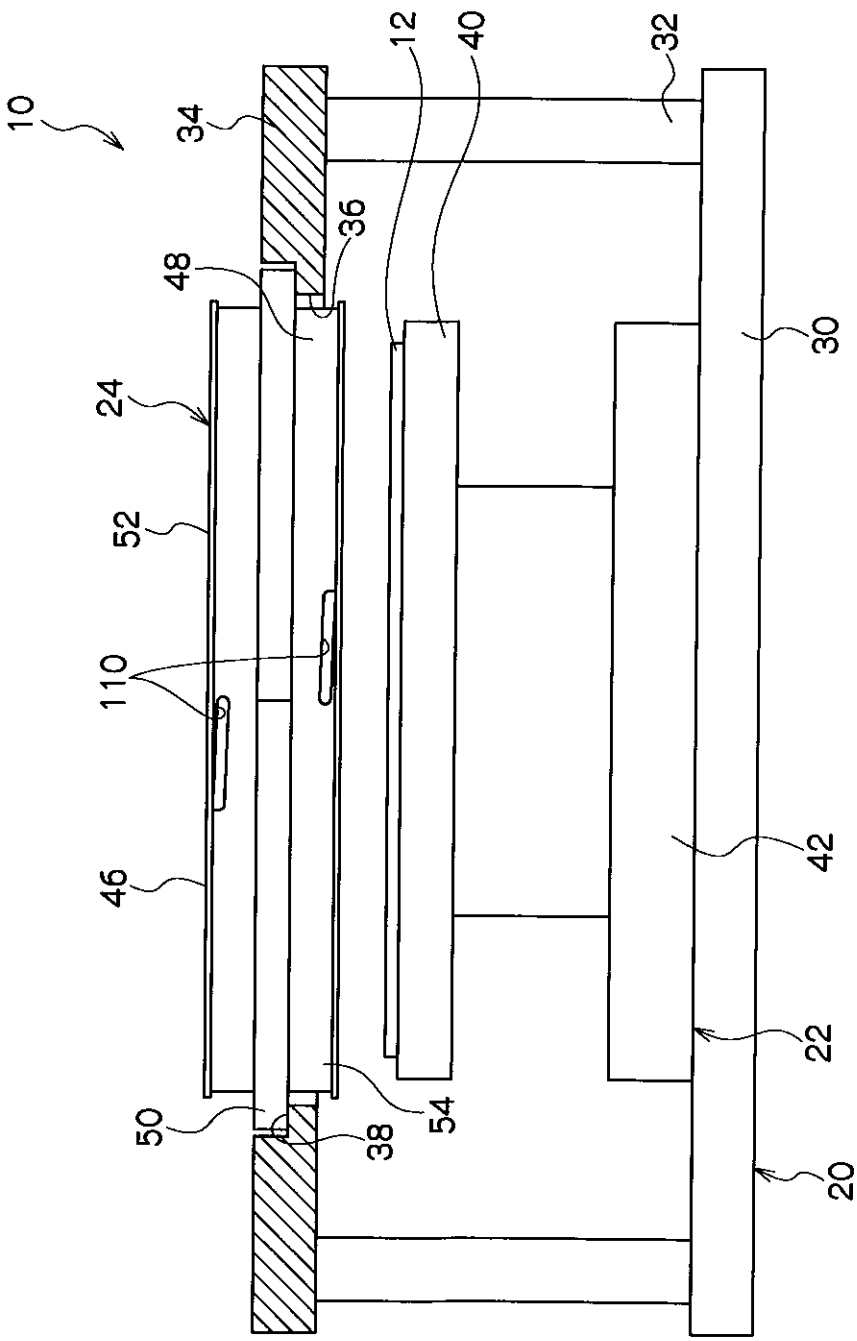


Fig. 1

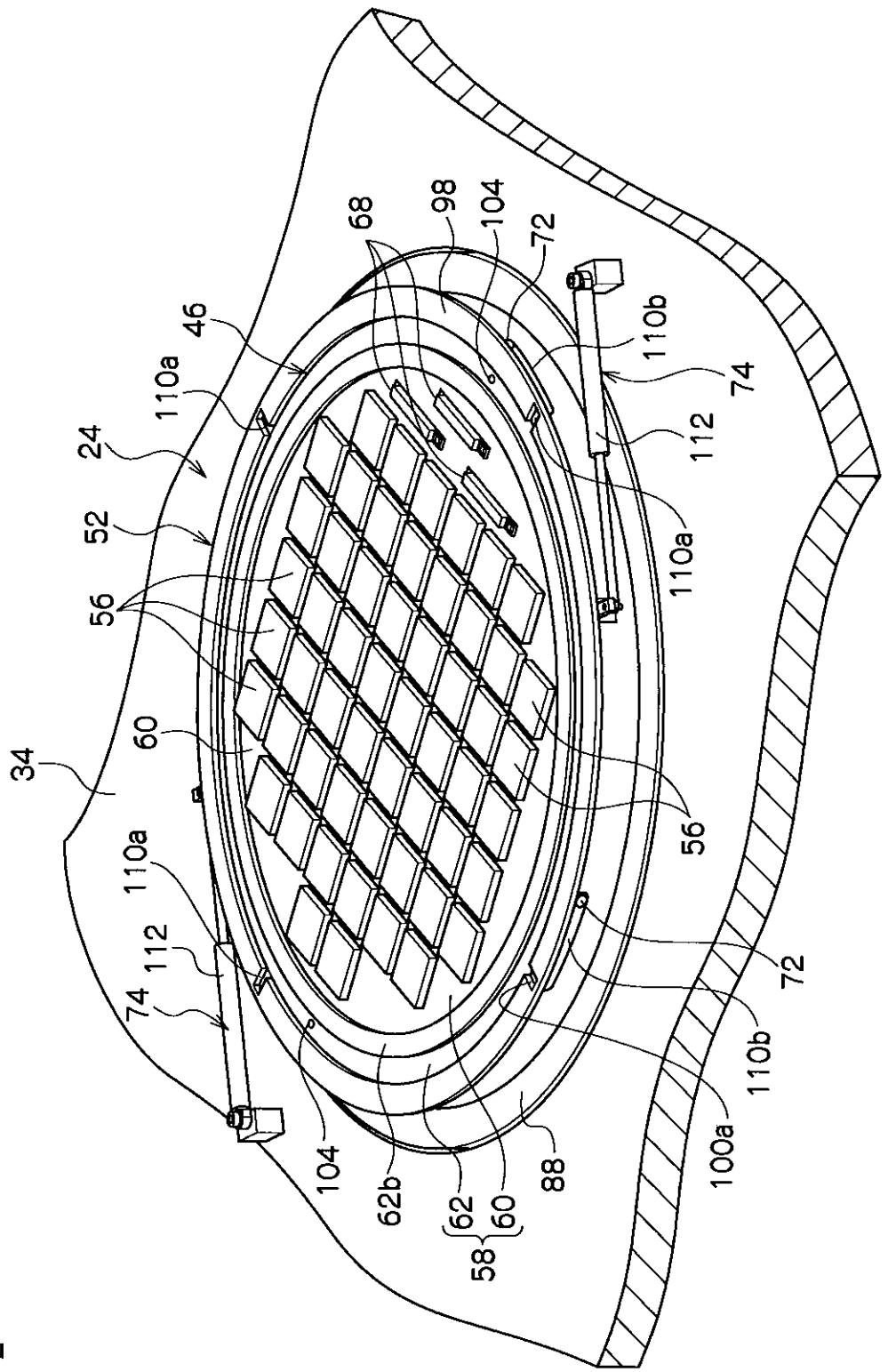
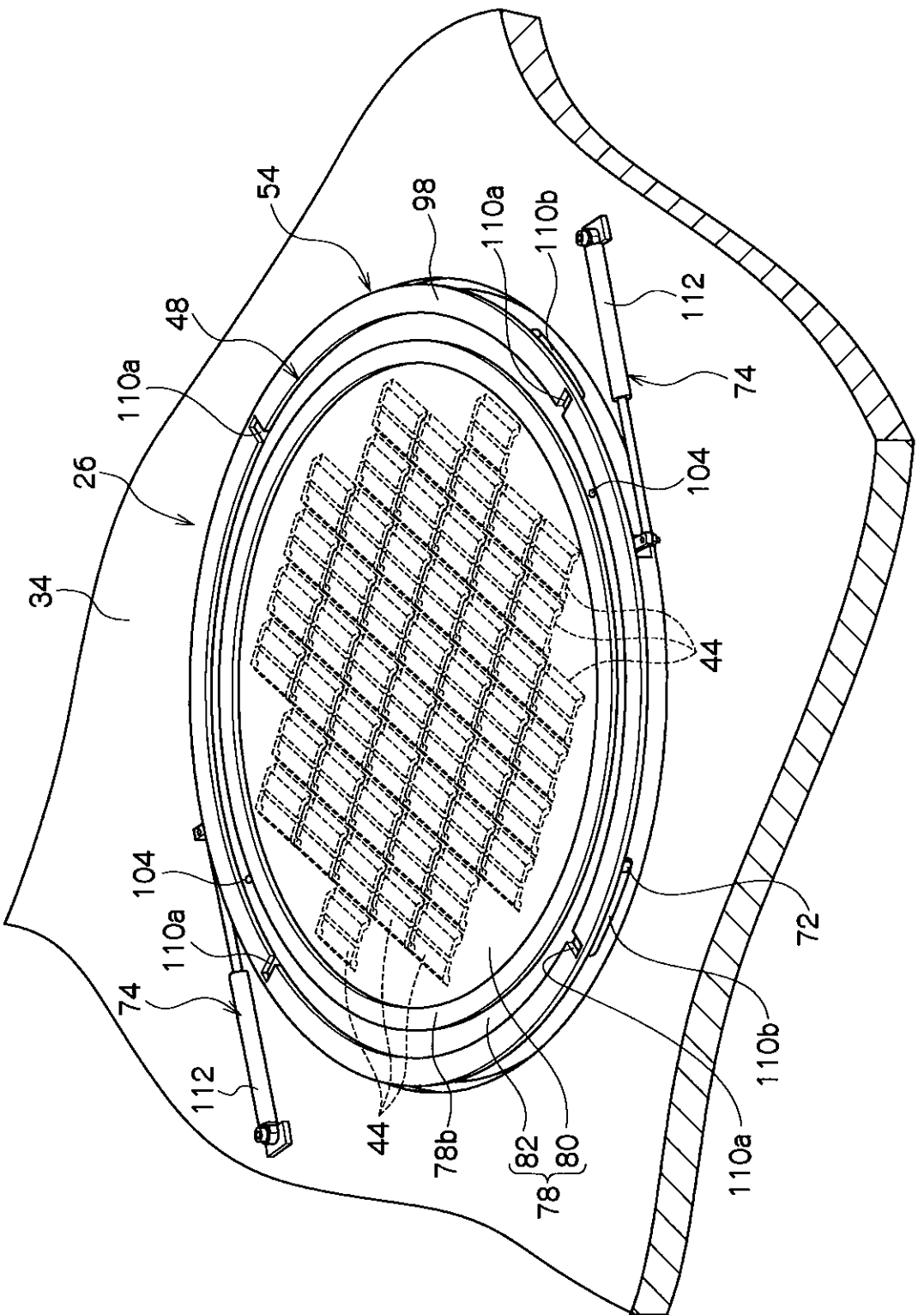

68
98
104
72
46
110a
24
52
56
60
34
110a
112
74
104
62b
62
60
58
88
110b
74
112
110a
56
72
110b
100a

Fig. 2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98
110a
110b
48
112
110a
74
26
104
34
44
104
110a
74
112
44
78b
82
80
78
110a
110b
72

Fig. 3

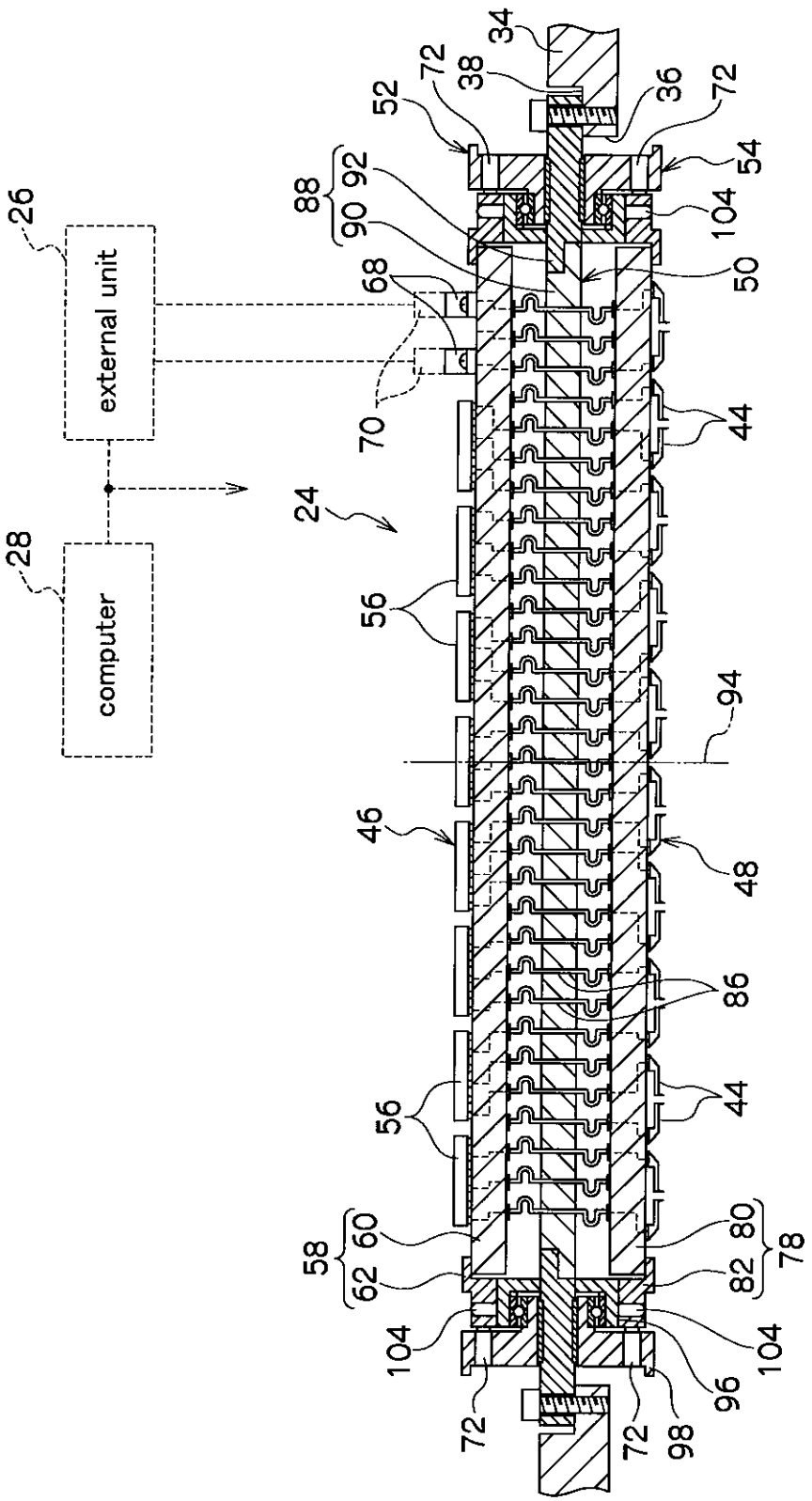

26
external unit
28
computer
24
34
38
36
72
52
54
88
92
90
104
50
68
70
44
56
94
46
48
86
58
60
62
80
82
78
96
98

Fig. 4

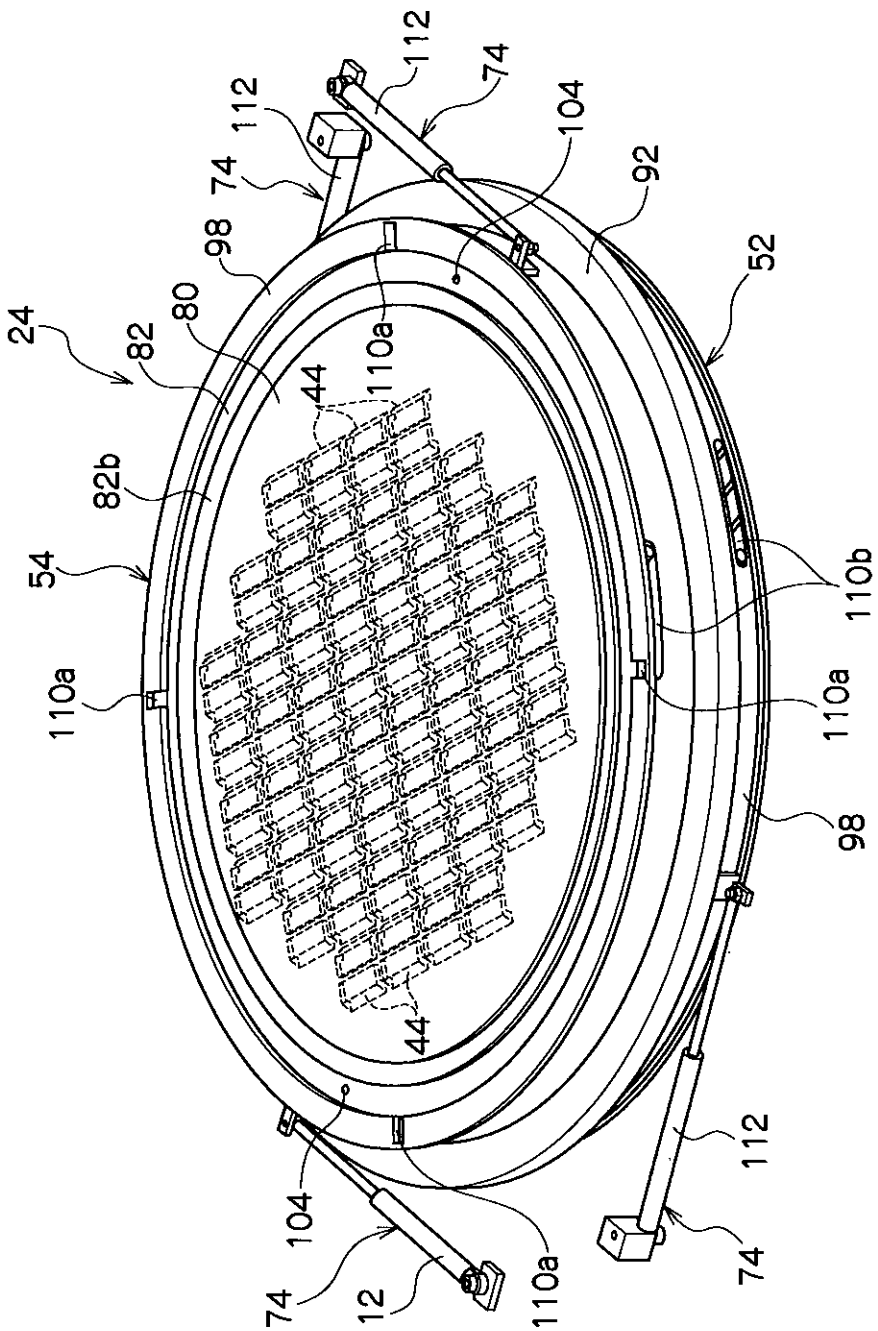

112
74
104
92
52
112
74
98
80
24
82
110a
44
82b
54
110b
110a
110a
98
44
112
104
74
112
110a
74

Fig. 5

Fig. 6

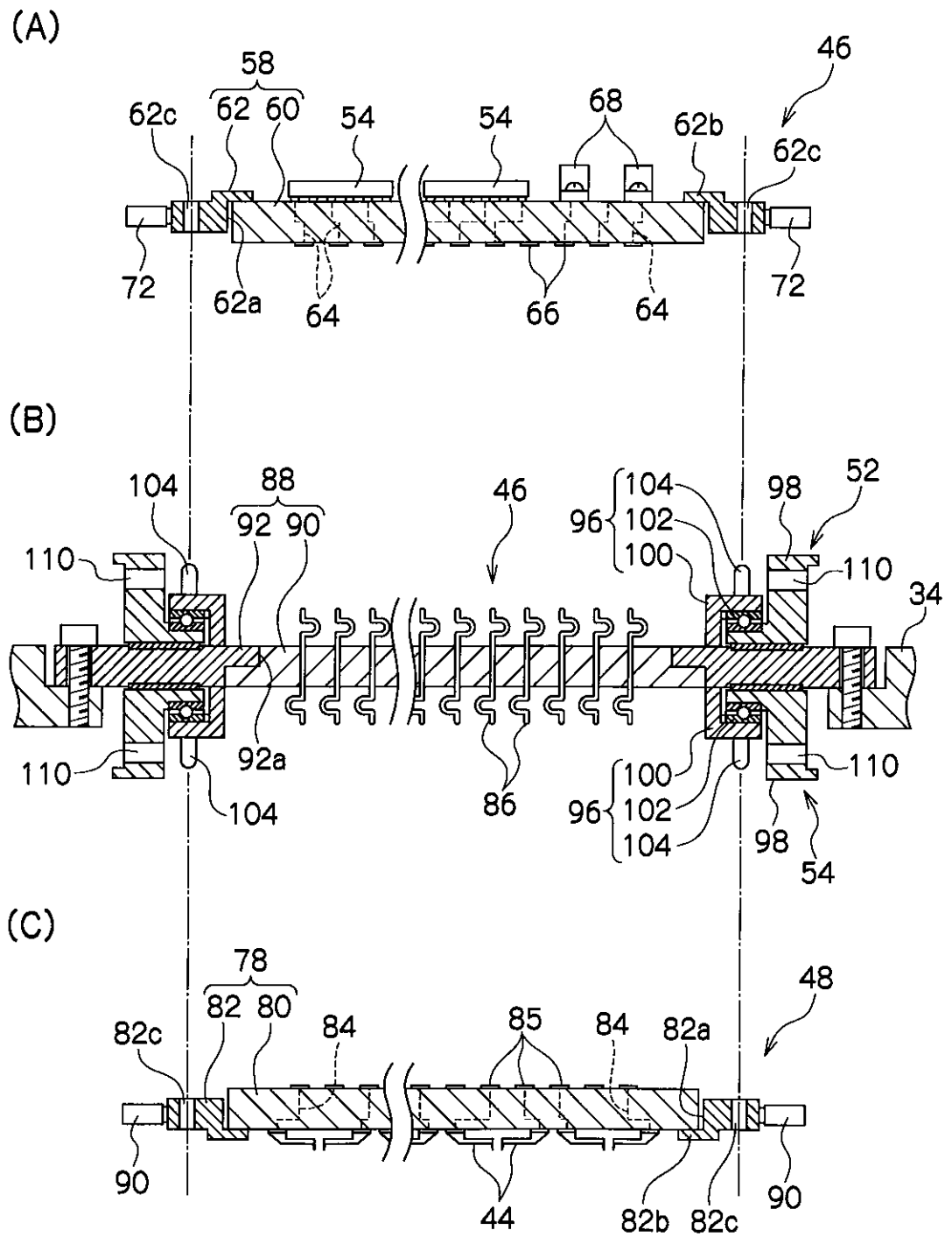

(A)
58
62 60
62c
54
54
68
62b
46
62c
72
62a
64
66
64
72
(B)
104
88
92 90
46
104
96 102
100
98
52
110
110
34
110
92a
104
86
100
96 102
104
110
98
54
(C)
78
82 80
82c
84
85
84
82a
48
90
44
82b
82c
90

Fig. 7

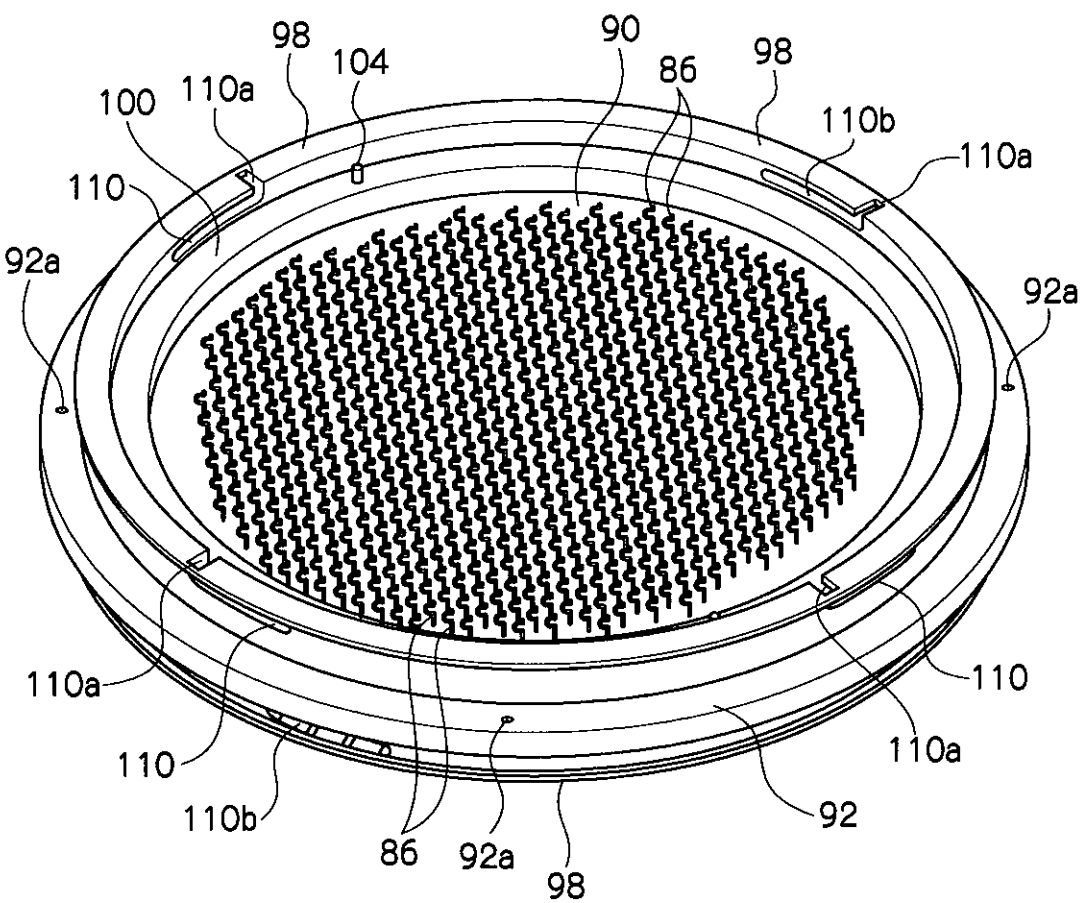

98
104
90
86
98
100
110a
110b
110a
110
92a
92a
110a
110
110
110a
110b
92
86
92a
98

Fig. 8

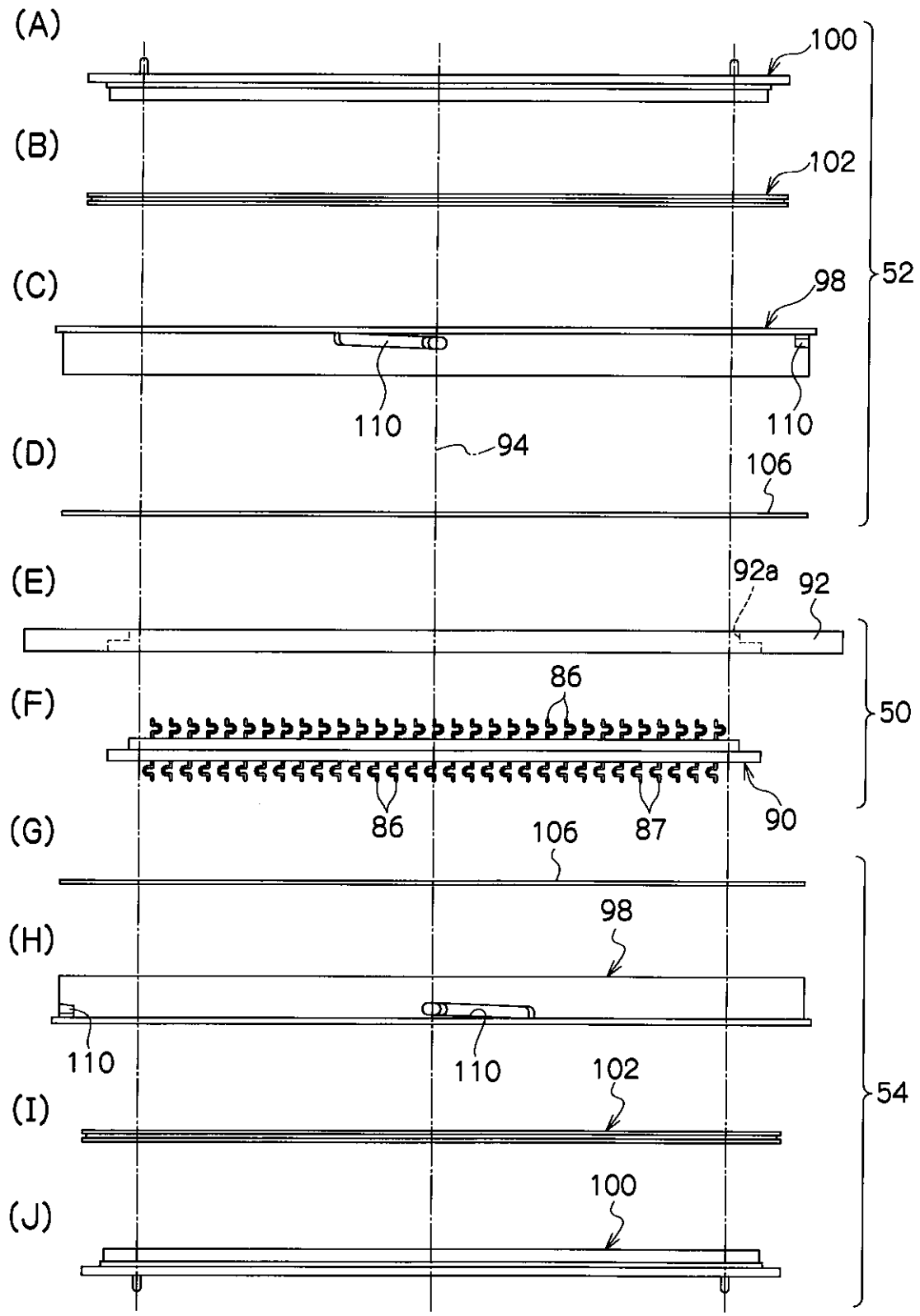

(A)
100
(B)
102
(C)
98
52
110
110
(D)
94
106
(E)
92a
92
(F)
86
50
86
87
90
(G)
106
(H)
98
110
110
102
54
(I)
(J)
100

Fig. 9

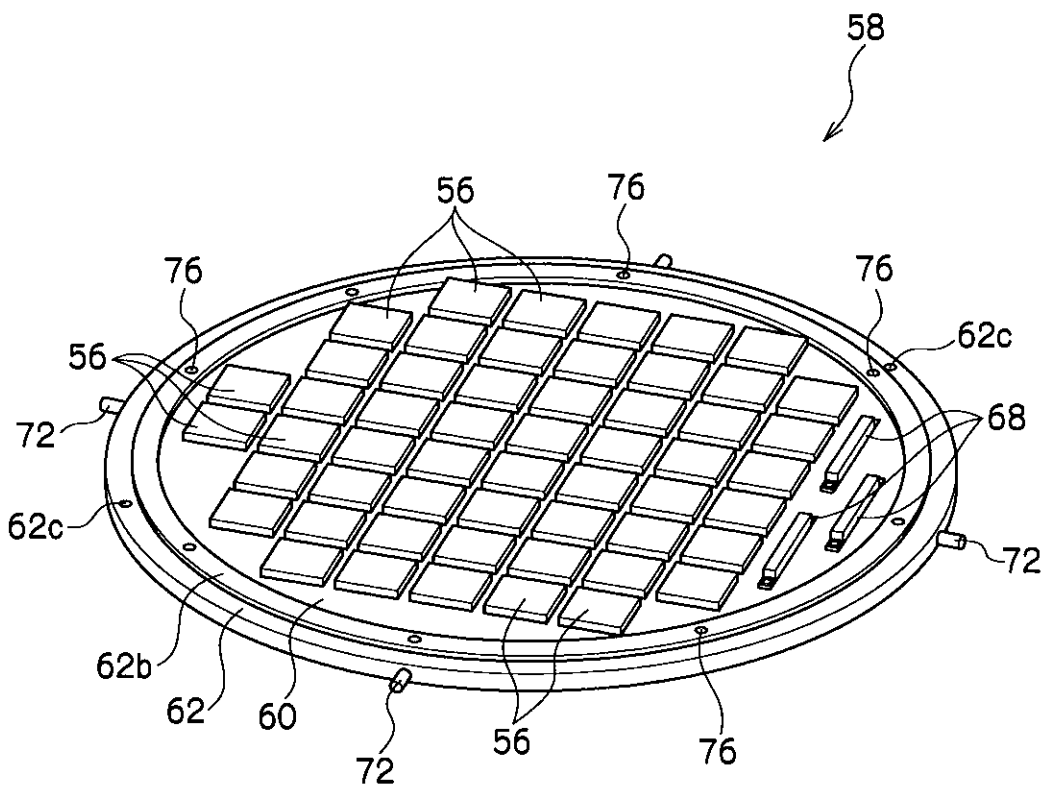


Fig. 10

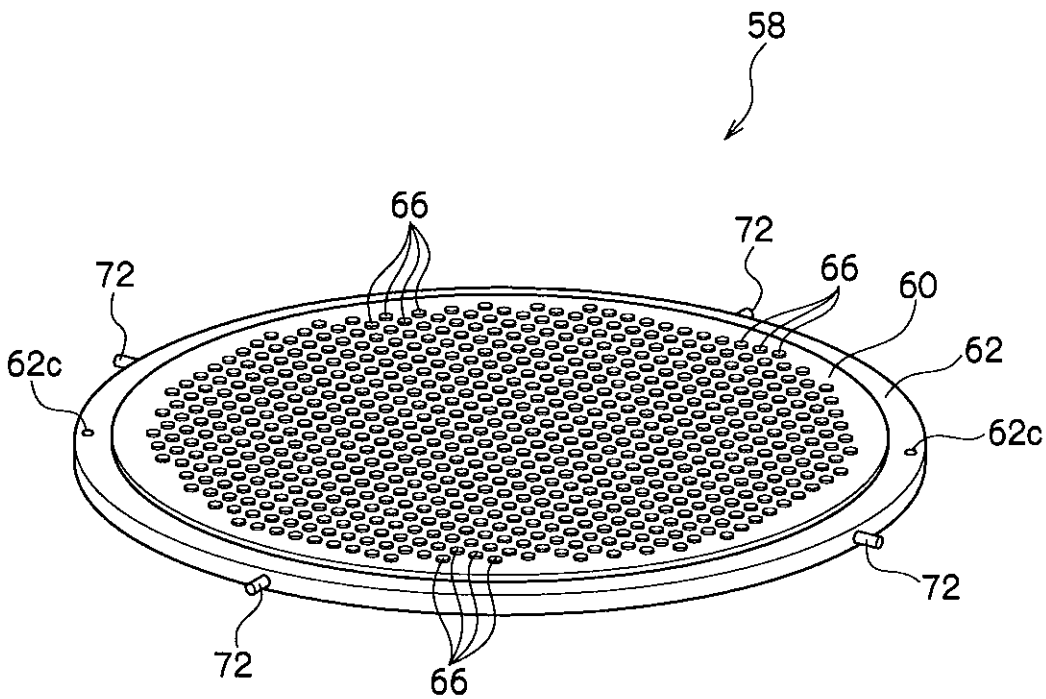
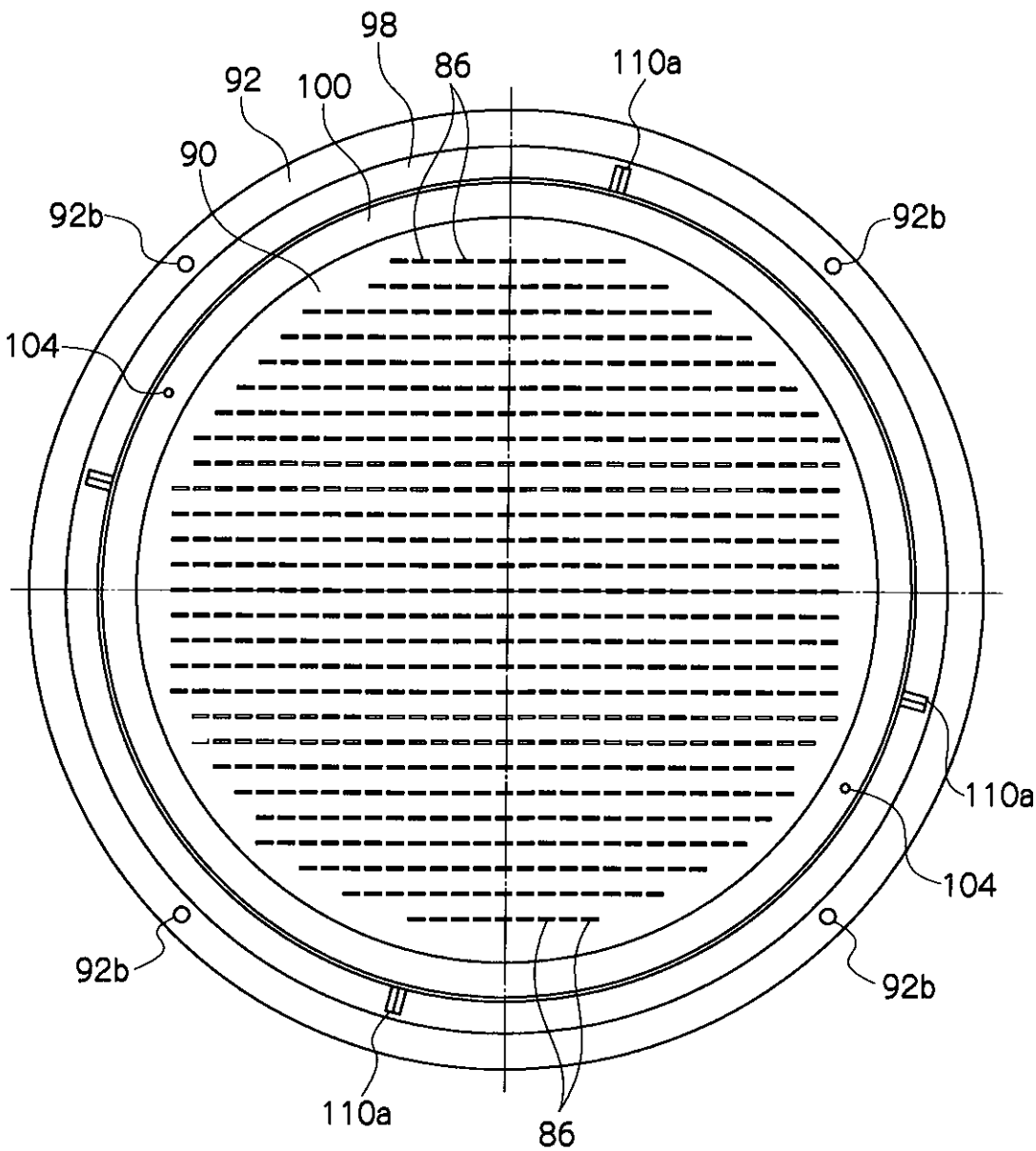
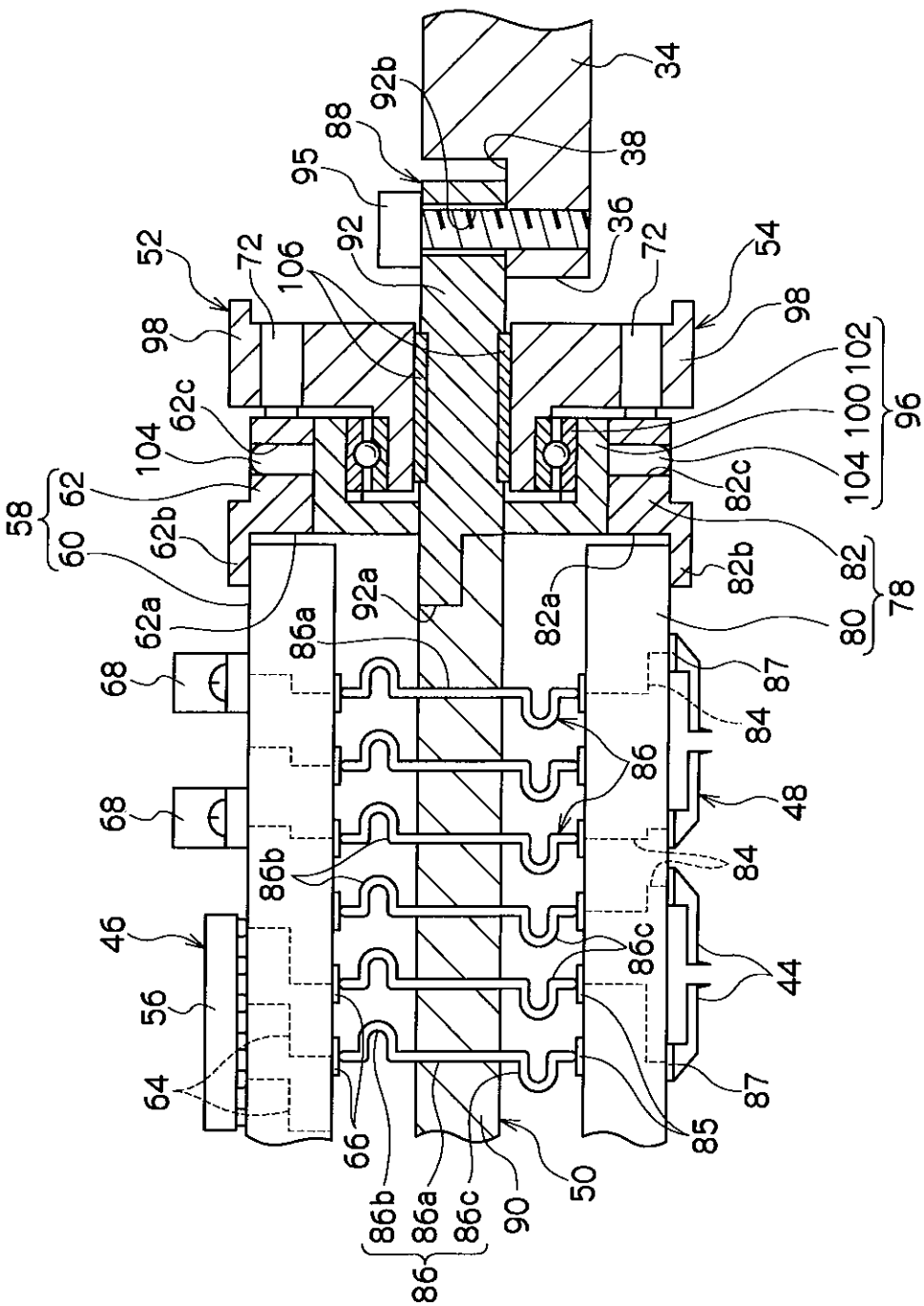


Fig. 11

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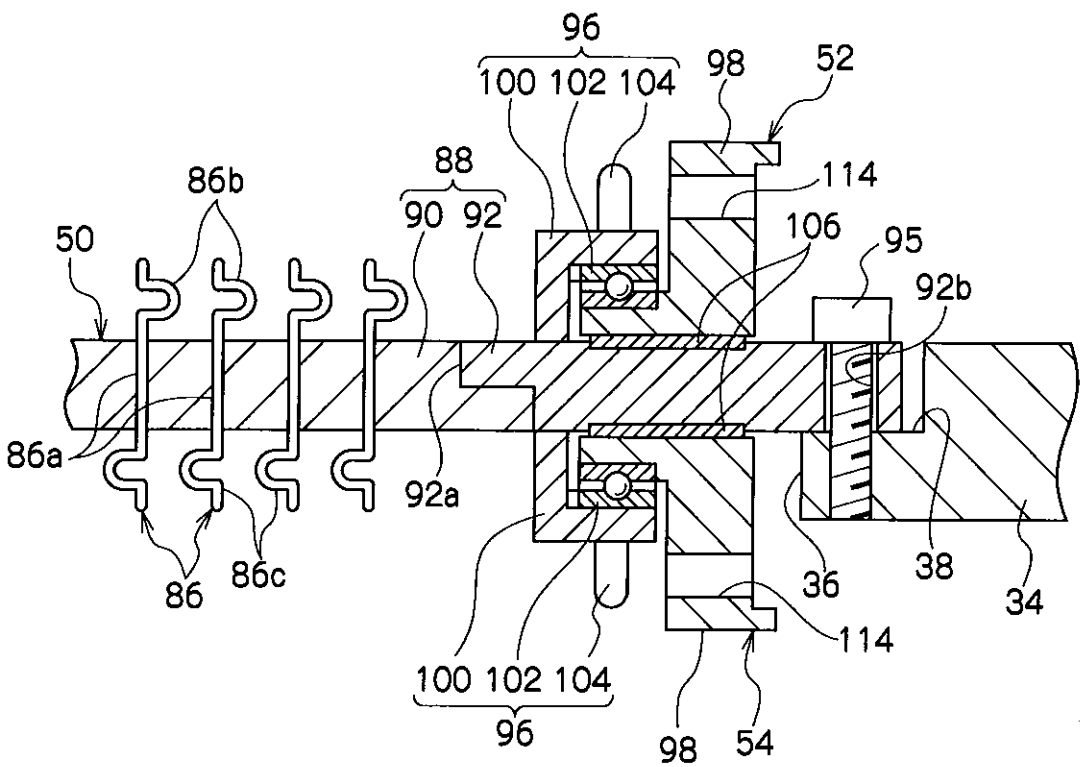
92b
88
38
95
36
92
72
106
72
52
54
98
98
102
100
96
104
62c
104
82c
58
62
60
62b
82
82b
78
80
62a
92a
82a
86a
87
68
84
86
48
68
84
86b
86c
46
44
56
64
87
66
85
50
86b
86a
86c
90
86

Fig. 12

Fig. 13


96
100 102 104
98
52
88
90 92
86b
114
106
95
92b
50
86a
92a
86
86c
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38
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114
100 102 104
96
98
54

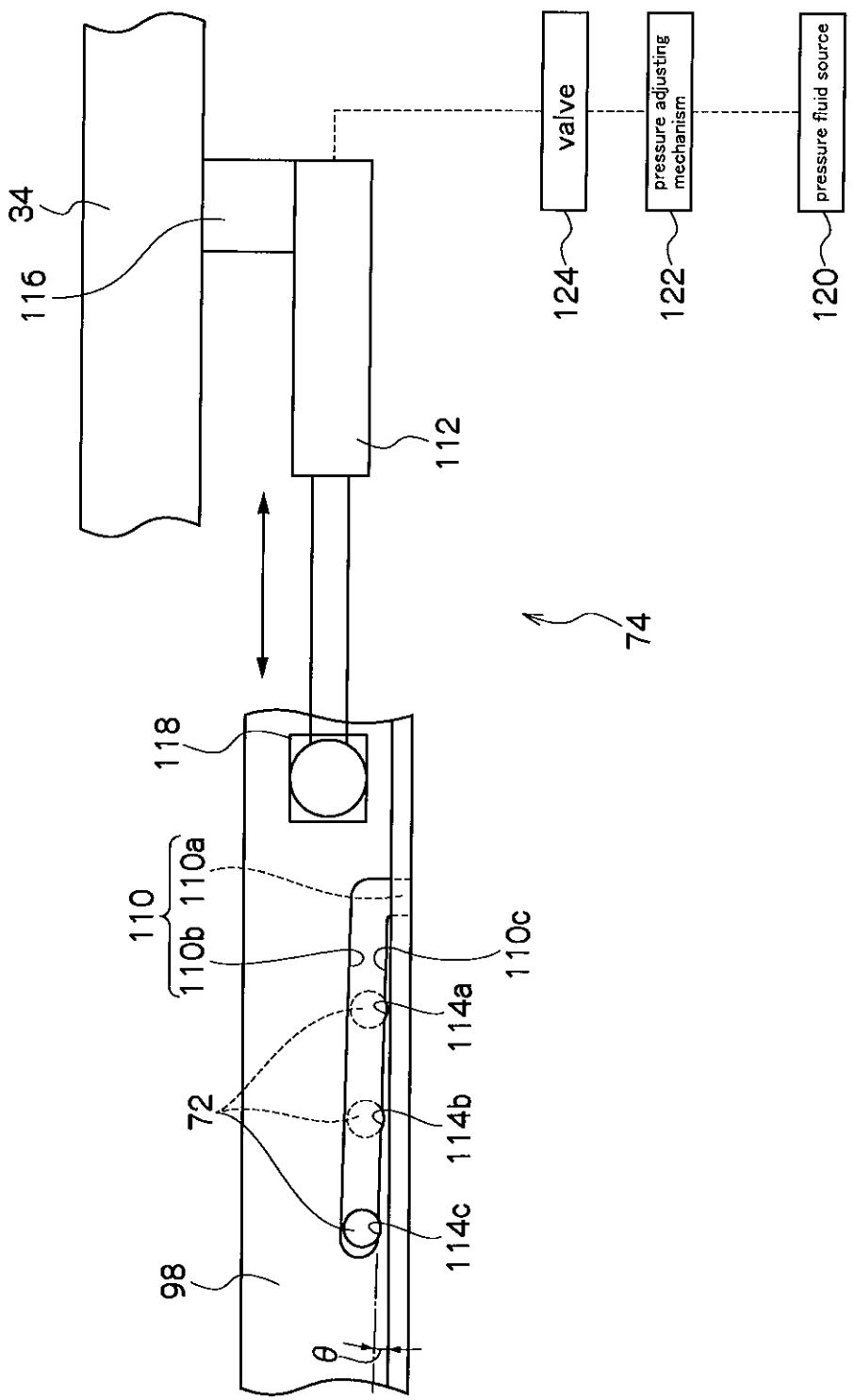

34
116
112
valve
pressure adjusting mechanism
pressure fluid source
124
122
120
74
118
110
110a
110b
110c
114a
114b
114c
72
98
θ

Fig. 14

Fig. 15

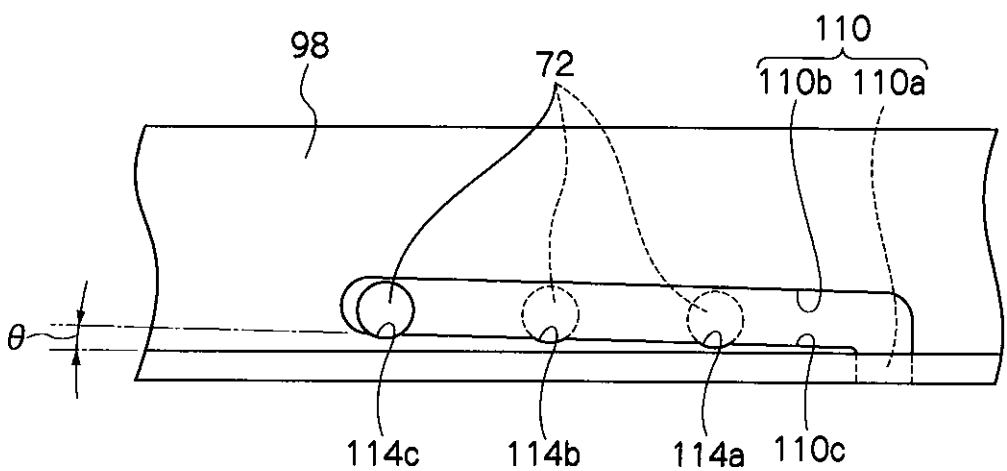


Fig. 16

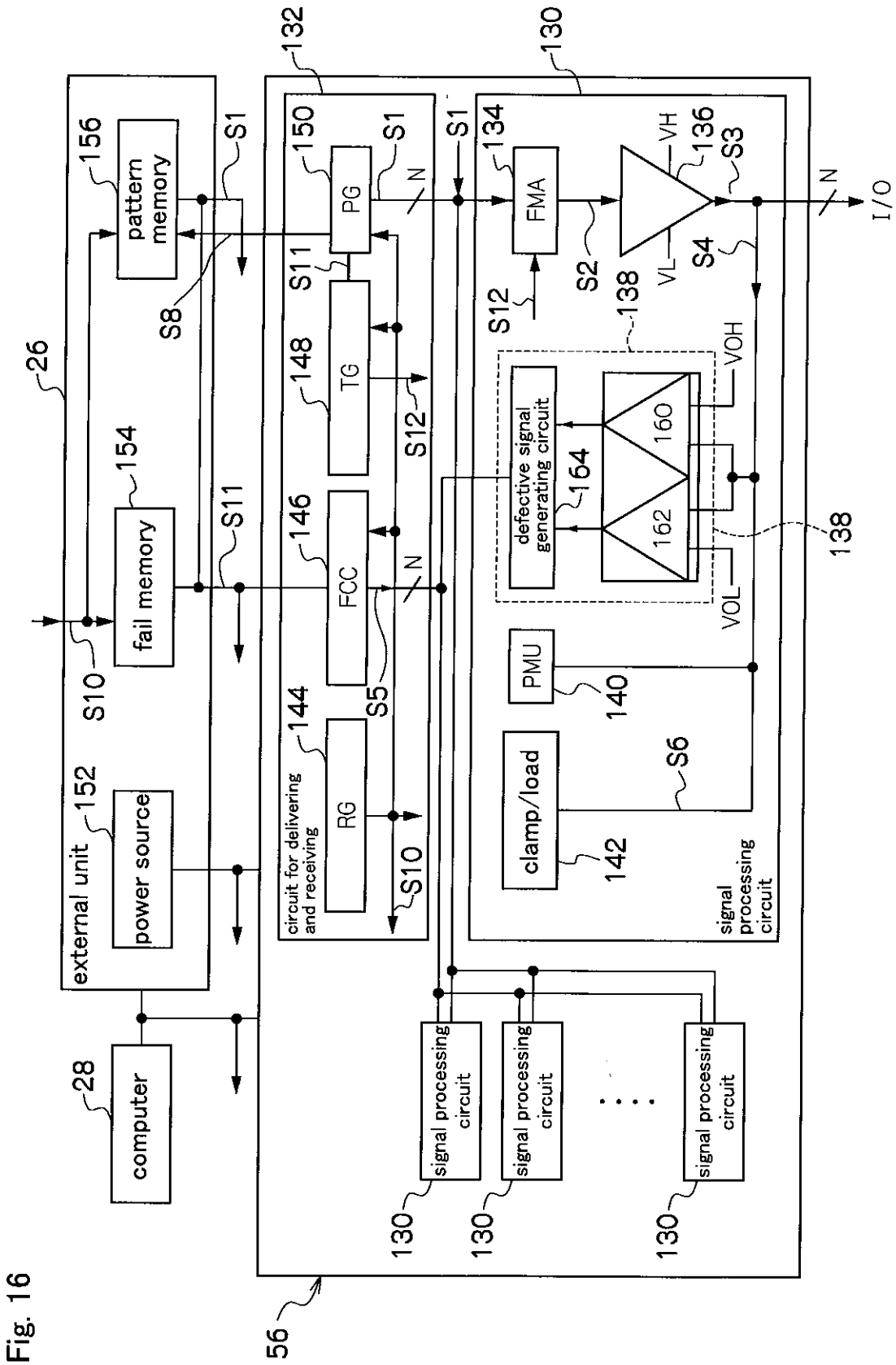

26
external unit
pattern memory
156
fail memory
154
power source
152
computer
28
S1
S8
S10
S11
132
150
PG
S1
N
S11
148
TG
S12
146
FCC
N
S5
144
RG
S10
circuit for delivering and receiving
130
134
FMA
S2
S12
VH
136
S3
VL
S4
N
I/O
138
defective signal generating circuit
164
160
162
VOH
VOL
138
PMU
140
clamp/load
142
S6
signal processing circuit
signal processing circuit
signal processing circuit
signal processing circuit
130
130
130
56

Fig. 17

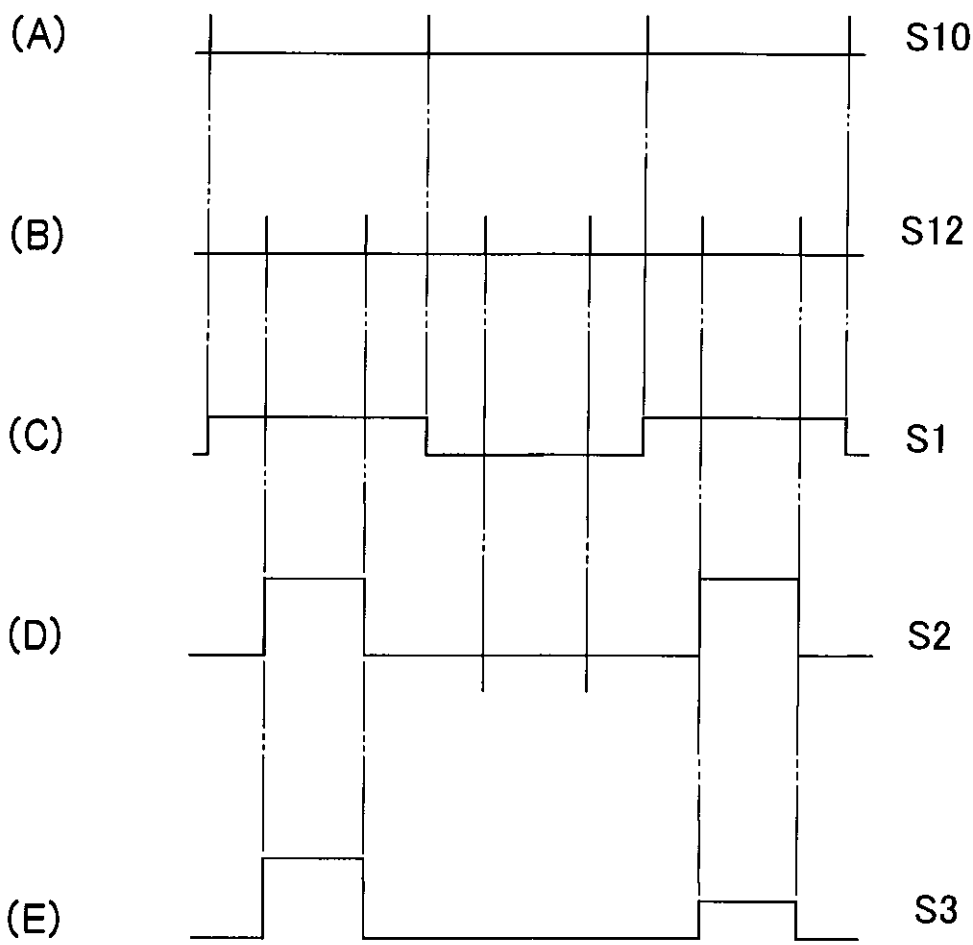
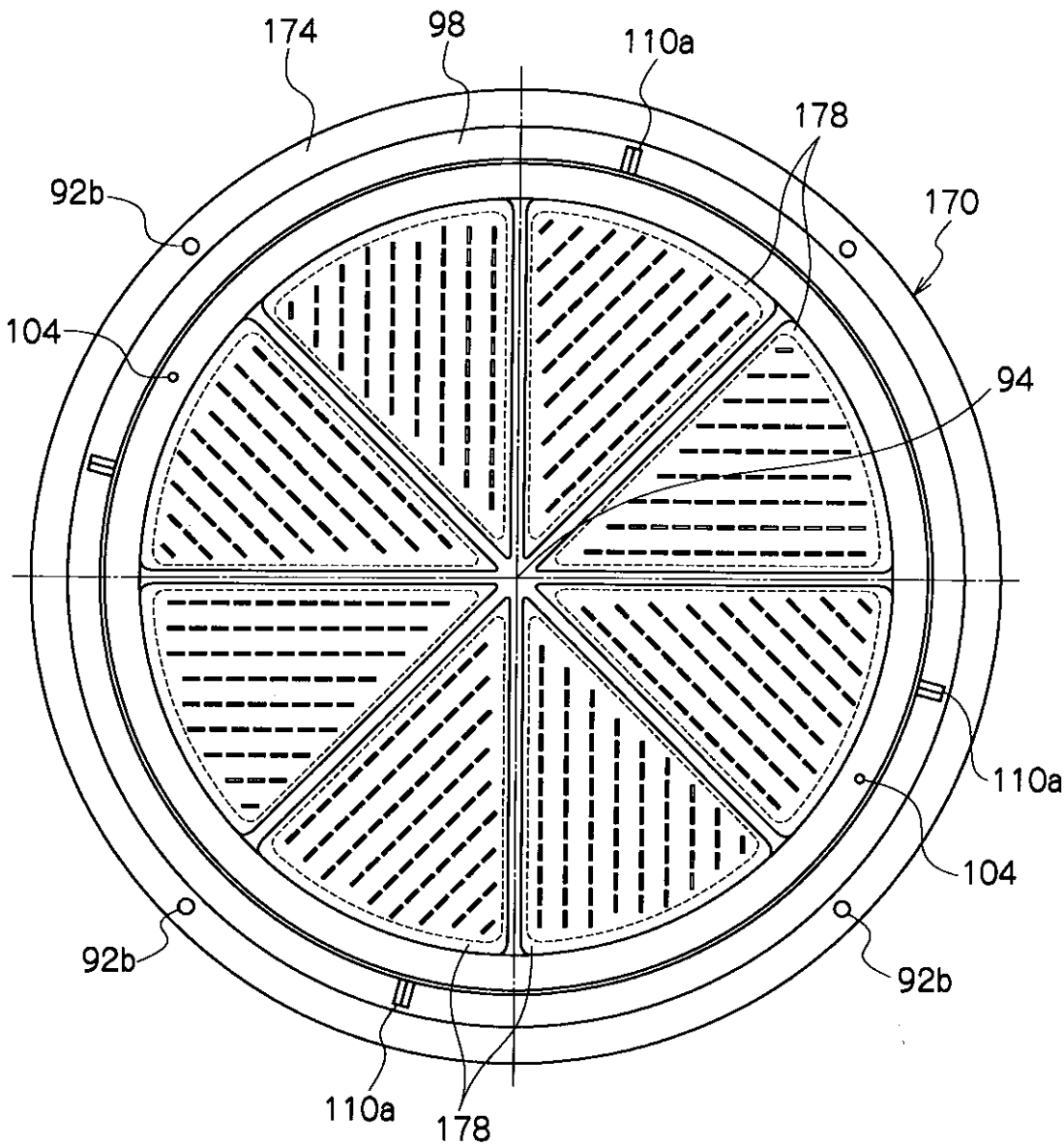


Fig. 18



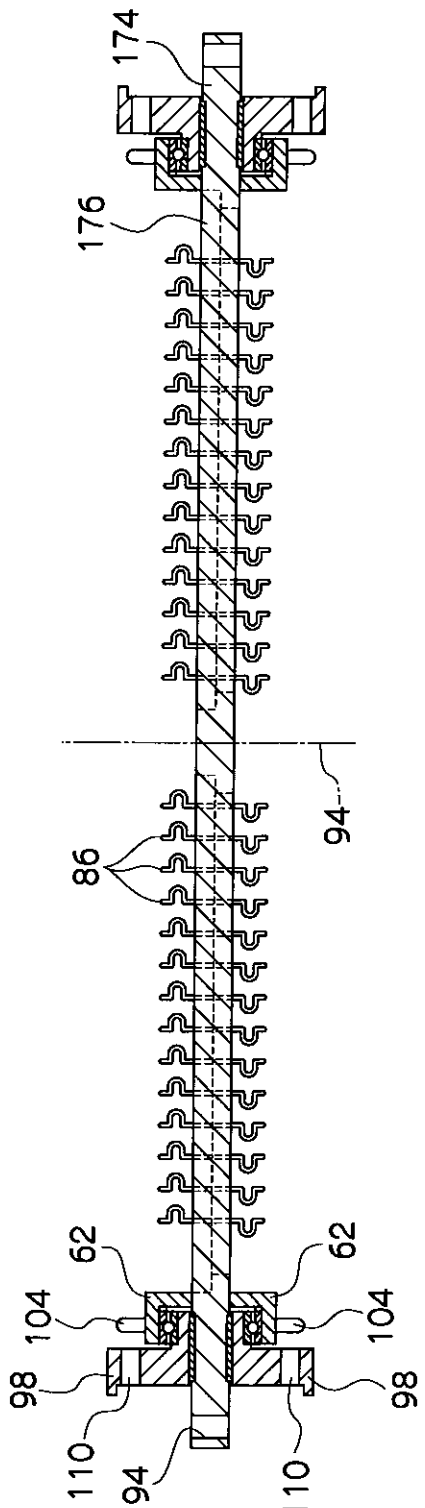
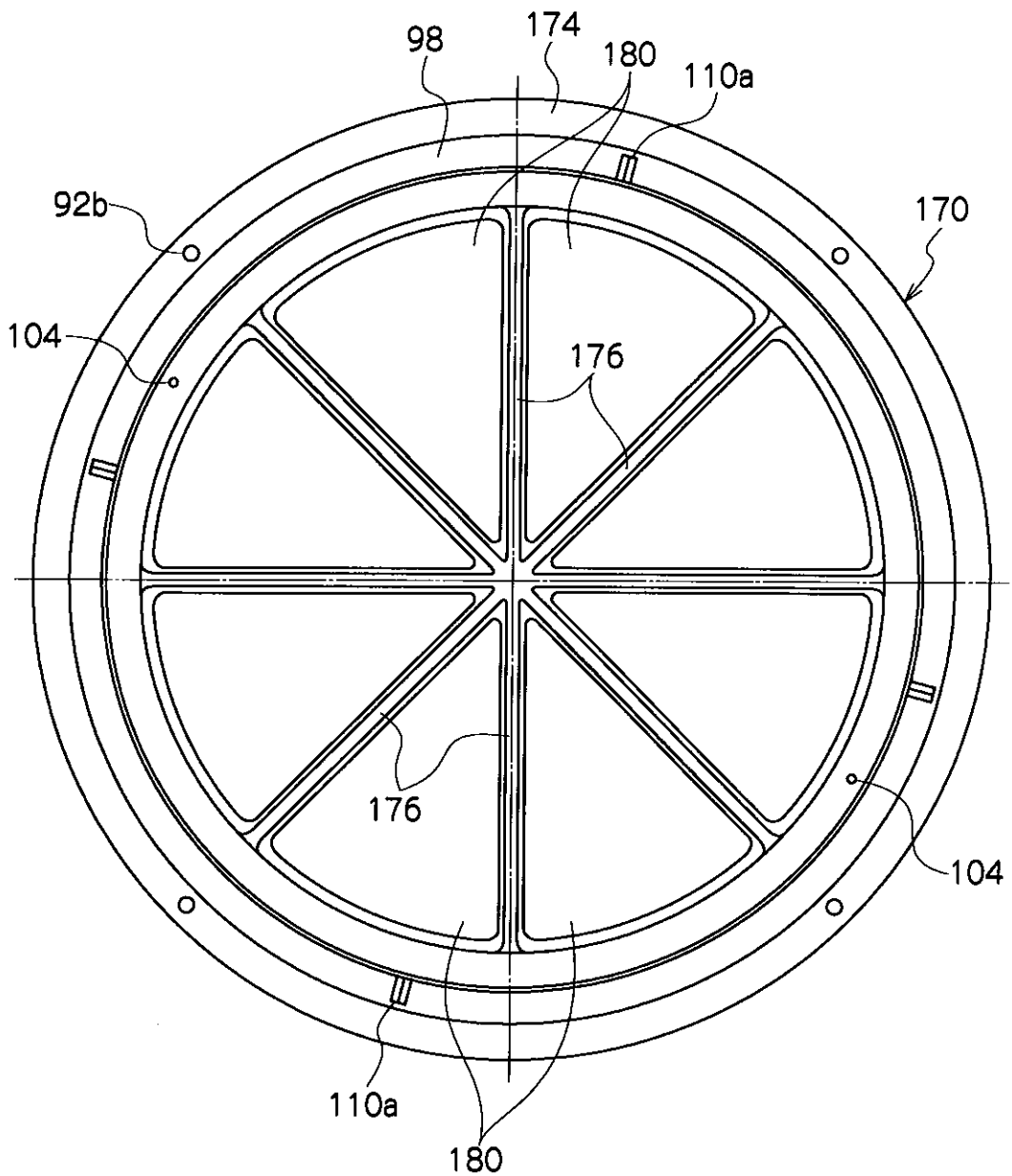


Fig. 19

Fig. 20



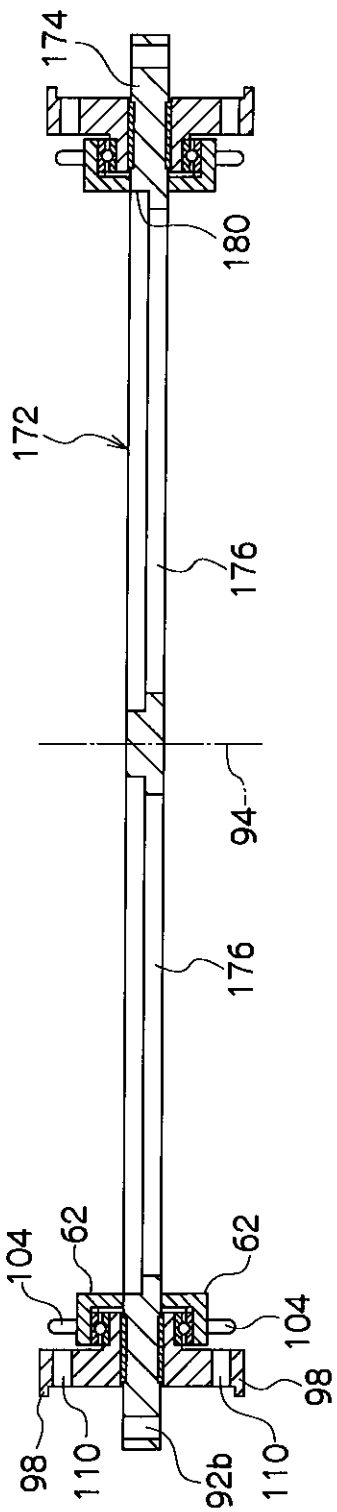


Fig. 21

Fig. 22

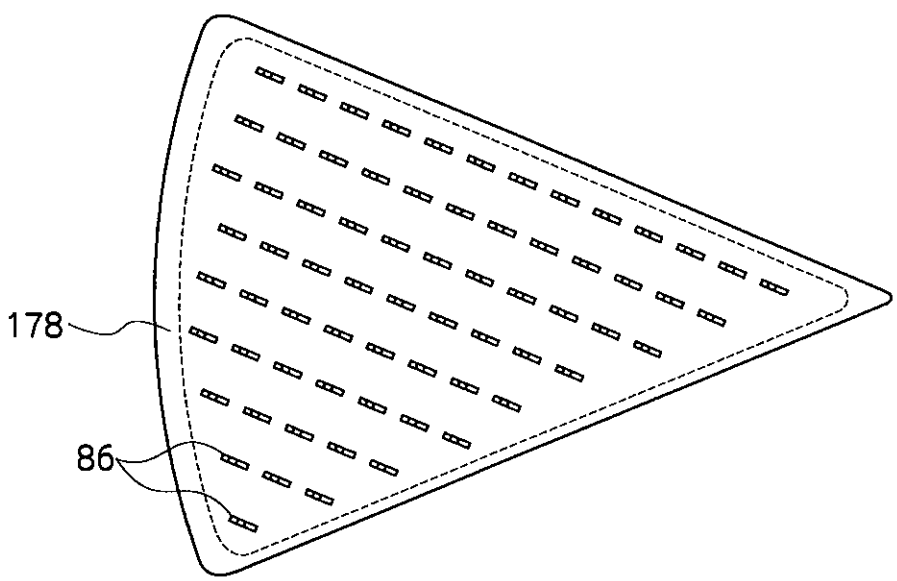


Fig. 23

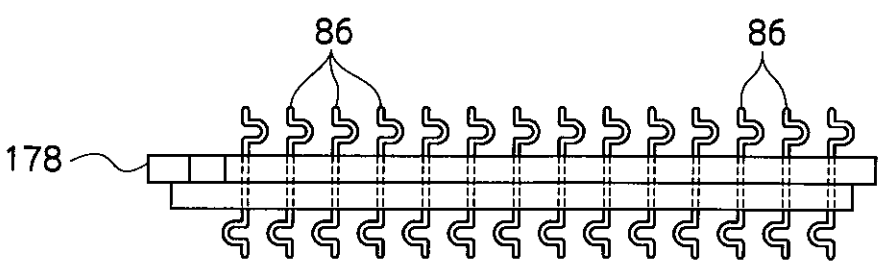


Fig. 24

