

WHAT IS CLAIMED IS:

1. A memory device comprising:
 - a substrate;
 - a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate, wherein each of the plurality of staircase structures comprises a plurality of conductor layers, wherein each of the plurality of conductor layers is located between two insulating layers;
 - a filling structure surrounding the multiple-stack staircase structure;
 - a semiconductor channel extending through the multiple-stack staircase structure, wherein the semiconductor channel comprises unaligned sidewall surfaces; and
 - a supporting pillar extending through at least one of the multiple-stack staircase structure and the filling structure, wherein the supporting pillar comprises aligned sidewall surfaces.
2. The memory device of claim 1, wherein the multi-stack staircase structure comprises a first staircase structure over the substrate and a second staircase structure over the first staircase structure.
3. The memory device of claim 2, wherein the supporting pillar extends from a top surface of the second staircase structure to a bottom surface of the first staircase structure.
4. The memory device of any one of claims 1-3, wherein the supporting pillar and the semiconductor channel comprise same filling layers.
5. The memory device of claim 4, wherein the supporting pillar and the semiconductor channel is each filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.
6. The memory device of any one of claims 1-3, wherein the supporting pillar and the semiconductor channel are filled with different filling layers.

7. The memory device of claim 6, wherein:
the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material; and
the semiconductor channel is filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.
8. The memory device of claim 7, wherein the insulating material comprises silicon oxide and the pillar-support material comprises at least one of copper, cobalt, nickel, and aluminum.
9. The memory device of claim 2, further comprising a joint insulating layer between the first staircase structure and the second staircase structure, and an insulating cap layer over the second staircase structure.
10. The memory device of any one of claims 2-9, further comprising a drain region over the semiconductor channel.
11. The memory device of claim 10, further comprising a connection layer in the semiconductor channel between two adjacent staircase structures, wherein the connection layer comprises a doped semiconductor material, and portions of the semiconductor channel separated by the connection layer each forms a semiconductor sub-channel.
12. A method for forming a memory device, comprising:
forming a plurality of dielectric stacks stacked on one another over a substrate to create a multiple-stack staircase structure, wherein each one of the plurality of dielectric stacks comprises a plurality of dielectric pairs arranged along a direction perpendicular to a top surface of the substrate;
forming a filling structure that surrounds the multiple-stack staircase structure;
forming a semiconductor channel extending through the multiple-staircase structure, wherein the semiconductor channel comprises unaligned sidewall surfaces; and

forming a supporting pillar extending through at least one of the multiple-staircase structure and the filling structure, wherein the supporting pillar comprises aligned sidewall surfaces.

13. The method of claim 12, wherein forming the supporting pillar comprises:
forming a photoresist layer over the at least one of the filling structure and the multiple-stack staircase structure;
patterning the photoresist layer to form a patterned photoresist layer with an opening that exposes a portion of the filling structure, wherein a location of the opening corresponds to a location of the supporting pillar;
using the patterned photoresist layer as an etch mask to etch through at least one of the filling structure and the multiple-stack staircase structure to form a pillar hole, wherein a bottom of the pillar hole contacts the substrate; and
filling the pillar hole with a first material.

14. The method of claim 13, wherein forming the semiconductor channel comprises:
forming a first sub-channel hole in a first dielectric stack of the plurality of dielectric stacks;
filling the first sub-channel hole with a sacrificial filling material to form a sacrificial filling structure;
forming a second dielectric stack over the first dielectric stack;
forming a second sub-channel hole in the second dielectric stack, wherein:
the second sub-channel hole aligns with the sacrificial filling structure along the direction perpendicular to the top surface of the substrate, and
the second sub-channel hole adjoins the first sub-channel hole to form a channel hole through the plurality of dielectric stacks and into the substrate;
removing the sacrificial filling structure in the first sub-channel hole; and
filling the channel hole with a second material.

15. The method of claim 14, wherein:

the first material is same as the second material and are formed by same fabrication operations; and

the same fabrication operations comprises depositing at least one of a charge trapping film, a semiconductor channel film, and a dielectric core into the channel hole and the pillar hole.

16. The method of claim 15, wherein the pillar hole is formed before a formation of the second sub-channel hole.

17. The method of claim 16, wherein the pillar hole is formed before the formation of the second sub-channel hole and after a formation of the sacrificial filling structure.

18. The method of claim 15, wherein the pillar hole is formed after a formation of the first sub-channel hole and a formation of the second sub-channel hole .

19. The method of claim 14, wherein the first material is different from the second material and is formed by a different deposition operation than the second material.

20. The method of claim 19, wherein the first material comprises at least one of an insulating material and a pillar-support material surrounded by the insulating material; and the second material comprises at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.

21. The method of claim 20, wherein the insulating material comprises silicon oxide and the pillar-support material comprises at least one of copper, cobalt, nickel, and aluminum.

22. The method of claim 12 or 13, wherein forming the semiconductor channel comprises:

forming a first semiconductor sub-channel in the first dielectric stack;

forming a connection layer over the first semiconductor sub-channel, wherein the connection layer comprises a doped semiconductor material; and

forming a second dielectric stack and a second semiconductor sub-channel in the second dielectric stack, wherein the second semiconductor sub-channel aligns with and adjoins the first semiconductor sub-channel to form a semiconductor channel extending through the plurality of dielectric stacks and into the substrate.

23. The method of claim 22, wherein:

forming the first semiconductor sub-channel comprises:

forming a first sub-channel hole in the first dielectric stack of the plurality of dielectric stacks; and

depositing a second material into the first sub-channel hole; and

forming the second semiconductor sub-channel hole comprises:

forming the second dielectric stack over the first dielectric stack of the plurality of dielectric stacks and a second sub-channel hole in the second dielectric stack; and

depositing the second material into the second sub-channel hole, wherein the second sub-channel hole aligns with and adjoins the first sub-channel hole along the direction perpendicular to the top surface of the substrate.

24. The method of claim 23, wherein:

the first material is same as the second material and are formed by same fabrication operations; and

the same fabrication operations comprises depositing at least one of a charge trapping film, a semiconductor channel film, and a dielectric core into the channel hole and the pillar hole.

25. The method of claim 24, wherein the pillar hole is formed before a formation of the second sub-channel hole.

26. The method of claim 25, wherein the pillar hole is formed after the formation of the first semiconductor sub-channel and before the formation of the second sub-channel hole.

27. The method of claim 24, wherein the pillar hole is formed after a formation of the first semiconductor sub-channel and the second sub-channel hole.

28. The method of claim 23, wherein the first material is different from the second material and is formed by a different deposition operation than the second material.

29. The method of claim 28, wherein the first material comprises at least one of an insulating material and a pillar-support material surrounded by the insulating material; and the second material comprises at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.

30. The method of claim 29, wherein the insulating material comprises silicon oxide and the pillar-support material comprises at least one of copper, cobalt, nickel, and aluminum.

31. The method of any one of claims 14-30, wherein the pillar hole is formed after a formation of the multiple-stack staircase structure and the first sub-channel hole.

32. A method for forming a memory device, comprising:

depositing a plurality of dielectric stacks over one another over a substrate to form a multiple-dielectric-stack structure, wherein each one of the plurality of dielectric stacks comprises a plurality of first material layer and second material layer alternatingly arranged along a direction perpendicular to a top surface of the substrate;

forming a first semiconductor sub-channel in a first dielectric stack of the plurality of dielectric stacks;

forming a second dielectric stack of the plurality of dielectric stacks over the first dielectric stack;

forming a second semiconductor sub-channel in the second dielectric stack, wherein the second semiconductor sub-channel aligns with the first semiconductor sub-channel along the direction perpendicular to the top surface of the substrate; and

patterning the multiple-dielectric-stack structure to form a multiple-stack staircase structure.

33. The method of claim 32, wherein patterning the multiple-dielectric-stack structure comprises a single staircase-forming patterning process.

34. The method of claim 33, wherein the staircase-forming patterning process comprises:

- forming a photoresist layer over the multiple-dielectric-stack structure;
- trimming the photoresist layer along a first direction parallel to a top surface of the substrate; and
- etching the multiple-dielectric-stack structure, using the trimmed photoresist layer as an etch mask to form a staircase.

35. The method of claim 32, wherein forming the first semiconductor sub-channel and the second semiconductor sub-channel comprise:

- forming a first sub-channel hole in the first dielectric stack and a second sub-channel hole in the second dielectric stack; and
- filling the first sub-channel hole and the second sub-channel hole each with channel-forming layers.

36. The method of claim 35, wherein the channel-forming layers comprise at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.

37. The method of any one of claims 32-36, further comprising:

- forming a joint insulating material layer between the first dielectric stack and the second dielectric layer;
- forming an opening in the joint insulating material layer to expose the first semiconductor sub-channel;

performing a recess etch to remove a top portion of the channel-forming layers of the first semiconductor sub-channel and form a recess region;
forming a connection layer in the recess region; and
patterning the joint insulating material layer to form a joint insulating layer.

38. The method of claim 37, wherein forming the connection layer comprises depositing a doped semiconductor material.

39. The method of claim 38, wherein the doped semiconductor material comprises doped silicon.

40. The method of any one of claims 32-39, further comprising forming a drain region over the second semiconductor sub-channel.