

Test system and test methodTechnical field

- 5 The present invention generally relates to the field of systems and methods for performing automated tests; in particular, the invention pertains to a test system for applying test stimuli and test measurements to at least one device to be tested.

Prior art

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Whenever a device is designed, it is also necessary to define a testing procedure to verify its correct operation at the end of production or during earlier steps such as prototype validation during the design step. In fact, any defects must be identified as early as possible to prevent the defective products from being released to the market. The same procedure, known as
15 functional testing, can also be used to determine characteristic parameters of the physically manufactured device and enable its classification into batches of differing quality levels.

The physical system used to apply a testing procedure to a physical device is known as a "test machine".

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Test machines are not necessarily dedicated systems designed exclusively for the functional testing of a single type of device but can be adapted as needed through configurability in terms of hardware (adding/removing physical modules) and software (programming the sequence of operations to be performed).

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In known technology, a significant gap exists regarding the transfer of information from the design step of a device to the automatic test machines by which a functional test must be applied to the designed device.

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In the prior art, this transfer is typically accomplished by a documentation written in human language, commonly referred to as the "functional test specification". It is widely accepted that the responsibility for defining this information is not clearly assigned.

Specifically, to verify the performance of a device, the "functional test specification" defines:

- the operations that must be performed;
- the sequence in which such operations must be performed.

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The use of a "functional test specification" written in human language to handle essential information for the testing step of a device results in considerable costs in terms of human resources and time required to adapt it to a corresponding test machine.

10 In fact, the "functional test specification" expressed in human language must be interpreted to configure and program a specific test machine.

What makes the aforementioned steps particularly burdensome giving rise to potential sources of errors is the fact that the use of non-formalized human language introduces ambiguity in interpretation. Moreover, the operator responsible for the conversion must have detailed knowledge of both the device to be tested and the test machine to be used, requiring therefore personnel with advanced engineering skills.

20 This ultimately translates into a waste of human resources and an extension of the time needed to achieve a correct functional test.

An improvement over the approach described so far consists of the preparation, by the test machine manufacturer, of algorithms sufficiently generic to be applicable to entire families of devices to be tested (e.g., diodes, IGBTs, half-bridge modules) and the creation of a user interface that allows the desired algorithm to be selected and its characteristic parameters (e.g., voltage or current values, pass/fail criteria, test durations) to be introduced. The advantage of this solution is that the "programming", understood as software development, is performed once and for all by the test machine manufacturer, while the manufacturer of the device to be functionally tested can create the desired sequence without any knowledge of the test machine or software programming. This solution reduces the time required to develop test programs but has the drawback of not allowing the user to independently modify the stimulus/measurement.

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An alternative approach, inspired by similar considerations, is based on the use of a formal language for defining the test sequence. This sequence is then converted into a sequence of elementary operations, variable depending on the test machine used to execute the functional
5 test. The manufacturer of the device to be tested must create the test sequence in formal language, while the test machine manufacturer must develop the program to convert the formal language into elementary instructions for the test machine.

In any case, all current solutions are tightly dependent on the test configuration for which
10 the test sequence was optimized, and any change to the test machine configuration, such as the level of parallelism at which the test must be executed, necessarily requires repeating the entire method, which is costly in terms of human resources and time.

Finally, none of the proposed solutions can automatically respond to events such as failures
15 of sub-parts of the test machine, nor can they leverage a possible over-dimensioning of the test machine to automatically minimize the total time required for performing the functional test.

A first solution aiming to address the aforementioned issues is described, for example, in
20 CN101896908 B. However, this solution is limited in that its implementation logic is based solely on information contained in a test document. Therefore, relying exclusively on the information related to the test to be performed does not allow for optimization of the use of available test resources provided by a potential test machine for performing the test.

25 Thus, even considering CN101896908 B, the aforementioned problems remain unresolved.

Additionally, existing test systems managed by a single software implementation, which implements stimuli and measurements based on the test resources for which they were designed, are unable to implement generic stimuli or optimize the execution of such stimuli for
30 test execution.

A recently developed "data-driven" test method has been introduced to overcome the

disadvantages of the previously described methods.

- In particular, in a "data-driven" test method, an operator does not (unless explicitly desired) need to define a chronological sequence of operations constituting the functional test. The operator also does not need to be limited to a finite number of existing stimulus and measurement tools in a real test system. The "data-driven" method provides for the optimization of the use of physical resources present in the test system through the definition of the sequence in which the functional test will be executed.
- However, existing known test systems do not feature architectures capable of adapting to or being used with such a "data-driven" test method.

Summary of the Invention

- An object of the present invention is to provide a test system with an optimized hardware architecture for performing functional tests.
- A further object is to provide a test system suitable for implementing "data-driven" test methods.
- The above and other objects and advantages are achieved, according to one aspect of the invention, by a test system for applying test stimuli and test measurements to at least one device to be tested, having the features defined in claim 1. Preferred embodiments of the invention are defined in the dependent claims, the content of which is to be understood as an integral part of the present description.

Brief description of the drawings

- The functional and structural characteristics of certain preferred embodiments of a test system for applying test stimuli and test measurements to at least one device to be tested according to the invention will now be described. Reference is made to the accompanying drawings, wherein:

- Figure 1 illustrates a first embodiment of a test system according to the present invention;
- Figure 2 illustrates a second embodiment of a test system according to the present invention;
- 5 - Figure 3 illustrates, by way of example, a connection of test logic components to a generic device to be tested;
- Figure 4 illustrates an exemplary implementation of a test module.

Detailed description

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Before detailing a plurality of embodiments of the invention, it should be clarified that the invention is not limited in its application to the structural details and configuration of components presented in the following description or illustrated in the drawings. The invention is capable of assuming other embodiments and being implemented or practically realized in various ways. It should also be understood that the phraseology and terminology are intended for descriptive purposes only and should not be construed as limiting. The use of the terms "include" and "comprise" and their variations are to be understood as encompassing the elements stated hereafter and their equivalents, as well as additional elements and their equivalents.

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Referring initially to Figure 1, a first embodiment of a test system 200 for applying test stimuli and test measurements to at least one device under test (DUT) is described hereafter.

The device under test (DUT) may be any device, such as, for example, an electronic device, a semiconductor device, a mechanical device, a pneumatic device, an optical device, etc.

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For instance, in the field of semiconductor devices, the following test functions, among others, may be performed: direct current tests, alternating current tests, time-domain tests, etc.

In general, a test function can be defined by test stimuli and test measurements to be applied to the device under test (DUT).

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According to a first embodiment, the test system 200 comprises electronic control (or processing) means 202 and a plurality of test modules 204.

For example, the electronic control means 202 may comprise or be at least one of the following: a processor, a microprocessor, a controller, a microcontroller, an FPGA, a PLC, or similar devices.

By way of example, a test module can be understood as an object capable of applying at least one test stimulus to the DUT and optionally applying/acquiring at least one test measurement to/from the DUT.

The test system 200 further comprises:

- a first communication network 206 arranged to enable communication between said electronic control means 202 and said plurality of test modules 204, at a first communication speed; and

- a second communication network 208 arranged to enable communication between said plurality of test modules 204 at a second communication speed, with a latency lower than a maximum latency.

The value of the maximum latency is a function of the discretization time of the test stimuli and test measurements to be applied via the test system.

In general, discretization time can be understood as the time interval between a test stimulus and an immediately subsequent test measurement, or the time interval between a first test stimulus and an immediately subsequent second test stimulus, or still the time interval between a first test measurement and an immediately subsequent second test measurement, or the minimum time between them.

For instance, the maximum latency value is lower than the discretization time as defined above.

In other words, the test system 200 has an architecture that can be defined as a "Dual Layer

Scalable Architecture". In general, in the first embodiment described earlier, two distinct communication infrastructures, or networks, coexist within the test system.

Preferably, the first communication speed of the first communication network may be in the
5 range of Megabits per second or Gigabits per second. For example, the first communication speed could range between 100Mb/s and 1Gb/s, or between 1Gb/s and 10Gb/s, and so on.

In one example, the first communication network 206 (i.e., a first communication channel) could have a tree architecture, based on the Ethernet standard, for instance, wherein a "TOP"
10 node can be identified, corresponding to the electronic control means 202. This "TOP" node may be connected, potentially through intermediate nodes not represented in Figure 1, to the test modules 204. As previously described, the first communication network 206 may feature high bandwidth but without real-time requirements. The bandwidth can be intrinsically scalable, as it is sufficient to change the type of communication standard used to enhance its
15 performance.

Conversely, the second communication network 208 could have an architecture based, for example, on the EtherCAT standard, which can connect all the test modules 204. As previously described, the second communication network 208 (i.e., a second communication
20 channel) does not require high bandwidth but must have real-time characteristics, i.e., low latency. The second communication network 208 can also be intrinsically scalable; for example, in the case of EtherCAT, scalability can be achieved by transitioning from EtherCAT to EtherCAT-G or EtherCAT-G10.

25 An embodiment of a second communication network 208 with an exemplary ring architecture is illustrated, for example, in Figure 2.

Preferably, the electronic control means 202 are arranged to transmit, via said first communication network 206, at least one test instruction to at least one test module of said plurality
30 of test modules 204.

In other words, the first communication network 206 can be used to transfer the "threads"

related to the steps to be executed to at least one test module or to each test module. Each "thread" can contain one or more test instructions (e.g., a sequence of test instructions) that must be executed by the at least one test module in order to perform a subset of the overall test.

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Each test module, upon receiving its respective test instruction, may be arranged to determine at least one test stimulus and/or at least one test measurement to be applied to said at least one device under test (DUT), depending on said at least one test instruction received.

10 In such a case, the second communication network 208 can be arranged to enable the sharing of a common time information among said plurality of test modules 204. The time information is arranged to allow said plurality of test modules 204 to define a common reference time.

15 In general, the second communication network 208 can be used to create time synchronization among all the test modules 204. In other words, the second communication network 208 can ensure that all objects in the test system have the same concept of "time" regardless of the complexity of the test system 200.

20 The at least one test module that has received said at least one test instruction may be arranged to apply said at least one test stimulus and/or said at least one test measurement to said at least one device under test (DUT) at an application time instant determined as a function of said common reference time.

25 Preferably, via the second communication network 208, at least one test module of said plurality of test modules 204 may be arranged to transmit its own status information to at least one additional test module of said plurality of test modules 204.

The status information can be an information indicating whether such test module has completed or not completed the application of said at least one test stimulus and/or said at least one test measurement.

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Preferably, the plurality of test modules 204 may comprise a primary test module arranged to transmit, via said second communication network 208, at least one test control information to at least one other test module of said plurality of test modules 204.

- 5 Preferably, the test control information is arranged to indicate the need to initiate the application of at least one test stimulus and/or at least one test measurement.

10 In general, the second communication network 208 can therefore be used to periodically transfer status and control information related to each individual test module 204. For example, each object "publishes" on the data packet traversing the ring (i.e., the second communication network) whether it has completed the current step or not. Alternatively, a "master" node sends a "start" signal to all test modules 204 to initiate a specific sequence of steps/instructions.

- 15 Preferably, via the first communication network 206, at least one test module of said plurality of test modules 204 may be arranged to transmit its own data information to said electronic control means 202.

20 In general, the first communication network 206 can therefore be used to collect data information (i.e., data) acquired during the execution of the test from one or more of the test modules 204. By definition, the test modules 204 can read all available quantities from the device under test (DUT), acquiring them with the highest possible resolution. Subsequently, only the data information that is actually to be used within the test can be transferred to the electronic control means 202 (i.e., the "TOP" node). This operation can be performed at the
25 end of the execution of each "thread".

30 Preferably, via the second communication network 208, at least one test module of said plurality of test modules 204 may be arranged to transmit its own data information to at least one other test module of said plurality of test modules 204.

Preferably, the data information can be an information indicating a value caused by at least one test stimulus applied by said test module or a value measured by a test measurement

applied by said test module.

Preferably, the at least one test module receiving the data information and the status information from at least one other test module may be arranged to determine at least one subsequent test stimulus or at least one subsequent test measurement to be applied, depending on the received status and data information.

In general, the second communication network 208 can thus be used to periodically transfer data information, such as point values measured and/or generated for voltage or current. In this way, feedback loops can be implemented between test modules 204, although with temporal quantization. One possible use case is the creation of signals dependent on real-time measurements.

Preferably, via the second communication network 208, at least one test module of said plurality of test modules 204 may be arranged to transmit at least one control/command information to at least one test logic component 300, which is provided by said at least one test stimulus or said at least one test measurement determined according to the test instruction.

In this case, the test logic component 300 must be connected to the device under test (DUT) during the application of said at least one test stimulus and/or said at least one test measurement.

Figure 3 illustrates, by way of example, test logic components that can be connected to the device under test (DUT) during the application of test stimuli and test measurements.

For instance, to define the test logic components 300, reference can be made to libraries of modules (generators, measuring devices, passive components) used to define the type of test to be performed. Such test logic components can be configured to be associated/connected to the device under test (DUT).

In general, the test modules 204 may communicate in turn with any possible physical generators or acquisition devices that will be connected to the device under test (DUT), for

example, via a programmable interconnection matrix.

Preferably, each test module may comprise respective second electronic control means.

- 5 Preferably, the second electronic control means may each comprise at least one of the following:

- a high-performance processor, with a non-real-time operating system;
- a low-performance processor, with a real-time operating system;
- an FPGA capable of managing high-speed communications.

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Preferably, the second electronic control means may each comprise all three elements listed above.

For example, high performance may refer to clock frequencies on the order of GHz. The
15 non-real-time operating system of the high-performance processor may, for instance, be Linux. This processor can handle high-speed communication and any requests for processing the acquired data.

As an example, lower performance may refer to clock frequencies in the range of tens or
20 hundreds of MHz. The real-time operating system of the lower-performance processor may, for instance, be FreeRTOS. This processor can manage high-resolution time synchronization with minimal latency and process packets received in real-time from the second communication network 208 (e.g., the ring communication channel).

25 For example the FPGA capable of managing high-speed data channels may be used to store the data acquired from the device under test (DUT) in a local buffer. These data would then need to be processed and transmitted via the aforementioned high-performance processor with a non-real-time operating system to the electronic control means 202 of the test system (i.e., the "TOP" node).

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Referring now to Figure 4, an exemplary implementation of a possible test module for the test system is described.

The test module may comprise a high-performance processor (on the left in Figure 4), connected to a Gigabit Ethernet interface (top left in Figure 4). On the right, there is a Real-time processor connected to the EtherCAT network (top right in Figure 4). In the center, an FPGA is shown, used to connect the two processing units to both the I/O modules (bottom center in Figure 4) and the data buffers (top center in Figure 4), managing shared access to the information appropriately.

The following describes an exemplary implementation of a test method for applying test stimuli and test measurements to at least one device under test (DUT), carried out through the test system.

The method may comprise the following steps:

- transmitting, via a first communication network with a first communication speed, at least one test instruction from the electronic control means to at least one test module of a plurality of test modules connected to said first communication network;
- sharing common time information among said plurality of test modules via a second communication network with a second communication speed and latency lower than a maximum latency, wherein the value of the maximum latency is a function of a discretization time of the test stimuli and test measurements to be applied by the test system;
- defining a common reference time for said test modules based on said common time information;
- using the at least one test module that has received said test instruction:
 - i) determining at least one test stimulus and/or at least one test measurement to be applied to said at least one device under test (DUT) based on said received test instruction;
 - ii) applying said determined at least one test stimulus and/or said determined at least one test measurement to said at least one device under test (DUT) at an application time instant determined as a function of said common reference time.

As described earlier for the test system 200, also for the method just described, the first communication speed may similarly be in the range of Megabits per second or Gigabits per

second.

What has been previously described for the test system 200, and not repeated here, may find analogous application to the test method just described.

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The advantages achieved by the present invention are therefore as follows:

- providing a test system with an optimized hardware architecture for performing functional tests;
- providing a test system suitable for implementing "data-driven" test methods.

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Various aspects and embodiments of a test system for applying test stimuli and test measurements to at least one device under test, according to the invention, have been described.

It is intended that each embodiment may be combined with any other embodiment. Furthermore, the invention is not limited to the described embodiments but may be modified within

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the scope defined by the appended claims.

CLAIMS

1. Test system (200) for applying test stimuli and test measurements on at least one device to be tested (DUT), comprising:
- 5 - electronic control means (202) and a plurality of test modules (204);
- a first communication network (206) arranged to enable communication between said electronic control means (202) and said plurality of test modules (204), according to a first communication speed;
- a second communication network (208) arranged to allow communication between
- 10 said plurality of test modules (204) at a second communication speed with latency less than a maximum latency;
- the value of the maximum latency being a function of a discretization time of the test stimuli and the test measurements to be applied by the test system.
- 15 2. Test system (200) according to claim 1, wherein the first communication speed is in the order of Megabits per second or Gigabits per second.
3. Test system (200) according to any one of the preceding claims, wherein said electronic control means (202) are arranged to transmit, via said first communication network
- 20 (206), at least one test instruction to at least one test module of said plurality of test modules (204);
- wherein each test module, when receiving a respective test instruction, is arranged to determine at least one test stimulus and/or at least one test measure to be applied on said at least one device to be tested (DUT), depending on said at least one test instruction received;
- 25 wherein said second communication network (208) is arranged to allow sharing of a common time information between said plurality of test modules (204);
- wherein said time information is arranged to allow said plurality of test modules (204) to define a common reference time;
- wherein said at least one test module that has received said at least one test instruction
- 30 is arranged to apply said at least one test stimulus and/or said at least one test measurement to said at least one device to be tested (DUT), at an application time instant determined as a function of said common reference time.

4. Test system (200) according to any one of the preceding claims, wherein, via said second communication network (208), at least one test module of said plurality of test modules (204) is arranged to transmit its own status information to at least one further test module of said plurality of test modules (204).

5. Test system (200) according to claim 4, wherein said status information is an information indicative of whether or not said test module has completed the application of said at least one test stimulus and/or said at least one test measure.

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6. Test system (200) according to any one of the preceding claims, wherein said plurality of test modules (204) comprises a primary test module arranged to, via said second communication network (208), transmit at least one test control information to at least one other test module of said plurality of test modules (204).

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7. Test system (200) according to claim 6, wherein said test control information is arranged to indicate the need to initiate the application of at least one test stimulus and/or test measure.

20 8. Test system (200) according to any one of the preceding claims, wherein, via the first communication network (206), at least one test module of said plurality of test modules (204) is arranged to transmit its own data information to said electronic control means (202).

25 9. Test system (200) according to any one of the preceding claims, wherein, via said second communication network (208), at least one test module of said plurality of test modules (204) is arranged to transmit its own data information to at least one other test module of said plurality of test modules (204).

30 10. Test system (200) according to claim 8 or 9, wherein said data information is an information indicative of a value caused by at least one test stimulus applied by said test module or a value measured by a test measure applied by said test module.

11. Test system (200) according to claim 9 or 10, when dependent on claim 4 or 5, wherein the at least one test module receiving the data information and the status information from the at least one other test module is arranged to:

- determine at least one subsequent test stimulus or at least one subsequent test measure to be applied, depending on the received state information and data information.

12. Test system (200) according to any one of the preceding claims, wherein, via said second communication network (208), at least one test module of said plurality of test modules (204) is arranged to transmit at least one control information to at least one test logic component (300) which is provided by said at least one test stimulus or said at least one test measure determined according to said test instruction,

wherein said test logic component (300) is to be connected to the device to be tested (DUT) during the application of said at least one test stimulus and/or said at least one test measure.

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13. Test system (200) according to any of the preceding claims, wherein each test module comprises respective second electronic control means.

14. Test system (200) according to claim 13, wherein the second electronic control means each comprise at least one of:

- a high-performance processor, with a non-real-time operating system;
- a low-performance processor, with a real-time operating system;
- an FPGA capable of handling high-speed communications.

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