

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a plurality of channel structures on a substrate, each channel structure of the plurality of channel structures extending in a first direction perpendicular to an upper surface of the substrate, and having a gate insulating layer and a channel layer;

a common source extension region between the substrate and the plurality of channel structures, the common source extension region including a first semiconductor layer having an n-type conductivity;

a plurality of gate electrodes on the common source extension region and spaced apart from each other on a sidewall of each of the plurality of channel structures in the first direction; and

a common source region on the substrate, the common source region being in contact with the common source extension region and including a second semiconductor layer having an n-type conductivity,

wherein the gate insulating layer of each of the plurality of channel structures extends to cover an upper surface and at least a portion of a bottom surface of the common source extension region.

2. The semiconductor device as claimed in claim 1, wherein a portion of the gate insulating layer extends from a sidewall of the channel layer, and the portion of the gate insulating layer covers the upper surface, a sidewall, and a portion of the bottom surface of the common source extension region.

3. The semiconductor device as claimed in claim 1 or claim 2, wherein a portion of the bottom surface of the common source extension region is in contact with the common source region.

4. The semiconductor device as claimed in any one of claims 1 to 3, wherein an upper surface of the second semiconductor layer is at a level that is lower than or identical to the upper surface of the common source extension region.

5. The semiconductor device as claimed in any one of claims 1 to 4, further comprising:

a base layer between the common source extension region and the substrate and having an n-type conductivity; and

a lower insulating layer between the base layer and the common source extension region.

6. The semiconductor device as claimed in claim 5, wherein a bottom surface of the common source region is at an identical level as a bottom surface of the base layer, and

the plurality of channel structures are electrically insulated from the substrate by the lower insulating layer.

7. The semiconductor device as claimed in claim 5 or claim 6, wherein a portion of the gate insulating layer is between the common source extension region and the lower insulating layer.

8. The semiconductor device as claimed in any one of claims 5 to 7, wherein an undercut region is in a portion of the lower insulating layer between the common source extension region and the base layer, and the common source region includes a protrusion that fills the undercut region and contacts the lower insulating layer.

9. The semiconductor device as claimed in any one of claims 1 to 8, wherein the common source region further includes a support layer that is on the second semiconductor layer, spaced apart from the common source extension region, and electrically connected to the common source extension region via the second semiconductor layer of the common source region.

10. The semiconductor device as claimed in claim 9, wherein an upper surface of the support layer is at a higher level than the upper surface of the common source extension region.

11. The semiconductor device as claimed in claim 9 or claim 10, further comprising a common source line on the common source region, wherein the support layer surrounds a lower sidewall of the common source line.

12. A semiconductor device, comprising:
a base layer on a substrate and having an n-type conductivity;
a common source extension region on the base layer and including a first semiconductor layer having an n-type conductivity;

a plurality of channel structures on the common source extension region and extending in a first direction perpendicular to an upper surface of the substrate, each of the plurality of channel structures having a gate insulating layer and a channel layer;

a plurality of gate electrodes on the common source extension region and spaced apart from each other on a sidewall of each of the plurality of channel structures in the first direction; and

a common source region on the substrate, the common source region being in contact with a portion of a bottom surface of the common source extension region and including a second semiconductor layer having an n-type conductivity,

wherein a portion of the gate insulating layer of each of the plurality of channel structures extends to cover an upper surface and at least a portion of the bottom surface of the common source extension region.

13. The semiconductor device as claimed in claim 12, further comprising a lower insulating layer between the base layer and the common source extension region, the plurality of channel structures being electrically insulated from the substrate by the lower insulating layer.

14. The semiconductor device as claimed in claim 13, wherein an undercut region is in a portion of the lower insulating layer between the common source extension region and the base layer, the common source region including a protrusion that fills the undercut region and contacts the lower insulating layer.

15. The semiconductor device as claimed in any one of claims 12 to 14, wherein a bottom surface of the common source region is at an identical level as a bottom surface of the base layer.

16. The semiconductor device as claimed in any one of claims 12 to 15, wherein the common source region includes a support layer on the second semiconductor layer and having an upper surface that is at a higher level than the upper surface of the common source extension region.

17. A method of manufacturing a semiconductor device, the method comprising:

forming a sacrificial layer on a substrate;

forming a gate mold structure on the sacrificial layer, the gate mold structure including a plurality of first material layers and a plurality of second material layers that are alternately arranged;

forming a plurality of channel holes passing through the gate mold structure to expose the sacrificial layer;

forming a first recess by removing the sacrificial layer;

forming a gate insulating layer on an inner wall of the first recess and an inner wall of the plurality of channel holes;

forming a common source extension region by filling the first recess with a first semiconductor layer having n-type conductivity;

forming a common source opening portion passing through the gate mold structure; and

forming a common source region by filling a bottom portion of the common source opening portion with a second semiconductor layer having n-type conductivity; wherein the common source region is in contact with the common source extension region.

18. The method as claimed in claim 17, wherein forming the common source extension region includes filling an inner portion of the first recess with the first semiconductor layer.

19. The method as claimed in claim 17 or claim 18, further comprising, before forming the sacrificial layer, forming a base layer having an n-type conductivity on the substrate,

wherein the method further comprises, after forming the common source opening portion, expanding the bottom portion of the common source opening portion by removing a portion of the base layer exposed through the common source opening portion, and

wherein the common source region fills the expanded bottom portion of the common source opening portion.

20. The method as claimed in any one of claims 17 to 19, further comprising, before forming the gate mold structure, forming a support layer that is laterally spaced apart from the sacrificial layer on the substrate,

wherein forming the common source opening portion includes forming the common source opening portion such that the common source opening portion passes through the gate mold structure and at least a portion of the support layer is removed.