WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate;

a first logic cell disposed on the substrate and including a first active pattern;

a second logic cell disposed on the substrate and including a second active pattern;

a first gate electrode extending in a first direction and disposed on the first logic cell;

a second gate electrode extending in the first direction and disposed on the second logic cell;

a power line extending in a second direction at a boundary between the first and second logic cells, the second direction being perpendicular to the first direction; and

a connection structure electrically connecting the power line to the first active pattern and to the second active pattern,

wherein the connection structure is disposed below the power line and extends from the first logic cell to the second logic cell,

wherein the connection structure is electrically isolated from the first and second gate electrodes,

a top surface of the connection structure is at a higher level than that of a top surface of the first gate electrode, and

wherein the connection structure comprises:

a first contact portion disposed on the first active pattern;

a second contact portion disposed on the second active pattern; and

a bridge portion connecting the first contact portion to the second contact

portion, and extending in a zigzag path at the boundary between the first and second logic cells, in plan view.

2. The semiconductor device of claim 1, wherein the second gate electrode is aligned in the first direction with the first gate electrode, and

the connection structure runs between the first gate electrode and the second gate electrode, in plan view.

3. The semiconductor device of claim 1, further comprising an insulation pattern between and separating the first gate electrode and the second gate electrode,

wherein the connection structure crosses over the insulation pattern.

4. The semiconductor device of claim 1, wherein the second contact portion is offset from a virtual line in the second direction, and

the virtual line runs across a center of the first contact portion and extends in the first direction.

5. The semiconductor device of claim 1, wherein the connection structure comprises:

a plurality of first contact portions including the first contact portion and disposed on the first active pattern;

a plurality of second contact portions including the second contact portion and disposed on the second active pattern; and

wherein the bridge portion connects the plurality of first contact portions to the plurality of second contact portions.

6. The semiconductor device of claim 1, wherein the first active pattern and the first gate electrode constitute a first transistor, and

the second active pattern and the second gate electrode constitutes a second transistor, the first and second transistors having the same conductivity.

7. The semiconductor device of claim 1, further comprising a via between the power line and the connection structure,

wherein the via has a bar shape extending in a third direction that are perpendicular to the first and second direction, in plan view, and

the connection structure has a portion below the via, the portion of the connection structure extending in the third direction.

8. The semiconductor device of claim 1, wherein the first active pattern comprises:

a first channel region disposed below the first gate electrode; and

a plurality of first source/drain regions disposed at opposite sides of the first channel region,

wherein the second active pattern comprises:

a second channel region disposed below the second gate electrode; and

a plurality of second source/drain regions disposed at opposite sides of the second channel region, and

wherein the connection structure connects the plurality of first source/drain regions to the plurality of second source/drain region.

9. A semiconductor device, comprising:

a substrate;

a first logic cell disposed on the substrate and including a first active pattern;

a second logic cell disposed on the substrate and including a second active pattern;

a first gate electrode extending in a first direction and disposed on the first logic cell;

a second gate electrode extending in the first direction and disposed on the second logic cell;

a power line extending in a second direction at a boundary between the first and second logic cells, the second direction being perpendicular to the first direction; and

a connection structure electrically connecting the power line to the first active pattern and to the second active pattern,

wherein the connection structure is electrically isolated from the first and second gate electrodes,

wherein the connection structure comprises:

a first contact portion disposed on the first active pattern;

a second contact portion disposed on the second active pattern; and

a bridge portion connecting the first contact portion to the second contact portion,

wherein the second gate electrode is aligned in the first direction with the first gate electrode,

wherein the bridge portion is disposed between the first gate electrode and the second gate electrode, in plan view, and

wherein the bridge portion extends in a zigzag path at the boundary between the first and second logic cells, in plan view.

10. The semiconductor device of claim 9, further comprising an insulation pattern between and separating the first gate electrode and the second gate electrode,

wherein the bridge portion crosses over the insulation pattern.

11. The semiconductor device of claim 9, further comprising a device isolation layer disposed between the first and second logic cells,

wherein the bridge portion is disposed on the device isolation layer.

12. The semiconductor device of claim 9, further comprising:

an active contact connected to the first active pattern and the second active pattern; and

an electrical line provided on and electrically connected to the active contact,

wherein a top surface of the connection structure and a top surface of the active contact are positioned at the same level, and

wherein a top surface of the power line and a top surface of the electrical line are positioned at the same level.

13. The semiconductor device of claim 9, wherein the first active pattern comprises:

a first channel region disposed below the first gate electrode; and

a plurality of first source/drain regions disposed at opposite sides of the first channel region,

wherein the second active pattern comprises:

a second channel region disposed below the second gate electrode; and

a plurality of second source/drain regions disposed at opposite sides of the second channel region, and

wherein the plurality of first source/drain regions are electrically connected to the first contact portion and have a first conductivity, and

the plurality of second source/drain regions are electrically connected to the second contact portion and have the first conductivity.

14. A method of manufacturing a semiconductor device, the method comprising:

designing a layout of the semiconductor device; and

using the layout to form patterns on a substrate,

wherein the designing the layout comprises:

placing a first standard cell and a second standard cell adjacent to each other in a first direction; and

substituting a connection pattern for a first contact pattern of contact patterns in the first standard cell and a second contact pattern of contact patterns in the second standard cell,

wherein the layout comprises a power pattern extending in a second direction at a boundary between the first and second standard cells, the second direction crossing the first direction,

wherein the first contact pattern extends to the power pattern from an active region of the first standard cell,

wherein the second contact pattern extends to the power pattern from an active region of the second standard cell,

wherein the patterns on a substrate includes a connection structure formed using the connection pattern, and gate electrodes formed using gate electrode patterns in the first and second standard cells,

wherein the connection structure is electrically isolated from the gate

electrodes, and

wherein the connection pattern runs across the power pattern and extends from the active region of the first standard cell to the active region of the second standard cell, and extends in a zigzag path across the power pattern.

15. The method of claim 14, wherein the designing the layout further comprises generating a via pattern on a zone where the connection pattern overlaps the power pattern.

16. The method of claim 14, wherein the designing the layout further comprises coloring the contact patterns in the first and second standard cells, and

wherein the first and second contact patterns are expressed with the same color and have a color conflict occurred between the first and second contact patterns.

17. The method of claim 16, wherein the first and second contact patterns are spaced apart at a distance less than a patterning resolution limit.