FIGs. 3a-3c illustrate a semiconductor wafer with a plurality of semiconductor die separated by saw streets;

FIGs. 4a-4k illustrate a process of forming a vertical interconnect structure for FO-WLCSP;

FIGs. 5a-5b illustrate the FO-WLCSP with vertical interconnect structure having conductive pillars;

FIG. 6 illustrates an alternate embodiment of the FO-WLCSP with vertical interconnect structure;

FIG. 7 illustrates the multi-layer UBM for the vertical interconnect structure of the FO-WLCSP;

FIG. 8 illustrates an alternate embodiment of the FO-WLCSP with vertical interconnect structure having conductive pillars and bumps;

FIGs. 9a-9~~b~~c illustrate the FO-WLCSP with vertical interconnect structure having RDL under the conductive pillars;

FIGs. 10a-10b illustrate another process of forming a vertical interconnect structure for 3-D FO-WLCSP;

FIG. 11 illustrates the FO-WLCSP with vertical interconnect structure having encapsulant over the semiconductor die;

FIG. 12 illustrates the FO-WLCSP with another vertical interconnect structure having encapsulant over the semiconductor die;

FIGs. 13a-13x illustrate another process of forming a vertical interconnect structure for 3-D FO-WLCSP;

FIGs. 14a-14d illustrate a process of mounting a bumped semiconductor device over a 3-D FO-WLCSP with vertical interconnect structure;

FIGs. 15a-15d illustrate another process of forming a vertical interconnect structure for a 3-D FO-WLCSP;

FIGs. 16a-16d illustrate another process of forming a

toward 3-D FO-WLCSP 378 such that bumps 376 extend into openings 350 and contact conductive bump material 370 within openings 350. The contact between bumps 376 and conductive bump material 370 results in an offset 380 between encapsulant 286 and a surface of semiconductor device 374. A footprint of semiconductor device 374 has an area that is larger than an area of a footprint of semiconductor die 276. Thus, the footprint of semiconductor die 276 is located within the footprint of semiconductor device 374 after the semiconductor device has been mounted to 3-D FO-WLCSP 378.

In FIG. 14c, the reconstituted wafer including semiconductor device 374 and 3-D FO-WLCSP 378 are heated to reflow bump material 370 and bumps 376. In one embodiment, bump material 370 and bumps 376 are reflowed by heating the materials above their melting points to form spherical balls or bumps ~~380~~382. In some applications, bumps ~~380~~382 are reflowed a second time to improve electrical contact to conductive layer 302. The bumps can also be compression bonded to conductive layer 302. Bumps ~~380~~382 represent one type of interconnect structure that can be formed over conductive layer 302. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect.

In FIG. 14d, the reconstituted wafer including semiconductor device 374 is singulated with saw blade or laser cutting device 384 into individual 3-D FO-PoPs 386. FO-PoPs 386 are singulated before back grinding tape 342 is removed. Alternatively, back grinding tape 342 is removed after completing the grinding of encapsulant 286 and after the formation and cleaning of openings 350 but before singulation. When back grinding tape 342 is removed before singulation of FO-PoPs 386, an optional dicing tape 387 is applied over bumps 326

Claims

What is claimed:

1. A method of making a semiconductor device, comprising:
providing a temporary carrier;
mounting a semiconductor die with an active surface oriented toward the temporary carrier;
depositing an encapsulant with a first surface over the temporary carrier and a second surface opposite the first surface, the second surface being over a backside of the semiconductor die;
removing the temporary carrier;
removing a portion of the encapsulant in a periphery of the semiconductor die to form an opening in the first surface of the encapsulant;
forming an interconnect structure over the active surface of the semiconductor die and extending into the opening;
forming a via from the second surface of the encapsulant to the opening; and
forming a first bump in the via that electrically connects to the interconnect structure.

2. The method of claim 1, further including depositing a temporary planarization and protection layer over the active surface of the semiconductor die.

3. The method of claim 1, wherein forming the interconnect structure includes:

depositing a first insulation layer over the active surface of the semiconductor die and over the first surface of the encapsulant;

depositing a conductive layer over the first insulation layer, the conductive layer being electrically connected to the first bump;

depositing a second insulation layer over the conductive layer; and

forming a second bump over the second insulation layer and electrically connected to the conductive layer.

4. The method of claim 1, further including forming a plurality of vias organized as an array with multiple rows wherein the plurality of vias extends from the second surface of the encapsulant to openings in the first surface of the encapsulant.

5. A method of making a semiconductor device, comprising:

providing a semiconductor die with an active surface;

depositing an encapsulant in a periphery of the semiconductor die with a first surface and a second surface opposite the first surface;

depositing a conductive material in the periphery of the semiconductor die extending from the first surface to the second surface of the encapsulant; and

forming an interconnect structure over the active surface of the semiconductor die and electrically connected to the conductive material.

6. The method of claim 5, wherein depositing the conductive material includes forming a copper pillar.

~~7. The method of claim 5, wherein the second surface of the encapsulant includes a step with a vertical offset.~~

~~8. The method of claim 5, further including depositing back grinding tape over the interconnect structure before depositing a conductive material in the periphery of the semiconductor die.~~

~~9~~1. A semiconductor device, comprising:

a semiconductor die~~ with an active surface~~;

an encapsulant deposited over~~in~~ a periphery of the semiconductor die including a stepped portion of the encapsulant extending across a surface of the semiconductor die ~~with a first surface and a second surface opposite the first surface~~;

an interconnect structure formed over ~~the active surface of~~ the semiconductor die opposite the stepped portion of the encapsulant; and

a ~~conductive~~ via formed in the encapsulant extending from a first surface of the encapsulant to the interconnect structure~~that extends from the second surface of the encapsulant to the interconnect structure~~.

~~10~~2. The semiconductor device of claim ~~9~~1, wherein the ~~conductive~~ via that extends from the ~~second~~ first surface of the encapsulant to the interconnect structure includes a sidewall with a vertical or tapered profile.

~~11~~3. The semiconductor device of claim ~~9~~1, further including a crack stop layer deposited over the ~~active surface of the~~ semiconductor die.

~~12~~4. The semiconductor device of claim ~~9~~1, further including a backside alignment unit ~~mounted~~ disposed in the periphery of the semiconductor die.

5. The semiconductor device of claim 1, further including a plurality of conductive vias that extend from the first surface of the encapsulant to a second surface of the encapsulant and organized as an array with multiple rows.

6. A semiconductor device, comprising:

a semiconductor die;

an insulating layer formed over a surface of the semiconductor die;

a preventative layer extending across the insulating layer over the semiconductor die to reduce formation of cracks with the insulating layer between the semiconductor die and the preventative layer; and

an interconnect structure formed over the semiconductor die.

7. The semiconductor device of claim 6, further including a conductive material disposed over a periphery of the semiconductor die.

8. The semiconductor device of claim 6, further including an encapsulant deposited over the semiconductor die wherein a surface of the encapsulant includes a step with a vertical offset.

9. The semiconductor device of claim 6, further including a temporary planarization and protection layer deposited over the surface of the semiconductor die.

10. The semiconductor device of claim 6, further including back grinding tape deposited over the interconnect structure.

11. A semiconductor device, comprising:

a semiconductor die;

an encapsulant disposed over the semiconductor die;

a bump disposed within a via of the encapsulant over a periphery of the semiconductor die;

a conductive pillar disposed over the bump; and

an interconnect structure formed over the semiconductor die.

12. The semiconductor device of claim 11, wherein the interconnect structure includes a solder bump.

13. The semiconductor device of claim 11, further including back grinding tape deposited over the interconnect structure.

14. A semiconductor device, comprising:

a semiconductor die;

a first conductive layer disposed over the semiconductor die including a first portion of the first conductive layer isolated from a second portion of the first conductive layer; and

an interconnect structure coupled to the first conductive layer and disposed between the first and second portions of the first conductive layer.

15. The semiconductor device of claim 14, wherein the interconnect structure includes a solder bump disposed over the first conductive layer.

16. The semiconductor device of claim 14, further including an encapsulant disposed around the semiconductor die.

17. The semiconductor device of claim 14, further including a temporary planarization and protection layer deposited over a surface of the semiconductor die.

18. The semiconductor device of claim 14, further including back grinding tape deposited over the interconnect structure.

19. The semiconductor device of claim 1, wherein the encapsulant has undergone a back grinding operation to reduce a thickness of the semiconductor device.

20. The semiconductor device of claim 1, wherein the semiconductor die includes a pre-applied adhesive disposed over the semiconductor die.