memory cell 105. Column decoder 130 may accept data, for example input 135, to be written to the memory cells 105. A ferroelectric memory cell 105 may be written by applying a voltage across the ferroelectric capacitor. This process is discussed in more detail below.

[025] In some memory architectures, accessing the memory cell 105 may degrade or destroy the stored logic state, and re-write or refresh operations may be performed to return the original logic state to memory cell 105. For example, the capacitor may be partially or completely discharged during a sense operation, corrupting the stored logic state. So the logic state may be re-written after a sense operation. Additionally, activating word lines 110 may result in the discharge of all memory cells in the row. Thus, several or all memory cells 105 in the row may need to be re-written.

[026] The memory controller 140 may control the operation (e.g., read, write, re-write, etc.) of memory cells 105 through the various components, such as row decoder 120, column decoder 130, and sense component 125. Memory controller 140 may generate row and column address signals in order to activate the desired word lines 110 and digit lines 115. Memory controller 140 may also generate and control various voltage potentials used during the operation of memory array 100. In general, the amplitude, shape, or duration of an applied voltage discussed herein may be adjusted or varied and may be different for the various operations for operating memory array 100. Furthermore, one, multiple, or all memory cells 105 within memory array 100 may be accessed simultaneously. For example, multiple or all cells of memory array 100 may be accessed simultaneously during a reset operation in which all memory cells 105, or a group of memory cells 105, are set to a single logic state.

[027] Figure 2A illustrates an example circuit 200 that includes a column of memory cells according to an embodiment of the present disclosure. Figure 2A illustrates an example circuit 200 that includes memory cells 105 in accordance with various embodiments of the present disclosure. Circuit 200 includes memory cells 105 MC(0)-MC(n), where “n” depends on the array size. The circuit 200 further includes word lines WL-CT(0)-WL-CT(n) and WL-CB(0)-WL-CB(n), digit lines BL-CT and BL-CB, and sense component 125. The word lines, digit lines, and sense component may be examples of word lines 110, digit lines 115, and sense component 125, respectively, as described with reference to Figure 1. While one column of

a row decoder coupled to the plurality of pairs of word lines and configured to activate a pair of word lines based on a row address;

a column decoder coupled to the plurality of pairs of digit lines and configured to activate a pair of digit lines based on a column address; and

sense components coupled to the plurality of pairs of digit lines and configured to determine the stored states of the memory cells of an activated row of memory cells.

14. The apparatus of claim 13 wherein each of the plurality of pairs of digit lines includes a first digit line coupled to the first selection components of the memory cells of the respective column of memory cells and further includes a second digit line coupled to the second selection components of the memory cells of the respective column of memory cells.

15. The apparatus of claim 14 wherein the sense components comprises a respective sense component coupled to each of the pairs of digit lines of the plurality of pairs of digit lines.

16. The apparatus of claim 15 wherein each sense component is configured to drive the second digit line of the pair of digit lines to which the sense component is coupled to a voltage and the sense component is further configured to drive the first digit line of the pair of digit lines to which the sense component is coupled to a voltage complementary to the voltage of the second digit line.

17. The apparatus of claim 14 wherein each pair of word lines of the plurality includes a first word line coupled to gates of the first selection components of the respective row of memory cells and further includes a second word line coupled to gates of the second selection components of the respective row of memory cells, wherein the first selection components of the respective row of memory cells are activated by the first word line and the second selection components of the respective row of memory cells are activated by the second word line.

wherein the opposite complementary voltage levels are coupled to the first and second plates to change the polarization of the ferroelectric memory cell.

27. The method of claim 25, further comprising decoupling the second sense node from the second digit line prior to comparing the voltage at the second sense node of the sense amplifier to the voltage of the first sense node.

28. The method of claim 27, further comprising coupling the second sense node to the second digit line after driving the first and second sense nodes to complementary voltage levels based on the comparison.

29. The method of claim 25 wherein coupling the first sense node to the first digit line to provide the complementary voltage levels to the first and second plates of the ferroelectric memory cell over the first and second digit lines, respectively, and isolating the first and second plates from the first and second digit lines, respectively, restores data on the ferroelectric memory cell.

30. The method of claim 25, further comprising driving the first and second sense nodes to a same voltage prior to isolating the first and second plates from the first and second digit lines.

31. The method of claim 25 wherein the complementary voltage levels comprise a supply voltage and ground.