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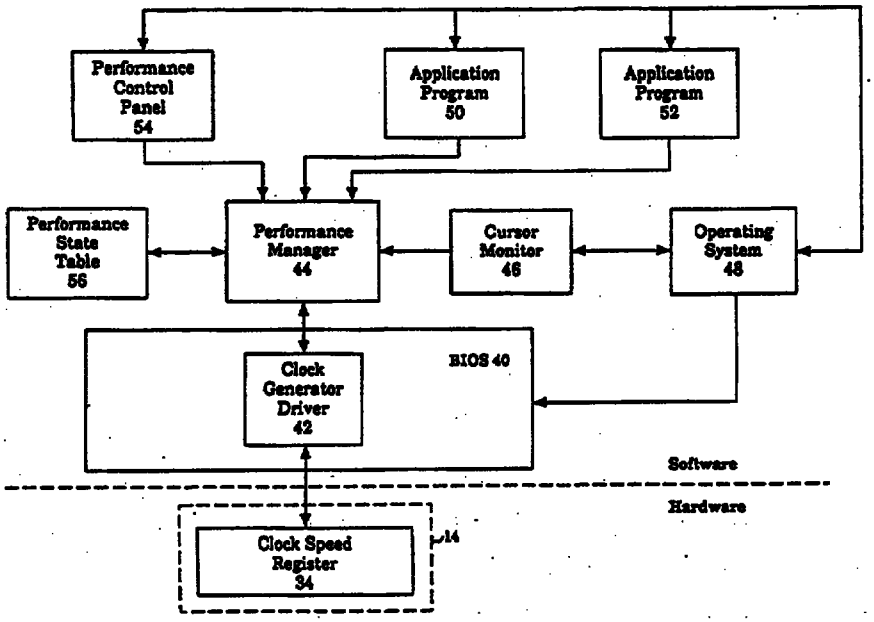
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(54) Title: DYNAMIC PROCESSOR PERFORMANCE AND POWER MANAGEMENT IN A COMPUTER SYSTEM



(57) Abstract

A computer system (10) is disclosed comprising a clock generator circuit (14) having a clock speed register (34) and circuitry for generating a processor clock signal (32) at a frequency determined by the clock speed register (34), wherein the processor (12) executes a performance manager program (44) that writes the clock speed register (34) according to a performance state selected by an application program (50, 52). The application program (50, 52) selects the performance state to maximize performance during processor intensive functions and to maximize power conservation during interactive functions.