

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
11 March 2004 (11.03.2004)

PCT

(10) International Publication Number
WO 2004/021359 A3

(51) International Patent Classification⁷: **G11C 11/406**,
16/34

(21) International Application Number:
PCT/US2003/027056

(22) International Filing Date: 28 August 2003 (28.08.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/234,001 29 August 2002 (29.08.2002) US

(71) Applicant: **MICRON TECHNOLOGY, INC.** [US/US];
8000 South Federal Way, Boise, ID 83707-0006 (US).

(72) Inventor: **GILTON, Terry, L.**; 3149 E. Nature Drive,
Boise, ID 83706 (US).

(74) Agent: **D'AMICO, Thomas, J.**; Dickstein Shapiro Morin
& Oshinsky LLP, 2101 L Street NW, Washington, DC
20037-1526 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,
CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,
GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW,
MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC,
SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA,
UG, UZ, VC, VN, YU, ZA, ZM, ZW.

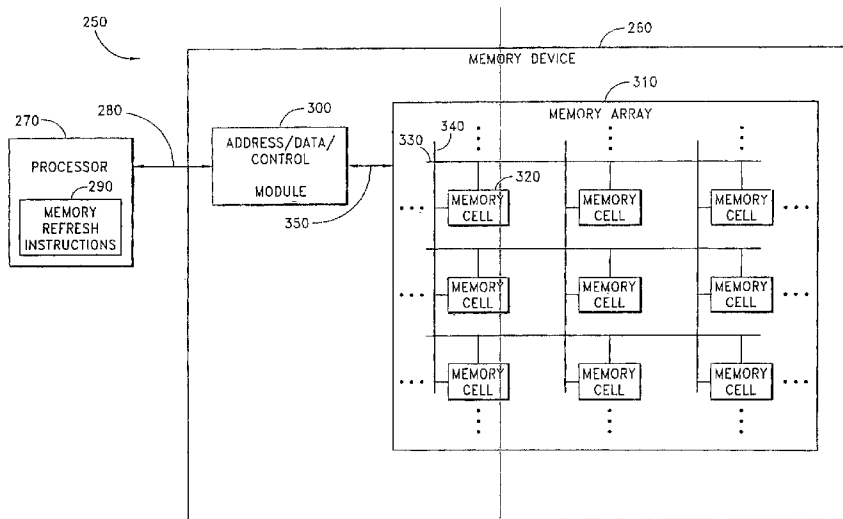
(84) Designated States (*regional*): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),
Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,
ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO,
SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM,
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— with international search report

(88) Date of publication of the international search report:
24 February 2005

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SOFTWARE REFRESHED MEMORY DEVICE AND METHOD



(57) **Abstract:** A software refreshed memory device comprises a plurality of memory cells that must be periodically refreshed to avoid losing data. Preferably, the memory cells can avoid losing data even though the time interval between successive memory refresh operations is relatively long, as compared to the time interval between successive memory refresh operations *in a* conventional volatile memory device, such as a DRAM. A processor can perform periodic memory refresh operations by executing a set of memory refresh instructions implemented in software, rather than in hardware. Accordingly, the memory device can advantageously be simplified, because the need for memory refresh circuitry and for a unique refresh control signal are advantageously eliminated. Moreover, the processor executing the memory refresh instructions can typically perform more sophisticated algorithms, as compared to memory refresh circuitry implemented in hardware, for determining when to perform a memory refresh operation. For example, the processor can determine whether each individual memory cell needs to be refreshed, thereby *advantageously avoiding* performing unnecessary refresh operations on memory cells that do not need to be refreshed.

WO 2004/021359 A3