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FORMING SOLDER BUMPS ON SEMICONDUCTOR CHIPS

TECHNICAL FIELD

This invention relates to a method for forming solder bumps on pad terminals of a semi-conductor die, such as for example, an integrated circuit (IC) chip.

BACKGROUND

IC chips are typically manufactured by forming the active devices for many chips on a single wafer of semiconductor material. The wafer is metallised to form the required interconnections among the active devices and then diced into individual chips. The chips are then mounted on a substrate such as, for example, a printed circuit board, and encapsulated to form a single chip or multichip module. One known method of mounting a chip on a substrate uses solder beads or "bumps" to electrically and mechanically interconnect terminal pads formed on one surface of the chip to terminal pads formed on the substrate. IC chips which are fabricated for such mounting are known as flip chips.

Solder bumps are commonly formed directly on the terminal pads of a flip chip. An example of such direct formation is disclosed in US Patent No. 5672542 to Schwiebert et al. This patent discloses applying a mask to the flip chip and forming apertures in the mask which are aligned with the terminal pads of the flip chip. A solder paste is stencilled onto the mask to fill the apertures and then heated to cause it to coalesce and form solder bumps on the terminal pads of the flip chip. The mask is then removed.

Alternatively, solder bumps may be initially formed on a separate substrate. Thus US Patent No. 5381946 to Koopman et al discloses forming solder bumps on terminal pads of a temporary substrate and then transferring the solder bumps to the terminal pads of a flip chip. According to this patent a sacrificial metal layer is formed on the terminal pads of the temporary

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substrate, which terminal pads are formed of a material which is non-wettable by the solder, and solder bumps are then formed on the sacrificial metal layer. The solder bumps may be formed by solder plating and subsequently heating the substrate to a first temperature wherein the solder liquefies to form the bumps whilst the sacrificial metal layer remains substantially intact. An unbumped flip chip with solder wettable pads is then placed on the solder bumps on the temporary substrate and the solder is reflowed at a second, higher temperature such that the solder dissolves the sacrificial metal layer and adheres to the flip chip pads. In addition to the terminal pads of the temporary substrate being formed of a material which is not wettable by the solder, the sacrificial metal layer must be a metal which is wettable by the solder, and dissolvable therein, whilst also being adherable to the terminal pads of the temporary substrate. This disclosed invention provides for "burn-in" and testing of chips via the temporary substrate with the chip mounted thereon prior to the second, higher temperature heating step to reflow the solder and transfer the bumps to the chip.

US Patent No. 5607099 to Shing Yeh et al also discloses forming solder bumps on a carrier substrate and then transferring them to a flip chip. This patent discloses forming cavities in a carrier substrate, for example of silicon which is masked and etched to form the cavities, filling the cavities with a solder paste, heating the carrier substrate for the paste to form into solder balls within the cavities, aligning the carrier substrate and a flip chip, heating the carrier substrate to liquefy the solder balls and bringing the flip chip into contact with the carrier substrate such that the solder balls wet and transfer to the terminal pads on the flip chip to form bumps thereon.

The formation of IC chips and their packaging into modules involves many processes which require considerable attention to detail and precision to create and maintain a high yield of functioning chips. Production time and cost is also of considerable importance and any process steps which save time and cost without sacrificing quality are highly significant for manufacturers.

SUMMARY OF THE INVENTION

The present invention provides a method for forming solder bumps on a semiconductor chip which is similar to the above mentioned Koopman et al and Shing Yeh et al prior art United States patents in that it utilises another substrate or carrier, but which is an improvement over that prior art in that the method involves less process steps. This allows for savings in production time and cost. Other advantages of the invention will become evident from the following description.

According to the invention, a method for forming solder bumps on a semiconductor chip is provided, wherein the chip includes metallised solder wettable terminal pads on one surface, the method comprising -

(i) providing a carrier substrate having a number of wells on or in a surface thereof, wherein the wells are non-wettable by the solder and are arranged in a pattern which corresponds with the metallised terminal pads of the chip,

(ii) filling the wells with a solder paste,

(iii) moving the chip and the carrier substrate relatively together to bring the terminal pads of the chip into contact with the solder paste in the wells of the carrier substrate,

(iv) heating the solder paste sufficiently for it to form solder and flow from the non-wettable wells to the wettable terminal pads and form bumps thereon, and

(v) relatively removing the chip from the carrier substrate.

It will be appreciated that in the above identified prior art of Koopman et al and Shing Yeh et al, the solder bumps are initially formed on the temporary

substrate or carrier and are then transferred to the flip chip, whereas according to the present invention the solder bumps are both formed and transferred in the one step.

The wells may be formed on a surface of a carrier substrate by laminating a layer of photoimageable film on that surface, then exposing and developing it such that the removed areas provide the wells. Alternatively a thin layer of photoimageable resist may be coated on the surface, exposed and developed to define the well locations and the carrier substrate then etched to form the wells therein. In both methods, the carrier substrate is preferably silicon whereby the wells will be non-wettable by the solder. However the invention encompasses the provision of a carrier substrate of another material and applying a treatment thereto as may be necessary to render the wells non-wettable by the solder.

A desired bump geometry or volume can be provided by appropriately sizing the wells. Thus a thickness for a dry film laminate, or depth for etched wells, can be determined from a desired bump volume and given terminal pads area. Also different bump geometries on a single chip can be provided by appropriately varying the dimensions of individual wells. Different bump geometries on a single chip may be required, for example, where some solder bumps are provided for spacing a chip from a substrate while others form the terminal interconnections.

Preferably the carrier substrate is of a size such that a plurality of chips can be simultaneously solder bumped according to the method of the invention. Thus the carrier substrate may be, for example, of wafer scale and have a repeating pattern of the wells over its surface so it can be fully loaded with chips which are simultaneously bumped by the method.

Preferably the carrier substrate is re-usable. Thus, as will be appreciated, the bumping of a number of chips in parallel using a recycled

carrier substrate admits of further cost savings. For example, the lithographic procedures are much reduced compared to conventional methods of bumping directly onto the pads of a chip given such a procedure need only be performed once per carrier substrate to define a pattern for the wells.

The method of the invention is primarily based on manipulating single chips, thus wafers are diced before the bumping method is applied and this eliminates the need, in bumping, to handle wafers of different diameters and thicknesses. Thus the invention allows for bumping at the wafer scale to be avoided whereat both good and bad chips will be simultaneously bumped, which is wasteful of resources and is potentially of high cost per bumped good chip in poor yield wafers. However an underbump metallisation (UBM) process may be performed on a wafer prior to its dicing into chips, for example by using a maskless electroless Nickel plating process, as different wafer sizes and thicknesses can be easily accommodated for this step without capital investment. It is to be understood, however, that the method of the invention is not limited to the solder bumping of individualised chips and may be applied to chips at a wafer scale prior to dicing the wafer.

Preferably the wells are filled with the solder paste by stencilling the paste into the wells. This involves placing a quantity of solder paste on the surface and spreading it using a squeegee such that each well is filled and excess paste is scraped off the surface. This is a known step and is thus not described in any further detail herein.

The composition of the solder paste may be selected according to requirements, and thus varied to suit particular applications. For example, if the wells are defined on the surface of the carrier substrate by a dry film mask which is laminated thereon, the solder will generally have to be a low temperature type.

For a better understanding of the invention and to show how it may be carried into effect, embodiments thereof will be described by way of non-limiting example only with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1(a)-(i) illustrate steps in a method according to one embodiment of the invention.

Figs. 2A and 2B are bottom and side views respectively of a flip chip showing its terminal pads.

Fig. 3 illustrates a carrier substrate.

Figs. 4 to 11 show stages in a method according to another embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Integrated circuit chips are typically manufactured by forming the active devices for many chips on a single wafer 12 (Fig. 1(a)) of semiconductor material. The wafer 12 is then diced to provide individual chips 14 (Fig. 1(b)). For a flip chip, terminal pads 18 for the circuitry of the chip are formed on a surface 16 (see Fig. 2A) and typically at the wafer scale. The terminal pads 18 may be of Aluminium and in order to enhance the formation of solder bumps on them they are typically coated with one or more layers 20 (see Fig. 2B) of suitable metals. This coating 20, known as under-bump metallisation or under-bump metallurgy (UBM), may be applied at the chip scale (see Fig. 1(c)), or the wafer scale. A suitable UBM for an Aluminium pad is Nickel. Examples of suitable underbump metals for solder adhesion are (a) for wafer scale processing: Ti-Ni-Au; Cr-CrCu-Cu-Au; Al-Ni-Cu; electroless Ni/Au; and (b) for chip scale processing: electroless Ni/Au. Figs. 1(a)-(c) illustrate the provision of an IC chip 14 having solder wettable metallised terminal pads 18-20 from a wafer 12.

The method requires the provision of a carrier substrate 22 (Fig. 1(d)) which may be a dummy silicon wafer which is baked at 125°C for 15 minutes. Other suitable materials may be used for the carrier substrate 22, provided such materials are not wettable by the solder. One other such material is glass. A layer of photoimageable dry film 24 is then applied to a surface of carrier substrate 22 (Fig. 1(d)). An example photoimageable dry film is: SUNFORT YQ - 50 PT dry film (made by Ashahi - Japan). This dry film is available in 50 micrometers thick sheet form and is laminated on to the carrier substrate by sending the dry film/carrier substrate in between two hot rolls at controlled temperature/pressure and travel speed. Layer 24 is preferably at least 1 mil (254 micrometers) thick. Film layer 24 is then exposed and developed to define wells 26 (Fig. 1(e)) at selected locations with which the terminal pads 18-20 of a chip 14 will register. The thickness of the laminate layer 24 and cross-sectional area of the wells 26 are determined according to a desired bump geometry. The carrier substrate 22 with layer 24 is then cured for 10 minutes at 60°C.

A solder paste 28 is then applied directly onto the surface of layer 24 and squeegeed thereover to completely fill the wells 26 (Fig. 1(f)). The carrier substrate 22 is then inspected to ensure the solder paste 28 uniformly fills the wells 26. If it doesn't, the substrate 22 is re-printed with further solder paste 28. A thin layer of liquid flux may be sprayed over the surface of film 24. Typically, the solder paste 28 contains metal powder in a flux vehicle. Generally, solder pastes that can be used are those with melting temperatures less than 200° Celsius. Examples are 63Pb/37Sn (183°C), 52 In/48Sn (118°C), 58 Bi/42Sn (138°C).

A plurality of the chips 14 are then placed on the carrier substrate 22 with the UBM 20 of each terminal pad 18 aligned with respective solder paste filled wells 26-28 (Fig. 1(g)). Preferably, to ensure there is good registration

between the terminal pads 18-20 and the solder paste 28 in wells 26, the pads 18-20 are smaller in area than the cross-sectional area of the wells 26.

The assembly of carrier substrate 22 and chips 14 is heated according to a predetermined temperature - time profile for the solder paste 28 to form solder and coalesce into solder bumps 30 on the terminal pads 18-20. During this solder reflow step, the solder adheres to the wettable terminal pads 18-20 and withdraws completely from the non-wettable wells 26 (Fig. 1(h)). The solder bumped chips 14 are then removed from the carrier substrate 22 (Fig. 1(i)) for example on a waffle pack or chip carrier (not shown). The carrier substrate 22 with layer 24 is available for re-use in the method, thus it may be recycled for the next batch of chips 14 to be bumped as indicated by arrow 32.

Although dry film laminate material is preferably used with the invention, it can be substituted with pre-drilled/electroformed stainless steel/Nickel foils of required thickness and design. The foils can be attached to any substrate using appropriate bonding techniques. Thereafter, the solder paste is printed directly on the substrate foil, the flip chips aligned on the substrate solder fills then the solder is reflowed to form solder bumps on the flip chip in a single reflow cycle.

As shown by Fig. 3, the substrates 22 can be provided with fine through holes 27 corresponding to each thin film aperture or well 26 before the laminating/bonding process step. This additional step provides easier removal of flip chips from the substrate carrier 22 after the reflow cycle.

Figs. 4-11 illustrate stages in a method wherein a surface 41 of a silicon carrier substrate 40 is coated with a photoimageable resist 42, which is then exposed and developed to define well locations 44 (Fig. 5). The carrier substrate 40 is then etched to form wells 46 in the substrate (Figs. 6 and 7). Preferably the etching is such as to form wells 46 of at least 1 mil (25 micrometres) depth. The wells 46 are then filled with a solder paste 48 (Fig. 8),

a chip 50 having UBM terminal pads 52 is placed onto substrate 40 such that pads 52 register with the solder paste 48 in wells 46 (Fig. 9), the assembly is heated to reflow the solder 48 and form bumps 54 on terminals 52 (Fig. 10), followed by removal of the solder bumped chip 50. The steps represented by Figs. 4 to 11 are generally a repeat of the steps represented by Figs. 1(f) to (i) and the description hereinabove relating to Figs. 1(f)-(i) applies also for Figs. 8-11. The carrier substrate 40 may also be recycled for bumping a subsequent batch of chips 50.

A photoimageable solder resist that can be used for silicon substrate etching is: SU8 - Supplier Proprietary resist. Alternatively, Nitride thin film can be used for etching silicon for defining wells on the nitride deposit. Nitride is deposited on the silicon wafer, Shipley/AZ photoresist is spin coated on the nitride deposited wafer, then exposed and developed for the required wells. Nitride etch to expose silicon, resist strip and silicon etch at the wells are the steps involved in this alternative process.

Either of the methods as represented by Figs. 1(a)-(i) or Figs. 4-11 may be used for bumping chips with either peripheral or array type terminal pad configurations. The invention is also suitable for bumping chips with a fine pitch and fine geometry. For example bumping of 5 mil pitch (125 micrometres) is possible. Individual Gallium Arsenide (Ga As) dies may also be solder bumped according to method of the invention.

The invention described herein is susceptible to variations, modifications and/or additions other than those specifically described and it is to be understood that the invention includes all such variations, modifications and/or additions which fall within the scope of the following claims.

CLAIMS:

1. A method for forming solder bumps on a semiconductor chip, wherein the chip includes metallised solder wettable terminal pads on one surface, the method comprising -

(i) providing a carrier substrate having a number of wells on or in a surface thereof, wherein the wells are non-wettable by the solder and are arranged in a pattern which corresponds with the metallised terminal pads of the chip,

(ii) filling the wells with a solder paste,

(iii) moving the chip and the carrier substrate relatively together to bring the terminal pads of the chip into contact with the solder paste in the wells of the carrier substrate,

(iv) heating the solder paste sufficiently for it to form solder and flow from the non-wettable wells to the wettable terminal pads and form bumps thereon, and

(v) relatively removing the chip from the carrier substrate.

2. A method as claimed in claim 1 wherein a photoimageable film is laminated on said surface of the carrier substrate, then exposed and developed to thereby define wells on said surface.

3. A method as claimed in claim 1 wherein a foil which is preformed with holes is bonded on said surface of the substrate, the holes defining said wells on said surface.

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4. A method as claimed in claim 2 wherein the photoimageable film and the carrier substrate are formed of substances which are non-wettable by the solder.

5. A method as claimed in claim 4 wherein the carrier substrate is formed of silicon.

6. A method as claimed in claim 1 wherein the carrier substrate is glass.

7. A method as claimed in claim 1 wherein a photoimageable resist is coated on said surface, then exposed and developed to define locations for the wells, the substrate then being etched to form said wells in said surface.

8. A method as claimed in claim 7 wherein the carrier substrate is made of a substance which is non-wettable by the solder.

9. A method as claimed in claim 8 wherein the carrier substrate is formed of silicon.

10. A method as claimed in any one of claim 1 wherein the wells are filled with the solder paste by applying the solder paste to the carrier substrate by stencilling using a squeegee.

11. A method as claimed in claim 1 wherein each well has a cross-sectional area which is larger than the area of a corresponding metallised solder wettable terminal pad of the chip such that the whole area of each terminal pad contacts the solder paste in a well.

12. A method as claimed in claim 1 wherein the metallised solder wettable pads are formed of Aluminium on which a layer of Nickel is deposited.

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