CLAIMS

1. A chip, comprising a die and a package substrate, wherein the die is disposed on the package substrate, and a plurality of pinmap patterns are disposed in a pin region of the package substrate;

in the plurality of pinmap patterns, at least two pinmap patterns are basic patterns comprising six signal pins;

a first pin, a second pin, a third pin, and a fourth pin in the six signal pins are sequentially spaced apart in a first direction, a fifth pin and a sixth pin in the six signal pins are spaced apart in a second direction, and the fifth pin and the sixth pin are respectively located on two sides of a connection line between the second pin and the third pin; and

the first pin, the fourth pin, the fifth pin, and the sixth pin are data signal pins, the second pin and the third pin are control signal pins, and the first direction is different from the second direction.

2. The chip according to claim 1, wherein the fifth pin and the sixth pin are disposed on a perpendicular line of the connection line between the second pin and the third pin, and the first direction is perpendicular to the second direction.

3. The chip according to claim 2, wherein the fifth pin and the sixth pin are disposed on a midperpendicular line of the connection line between the second pin and the third pin.

4. The chip according to any one of claims 1 to 3, wherein the basic pattern is of a centrosymmetric structure or an axisymmetric structure.

5. The chip according to any one of claims 1 to 4, wherein pins in the pin region are arranged in an array, and pins in rows and columns are staggered.

6. The chip according to any one of claims 1 to 5, wherein the pins in the pin region are arranged in a triangular grid shape, and connection lines between the pin and two adjacent pins of the pin constitute an equilateral triangle.

7. The chip according to any one of claims 1 to 6, wherein the basic pattern further comprises a ground pin, and the ground pin is arranged at a periphery of the six signal pins.

8. The chip according to claim 7, wherein there are 14 ground pins in the basic pattern, and the 14 ground pins are sequentially spaced apart at the periphery of the six signal pins; in the first direction, a first ground pin is located on a side of the first pin, an eighth ground pin is located on a side of the fourth pin, and a second ground pin, a third ground pin, a fourth ground pin, a fifth ground pin, a sixth ground pin, and a seventh ground pin are sequentially arranged between the first ground pin and the eighth ground pin; and a ninth ground pin, a tenth ground pin, an eleventh ground pin, a twelfth ground pin, a thirteenth ground pin, and a fourteenth ground pin are sequentially arranged between the eighth ground pin and the first ground pin.

9. The chip according to claim 8, wherein two basic patterns are adjacently disposed, one is a first basic pattern, the other is a second basic pattern, and adjacent sides of the first basic pattern and the second basic pattern share a ground pin.

10. The chip according to claim 9, wherein the first basic pattern and the second basic pattern are translated patterns of each other, and an eighth ground pin of the first basic pattern and a first ground pin of the second basic pattern are a shared ground pin.

11. The chip according to claim 9, wherein the first basic pattern and the second basic pattern are translated patterns of each other, a twelfth ground pin of the first basic pattern and a fourth ground pin of the second basic pattern are a shared ground pin, and an eleventh ground pin of the first basic pattern and a fifth ground pin of the second basic pattern are a shared ground pin.

12. The chip according to claim 9, wherein the first basic pattern and the second basic pattern are translated patterns of each other, a seventh ground pin of the first basic pattern and a first ground pin of the second basic pattern are a shared ground pin, and an eighth ground pin of the first basic pattern and a fourteenth ground pin of the second basic pattern are a shared ground pin.

13. The chip according to claim 9, wherein the first basic pattern and the second basic pattern are translated patterns of each other, a twelfth ground pin of the first basic pattern and a second ground pin of the second basic pattern are a shared ground pin, an eleventh ground pin of the first basic pattern and a third ground pin of the second basic pattern are a shared ground pin, a tenth ground pin of the first basic pattern and a fourth ground pin of the second basic pattern are a shared ground pin, and a ninth ground pin of the first basic pattern and a fifth ground pin of the second basic pattern are a shared ground pin.

14. The chip according to claim 9, wherein the first basic pattern and the second basic pattern are translated patterns of each other, an eleventh ground pin of the first basic pattern and a first ground pin of the second basic pattern are a shared ground pin, a tenth ground pin of the first basic pattern and a second ground pin of the second basic pattern are a shared ground pin, a ninth ground pin of the first basic pattern and a third ground pin of the second basic pattern are a shared ground pin, and an eighth ground pin of the first basic pattern and a fourth ground pin of the second basic pattern are a shared ground pin.

15. The chip according to claim 9, wherein the first basic pattern and the second basic pattern are translated and rotated patterns of each other, a fifth ground pin of the first basic pattern and a fifth ground pin of the second basic pattern are a shared ground pin, a sixth ground pin of the first basic pattern and a fourth ground pin of the second basic pattern are a shared ground pin, a seventh ground pin of the first basic pattern and a third ground pin of the second basic pattern are a shared ground pin, and an eighth ground pin of the first basic pattern and a second ground pin of the second basic pattern are a shared ground pin.

16. The chip according to any one of claims 8 to 15, wherein in the basic pattern, connection lines between the data signal pin adjacent to two adjacent ground pins and the two adjacent ground pins constitute an equilateral triangle.

17. The chip according to any one of claims 1 to 16, wherein the first pin, the fourth pin, the fifth pin, and the sixth pin are single-ended signal pins, and the second pin and the third pin are a pair of differential signal pins.

18. The chip according to any one of claims 1 to 17, wherein the chip is a central processing unit, the central processing unit is configured with a plurality of memory channels, the memory channel comprises a plurality of bytes, the byte corresponds to two basic patterns, and the data signal pin in the basic pattern is for transmitting a data signal of the corresponding byte.

19. An electronic device, comprising a housing and a circuit board disposed in the housing, wherein a chip is disposed on the circuit board, the chip is the chip according to any one of claims 1 to 18, and a signal pin of the chip is electrically connected to the circuit board.

20. A signal transmission method, wherein the signal transmission method is applied to a chip, the chip comprises a package substrate, a plurality of pinmap patterns are disposed in a pin region of the package substrate; in the plurality of pinmap patterns, at least two pinmap patterns are basic patterns comprising six signal pins; a first pin, a second pin, a third pin, and a fourth pin in the six signal pins are sequentially spaced apart in a first direction, a fifth pin and a sixth pin in the six signal pins are spaced apart in a second direction, and the fifth pin and the sixth pin are respectively located on two sides of a connection line between the second pin and the third pin; the first pin, the fourth pin, the fifth pin, and the sixth pin are data signal pins, the second pin and the third pin are control signal pins, the first direction is different from the second direction; and the method comprises:

transmitting a data signal through the first pin, the fourth pin, the fifth pin, and the sixth pin, and transmitting a control signal through the second pin and the third pin.