SIGNAL RECEIVING APPARATUS AND METHOD, ANALOG-TO-DIGITAL MIXED TEST BOARD, AND TESTER

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to Chinese Patent Application No. 202411457683.3, filed on October 18, 2024, and titled "SIGNAL RECEIVING APPARATUS AND METHOD, ANALOG-TO-DIGITAL MIXED TEST BOARD, AND TESTER". The content of the above identified application is hereby incorporated herein in its entirety by reference.

TECHNICAL FIELD

[0002] The present application relates to the field of semiconductor test technologies, and in particular, to a signal receiving apparatus and method, an analog-to-digital mixed test board, and a tester.

BACKGROUND

[0003] A semiconductor automation test refers to detecting each parameter indicator of a Device Under Test (DUT) by an Automatic Test Equipment (ATE), and removing a defective product to control delivery quality of a semiconductor device. In an analog test, especially in a high-speed analog test, a test signal delivered to the DUT is usually highly required in terms of a harmonic, a signal-to-noise ratio, an amplitude, and a signal frequency. When implementing an IQ (in-phase and quadrature) function, a tester needs to ensure IQ channel synchronization.

[0004] A conventional test signal receiving scheme adjusts a sampling clock phase of a ADC

(analog-to-digital converter) of IQ channels by changing a frequency of a clock signal output from a clock circuit, so as to synchronize the IQ channels. The test signal is received by adjusting the sampling clock phase of the ADC, which has a complex control logic, a cumbersome operation, and low test efficiency.

[0005] For the issue of the complex control logic, the cumbersome operation, and the low test efficiency for outputting the test signal, no effective solution has been proposed.

SUMMARY

[0006] According to various embodiments of the present application, a signal receiving apparatus and method, an analog-to-digital mixed test board, and a tester are provided.

[0007] In a first aspect of the present application, the signal receiving apparatus is provided, including a main test unit and a sub-test unit. The sub-test unit includes a waveform digitizer, a first communicating module, and an external clock chip. The external clock chip is configured to output a sampling clock to an analog-to-digital converter, and the sampling clock has a fixed frequency. The waveform digitizer is connected to the analog-to-digital converter and the first communicating module, respectively, and the waveform digitizer is configured to receive an original waveform at the fixed frequency output by the analog-to-digital converter according to the sampling clock, perform resampling on the original waveform, generate a reconstructed waveform at any required frequency, and send the reconstructed waveform to the first communicating module. The main test unit further includes a second communicating module, a waveform receiving module, and a storage module. The second communicating module is connected to the first communicating module

and the waveform receiving module, respectively, the second communicating module is configured to receive the reconstructed waveform and send the reconstructed waveform to the waveform receiving module, and the waveform receiving module is connected to the storage module and configured to store the received reconstructed waveform into the storage module.

[0008] In an embodiment, the waveform digitizer further includes a synchronization control module and a waveform data processing module. The synchronization control module is connected to the waveform data processing module and the analog-to-digital converter, respectively, and configured to receive the original waveform at the fixed frequency output by the analog-to-digital converter, and send the original waveform to the waveform data processing module after receiving a trigger signal. The waveform data processing module is connected to the first communicating module and configured to perform resampling on the original waveform, generate the reconstructed waveform at any required frequency, and send the reconstructed waveform to the first communicating module.

[0009] In an embodiment, the synchronization control module further includes a synchronous receiving control module and an acquired signal processing module. The synchronous receiving control module is connected to the acquired signal processing module and two or more analog-to-digital converters, and configured to receive original waveforms output by the two or more analog-to-digital converters, and synchronously send the original waveforms to the acquired signal processing module after receiving a trigger signal. The acquired signal processing module is connected to the waveform data processing module, and configured to synthesize the received original waveforms and output a synthesized original waveform to the

waveform data processing module.

[0010] In an embodiment, the waveform data processing module further includes a calibrating module and a digital resampling module. The calibrating module is connected to the synchronization control module, and configured to perform calibration on the received original waveform and output calibrated waveform data. The digital resampling module is connected to the calibrating module and the first communicating module, respectively, and configured to perform resampling on the calibrated waveform data, generate the reconstructed waveform at any required frequency, and send the reconstructed waveform to the first communicating module.

[0011] In an embodiment, the calibrating module further includes at least one of a Direct Current (DC) calibrating module, an Alternating Current (AC) amplitude calibrating module, or a low-pass filtering module.

[0012] In an embodiment, the digital resampling module further includes an input waveform data cache module, a valid location calculating module, a valid coefficient generating module, a valid data cache module, and a data calculating module. The input waveform data cache module is connected to the calibrating module, the valid location calculating module, and the valid data cache module, respectively, the input waveform data cache module is configured to cache the calibrated waveform data, send a start signal to the valid location calculating module when the quantity of cached data is greater than a specified threshold, read valid data corresponding to a valid location from the cached data according to a received read enable signal, and send the read valid data to the valid data cache module for caching. The valid

location calculating module is connected to the valid coefficient generating module, and configured to obtain valid location information by calculation according to a set step and an initial phase after receiving the start signal, send the valid location information to the valid coefficient generating module, and send the read enable signal to the input waveform data cache module. The valid coefficient generating module is connected to the data calculation module and a valid data cache module, respectively, and configured to read a coefficient from a plurality of groups of pre-stored coefficients according to the valid location information, to obtain a valid coefficient and send the valid coefficient to the data calculating module, and send a data-read enable signal to the valid data cache module. The valid data cache module is connected to the data calculating module, and configured to read cached valid data according to the received data-read enable signal and send the cached valid data to the data calculating module. The data calculating module is connected to the first communicating module, and configured to perform convolution calculation according to the received valid coefficient and the received valid data to obtain the reconstructed waveform and send the reconstructed waveform to the first communicating module.

[0013] In an embodiment, the valid data cache module is configured to store the valid data in a shift manner in parallel into continuous internal cache units, and/or the valid coefficient generating module is configured to read two adjacent groups of coefficients according to integer location information of the valid location information, and perform calculation, according to decimal location information of the valid location information, on the two adjacent groups of coefficients by a linear interpolation algorithm, to obtain the valid

coefficient.

[0014] In an embodiment, the data calculating module is configured to perform the convolution calculation according to the received valid coefficient and the received valid data in a following formula:

$$\mathrm{DATA_VALID} = \sum_{k=0}^{15} \mathrm{COE}[k] * \mathrm{DATA_IN}[16 - k]$$

DATA_VALID represents a reconstructing point of the reconstructed waveform, COE represents a valid coefficient corresponding to a valid location of the reconstructing point, and DATA_IN represents valid data corresponding to the valid location.

[0015] In an embodiment, the waveform receiving module further includes a receiving control module and a read-write control module. The receiving control module is connected to the second communicating module and the read-write control module, respectively, and configured to receive the reconstructed waveform by the second communicating module and send a write request instruction to the read-write control module. The read-write control module is connected to the storage module, and configured to store the reconstructed waveform into the storage module according to the write request instruction.

[0016] In an embodiment, the sub-test unit further includes a first service decoding module, the first service decoding module is connected to a host, the waveform digitizer, and the external clock chip, respectively, and the first service decoding module is configured to perform parameter configuration on the waveform digitizer and the external clock chip according to an instruction delivered by the host, and/or the main test unit further includes a

second service decoding module, the second service decoding module is connected to the host and the waveform receiving module, respectively, and the second service decoding module is configured to perform parameter configuration on the waveform receiving module according to an instruction delivered by the host and perform waveform reading operation on the storage module by the waveform receiving module.

[0017] In a second aspect of the present application, a signal receiving method is provided, including: an external clock chip in a sub-test unit outputting a sampling clock to an analog-to-digital converter, and the sampling clock having a fixed frequency; a waveform digitizer in the sub-test unit receiving an original waveform at the fixed frequency output by the analog-to-digital converter according to the sampling clock, performing resampling on the original waveform, generating a reconstructed waveform at any required frequency, and sending the reconstructed waveform to a first communicating module in the sub-test unit; a second communicating module in a main test unit receiving the reconstructed waveform sent from the first communicating module and sending the reconstructed waveform to a waveform receiving module in the main test unit; and the waveform receiving module storing the received reconstructed waveform into a storage module in the main test unit.

[0018] In a third aspect of the present application, an analog-to-digital mixed test board is provided, including the above signal receiving apparatus.

[0019] In a fourth aspect of the present application, a tester is provided, including a communicating board, a back board, and the above analog-to-digital mixed test board.

[0020] Details of one or more embodiments of the present application are set forth in the

accompanying drawings and the description below, so that other features, objects, and advantages of the present application will be apparent.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] To illustrate the technical solutions in the embodiments of the present application more clearly, the drawings required for describing the embodiments will be described briefly. Apparently, the following described drawings are merely for some embodiments of the present application, and other drawings can be derived from these drawings by one skilled in the art without any creative effort.

[0022] FIG. 1 is a structural block diagram of a signal receiving apparatus in an embodiment.

[0023] FIG. 2 is a schematic structural diagram of a signal generation apparatus in an embodiment.

[0024] FIG. 3 is a schematic structural diagram of a waveform data processing module in an embodiment.

[0025] FIG. 4 is a schematic principle diagram of digital resampling in an embodiment.

[0026] FIG. 5 is a flowchart of a signal receiving method in an embodiment.

DETAILED DESCRIPTION

[0027] To better understand objectives, technical solutions, and advantages of the present application, the following describes the present application with reference to the accompanying drawings and embodiments. The specific embodiments described herein are merely used to explain the present application, and are not intended to limit the present application.

[0028] Unless otherwise defined, the technical or scientific terms referred to in the disclosure shall have the usual meanings understood by one skilled in the art to which the present application belongs. The terms used in the specification of the present application are merely intended to describe specific embodiments, and are not intended to limit the present application.

[0029] The “connection” in the following embodiments is understood as “electrical connection”, “communicating connection”, or the like if the connected circuits, modules, units, or the like have transmission of electrical signals or data between each other.

[0030] Words in the present application such as “one”, “a”, “a kind of”, and/or “the” do not specifically refer to singular, but may also include plural, unless the context clearly indicates another manner. The terms “include”, “contain”, “have” and any variations thereof referred to specify the presence of the stated features, entirety, steps, operations, components, portions or combinations thereof, but does not rule out the possibility of existing or adding one or more other features, entirety, steps, components, portions or combinations thereof. Meanwhile, the term “and/or” used in the specification includes any and all combinations of the items listed.

[0031] In an embodiment, referring to FIG. 1, a signal receiving apparatus is provided, including a sub-test unit 100 and a main test unit 200.

[0032] The sub-test unit 100 includes a waveform digitizer (DGT) 110, a first communicating module 120, and an external clock chip 130. The sub-test unit may further include an analog-to-digital converter (ADC) 140. The external clock chip 130 is configured to output a sampling clock to the ADC 140, and the sampling clock has a fixed frequency. The waveform

digitizer 110 is connected to the ADC 140 and the first communicating module 120, respectively, and the DGT 110 is configured to receive an original waveform at the fixed frequency output by the analog-to-digital converter according to the sampling clock, perform resampling on the original waveform, generate a reconstructed waveform at any required frequency, and send the reconstructed waveform to the first communicating module 120. In addition, the external clock chip 130 may further be connected to the DGT 110 and output the sampling clock at the fixed frequency to the DGT 110, and the DGT 110 may receive the original waveform according to the sampling clock.

[0033] The main test unit 200 further includes a second communicating module 210, a waveform receiving module 220, and a storage module 230. The second communicating module 210 is connected to the first communicating module 120 and the waveform receiving module 220, respectively, and the second communicating module 210 is configured to receive the reconstructed waveform and send the reconstructed waveform to the waveform receiving module 220. The waveform receiving module 220 is connected to the storage module 230 and configured to store the received reconstructed waveform into the storage module 230.

[0034] The main test unit 200 and the sub-test unit 100 may be taken as a main test board and a sub-test board of a tester, respectively, or may be designed as a same test board. The user may perform parameter configuration on the DGT 110 according to an actual scenario, so that after performing resampling on the original waveform, the DGT 110 generates the reconstructed waveform at any frequency required by the user. Any frequency of the reconstructed waveform set by the user may be less than or equal to the fixed frequency of

the sampling clock. The external clock chip 130 may include a Phase Locked Loop (PLL) clock chip, and the storage module 230 may include a Double Data Rate (DDR) storage module, including DDR4 chips. The first communicating module 120 and the second communicating module 210 may include a gigabit (such as GTX (GT eXtreme)) communicating module, or other types of communicating modules. In actual application, modules in the main test unit 200 and modules in the sub-test unit 100 may be interchanged in a relationship that meets a function, for example, the DGT 110 is located in the main test unit 200, or the like.

[0035] After receiving an analog waveform output by a DUT, the ADC 140 may perform analog-to-digital converting and sampling on the analog waveform according to the sampling clock at the fixed frequency to generate the original waveform and send the original waveform to the DGT 110. The DGT 110 may process the original waveform to generate the reconstructed waveform at any required frequency. The DUT may include a semiconductor chip or other devices. The quantity of the ADC 140 may be one or more. For example, for IQ channels of the tester, one or more ADCs 140 may be disposed for each of the IQ channels, receive the analog waveform output by the DUT, and perform analog-to-digital conversion on the analog waveform based on the sampling clock.

[0036] Referring to FIG. 2, the DGT 110 may further include a synchronization control module 112 and a waveform data processing module 114. The synchronization control module 112 may be connected to the waveform data processing module 114 and the ADC 140, respectively, and configured to receive the original waveform at the fixed frequency output

by the ADC 140, and send the original waveform to the waveform data processing module 114 after receiving a trigger signal. The waveform data processing module 114 may be connected to the first communicating module 120 and configured to perform resampling on the original waveform, generate the reconstructed waveform at any required frequency, and send the reconstructed waveform to the first communicating module 120. Furthermore, the sub-test unit 100 may further include a first service decoding module 150, the first service decoding module 150 may be connected to a host, the DGT 110, and the external clock chip 130, respectively, and the first service decoding module 150 may be configured to perform parameter configuration on the DGT 110 and the external clock chip 130 according to an instruction delivered by the host.

[0037] The DGT 110, the first communicating module 120, and the first service decoding module 150 may be disposed in a Field-Programmable Gate Array (FPGA), the external clock chip 130 and the ADC 140 may be located outside the FPGA. A port PLL_CTRL of the first service decoding module 150 may be connected to the external clock chip 130 through a Serial Peripheral Interface (SPI) to configure parameters of the external clock chip 130, so that the external clock chip 130 may output the sampling clock at the fixed frequency to the ADC 140. The external clock chip 130 may be configured to output a sampling clock at an allowable maximum frequency (such as 400 MHz), or may be configured to output a sampling clock at another frequency. The port DTG_CTRL of the first service decoding module 150 may be connected to the synchronization control module 112 and the waveform data processing module 114 for parameter configuration, respectively.

[0038] Referring to FIG. 2, the synchronization control module 112 may further include a synchronous receiving control module 1122 and an acquired signal processing module 1124. The synchronous receiving control module 1122 may be connected to the acquired signal processing module 1124 and two or more ADCs 140, respectively, and configured to receive original waveforms output by the two or more ADCs 140, and synchronously send the original waveforms to the acquired signal processing module 1124 after receiving a trigger signal. The acquired signal processing module 1124 may be connected to the waveform data processing module 114, and configured to synthesize the received original waveforms and output a synthesized original waveform to the waveform data processing module 114.

[0039] Similarly, taking that the tester includes IQ channels as an example, two ADC chips may be configured for each of the IQ channels. The acquired signal processing module 1124, the waveform data processing module 114, the first communicating module 120, and the second communicating module 210 may be configured for each of the IQ channels. The synchronous receiving control module 1122 may receive two original waveforms of each of the IQ channels through a Low-Voltage Differential Signaling (LVDS) interface and cache the two original waveforms in an internal First Input First Output (FIFO) cache. After receiving a trigger signal TRIG sent by the first service decoding module 150, the synchronous receiving control module 1122 may output two original waveforms of the same channel in the internal FIFO cache to a corresponding acquired signal processing module 1124. The acquired signal processing module 1124 may synthesize the two original waveforms of the same channel into one original waveform and output the synthesized

original waveform to the waveform data processing module 114. By synthesizing the two original waveforms into one original waveform of an I channel / a Q channel, influence of noise may be reduced and a SNR index may be improved. The waveform data processing module 114 may perform digital signal processing such as alternating current (AC) calibration, direct current (DC) calibration, resampling control, and low-pass filtering according to an instruction (e.g., a DTG_Digital_CTRL_SIGNAL instruction) delivered by the first service decoding module 150, generate the reconstructed waveform at the required frequency, and send the reconstructed waveform to the first communicating module 120. The first communicating module 120 may include a GTX communicating module, which is configured to convert the reconstructed waveform with a bit width of 32 bits into a reconstructed waveform with a bit width of 64 bits and transmit the reconstructed waveform with the bit width of 64 bits to the second communicating module 210, so as to improve communicating bandwidth. The second communicating module 210 may include a GTX communicating module, which is configured to convert the received reconstructed waveform with the bit width of 64 bits into a reconstructed waveform with a bit width of 32 bits and send the reconstructed waveform with the bit width of 32 bits to the waveform receiving module 220.

[0040] Referring to FIG. 2, for four ADC chips of the IQ channels, the sampling clock may be set to a fixed maximum sampling clock (400MHz), but the user requires a waveform at any frequency. In this case, the waveform data processing module 114 may need to resample the original waveform sampled at the fixed frequency. Meanwhile, in the resampling process, an initial phase of the reconstructed waveform generated by resampling may be changed by

setting the initial phase, so as to realize adjustable function of any frequency and any phase of the IQ channels. The IQ function may be realized by a conventional ADC chip, and functions of two non-IQ channels may also be realized, without the need for the external clock chip 130 to adjust the frequency of the sampling clock, thereby simplifying operation and improving test efficiency.

[0041] Furthermore, the synchronous receiving control module 1122 may also collect the original waveform and an associated clock data_clk output by the ADC 140 simultaneously according to the sampling clock to ensure synchronization of output sampled data. Similarly, taking that the tester includes two IQ channels as an example, both the sampling clocks input to two ADC chips of each of IQ channels may be provided by the external clock chip 130, and the external clock chip 130 may also transmit the sampling clock to the synchronous receiving control module 1122, so the sampling clock input to the synchronous receiving control module 1122 and the sampling clocks of the four ADC chips may have the same source and the same frequency, and the synchronous receiving control module 1122 may use the input sampling clock to perform digital sampling on the four ADC chips simultaneously.

[0042] Since output data of the ADC chips is output in a DDR double-edge sampling manner, the synchronous receiving control module 1122 may simultaneously sample original waveforms and associated clocks data_clk output from the four ADC chips by using the sampling clock input by the external clock chip 130, and determine a double-edge sampling result of ADC data according to a sampling result of the associated clock data_clk of each of the four ADC chips. When the sampling result of the associated clock data_clk of the ADC is

high, the ADC data may be sampled in an odd number, otherwise, the ADC data may be sampled in an even number. After obtaining data sampling results of the four ADC chips, the synchronous receiving control module 1122 may arrange 4 pieces of 16-bit sampling data into 64-bit data according to a channel sequence, and take the input sampling clock as a write clock to write the 64-bit data into a cross-clock domain FIFO cache. After the cross-clock FIFO cache is not empty, the synchronous receiving control module 1122 may take a system clock as a read clock to read out the data in the cache to complete a cross-clock domain conversion operation. After the cross-clock domain is converted into the system clock, data synchronization control of the four ADC chips may still be maintained.

[0043] After obtaining the data of the four ADCs based on the system clock, the synchronous receiving control module 1122 may divide the 64-bit data into 4 pieces of 16-bit data according to the channel sequence, and then the acquired signal processing module 1124 may combine the data of ADC0 of the I channel and the data of ADC1 of the I channel into one piece of data, and combine the data of ADC0 of the Q channel and the data of ADC1 of the Q channel into one piece of data. Two pieces of data of the I channel may be directly added, and two piece of data of the Q channel may be directly added. In this case, synchronous collecting control of the data of the I channel and the data of the Q channel may be completed.

[0044] After receiving the trigger signal TRIG sent by the first service decoding module 150, the synchronous receiving control module 1122 may determine whether an operating mode delivered by the first service decoding module 150 is an IQ mode, if yes, as long as the trigger signal TRIG of one channel of the two IQ channels is pulled up, the synchronous receiving

control module 1122 may control the two IQ channels to start collecting data at the same time, and transmit integrated data of the I channel and the Q channel to the waveform data processing module 114 of a subsequent stage for processing. In this case, the synchronous receiving control module 1122 may output the data of the two IQ channels synchronously until a collecting length is reached, and then the synchronous receiving control module 1122 may not send the data of the I channel and the Q channel to the waveform data processing module 114. When the trigger signal TRIG is not received, the synchronous receiving control module 1122 may not send the data of the I channel and the Q channel to the waveform data processing module 114. When the operation mode is not the IQ mode, the synchronous receiving control module 1122 may control the data collected by the two IQ channels to be output to the waveform data processing module 114 of the subsequent stage according to respective trigger signals TRIG of the two IQ channels.

[0045] It may be understood that, a specific structure of the waveform data processing module 114 may not be unique. The waveform data processing module 114 may include a calibrating module and a digital resampling module. The calibrating module may be connected to the synchronization control module 112, and configured to perform calibration on the received original waveform and output calibrated waveform data. The digital resampling module may be connected to the calibrating module and the first communicating module 120, and configured to perform resampling on the calibrated waveform data to generate the reconstructed waveform at any required frequency and send the reconstructed waveform to the first communicating module 120.

[0046] Referring to FIG. 3, the calibrating module may specifically include at least one of a Direct Current (DC) calibrating module 40, an Alternating Current (AC) amplitude calibrating module 41, or a low-pass filtering module 42. Taking that the calibrating module includes the DC calibrating module 40, the AC amplitude calibrating module 41, and the low-pass filtering module 42 as an example, all the DC calibrating module 40, the AC amplitude calibrating module 41, and the low-pass filtering module 42 may be connected to the first service decoding module 150, the DC calibrating module 40 may be connected to the acquired signal processing module 1124 in the synchronization control module 112, the AC amplitude calibrating module 41 may be connected to the DC calibrating module 40 and the low-pass filtering module 42, and the low-pass filtering module 42 may be connected to the digital resampling module. The DC calibrating module 40 may perform DC calibration on the received original waveform according to a DC calibration coefficient delivered by the first service decoding module 150, and send the calibrated waveform to the AC amplitude calibrating module 41, so as to ensure that amplitude precision of channel data meets an indicator requirement. Since the IQ channels require relatively high flatness of the AC, the AC amplitude calibrating module 41 may further perform AC amplitude calibration on the waveform after the DC calibration according to an AC calibration coefficient delivered by the first service decoding module 150, so as to ensure that the amplitude precision of the channel data meets the indicator requirement. The AC amplitude calibrating module 41 may send the waveform after the AC amplitude calibration to the low-pass filtering module 42. The low-pass filtering module 42 may generate a filter coefficient according to a low-pass filter

parameter delivered by the first service decoding module 150, and perform low-pass filtering processing on the waveform, so as to reduce impact of high-frequency noise and improve performance. The waveform after processing of the low-pass filtering module 42 may be sent to the digital resampling module.

[0047] The external clock chip 130 may be set at a fixed maximum sampling clock frequency, and the ADC 140 may sample an analog waveform based on the maximum sampling clock frequency. A function of the digital resampling module may be to resample the original waveform at the maximum sampling clock frequency into the reconstructed waveform at the required frequency. A principle of resampling is to use a SINC function to perform waveform recovery on a continuous signal. Since the DGT 110 resamples an original waveform at a fixed maximum sampling frequency into the reconstructed waveform at any frequency (less than or equal to the fixed maximum sampling frequency) and a frequency after resampling is less than or equal to a fixed maximum sampling rate, a function implemented by the DGT 110 may be summarized as a decimation function with any decimal multiple. For a known continuous waveform x (n), data resampling recovery may be performed by using the SINC function to recover x (n) to x (t) at any time. By using 8 forward points and 8 backward points of a location of a valid point to be recovered, an actual value of the recovered point may be obtained after a convolution operation of 16 pieces of data of the 8 forward points and 8 backward points and 16 continuous SINC coefficients is performed.

[0048] To recover an ideal SINC function, countless sets of coefficients may be required to perform the operation in theory. Apparently, it is not feasible. Therefore, a model of the SINC

function may be selected and divided into 1024 groups of coefficients, each of which includes 16 coefficients stored in a ROM, and a valid coefficient may be read from the ROM according to the valid location information. Since infinite multiple groups of coefficients cannot be stored, for higher precision, the stored coefficients may not be directly used when calculating the valid coefficient, but be considered as continuous coefficients between each group of coefficients, and the valid coefficient of any point may be obtained by using a linear weighting algorithm.

[0049] Based on this, referring to FIG. 3, the digital resampling module may include an input waveform data cache module 43, a valid location calculating module 44, a valid coefficient generating module 45, a valid data cache module 46, and a data calculating module 47. The input waveform data cache module 43 may be connected to the calibrating module, the valid location calculating module 44, and the valid data cache module 46, respectively. The valid location calculating module 44 may be connected to the valid coefficient generating module 45, the valid coefficient generating module 45 may be connected to the data calculating module 47 and the valid data cache module 46, respectively, and the valid data cache module 46 may be connected to the data calculating module 47.

[0050] Specifically, the input waveform data cache module 43 may be connected to the low-pass filtering module 42 in the calibrating module, and configured to cache the calibrated waveform data, send a start signal SINC_START to the valid location calculating module 44 when the quantity of cached data is greater than a specified threshold quantity, read valid data corresponding to a valid location from the cached data according to a received read enable

signal, and send the read valid data to the valid data cache module 46 for caching. The valid location calculating module 44 may be configured to obtain valid location information by calculation according to a set step and an initial phase after receiving the start signal SINC_START, send the valid location information to the valid coefficient generating module 45, and send the read enable signal to the input waveform data cache module 43. The valid coefficient generating module 45 may be configured to read a coefficient from a plurality of groups of pre-stored coefficients according to the valid location information, to obtain a valid coefficient and send the valid coefficient to the data calculating module 47, and send a data-read enable signal to the valid data cache module 46. The valid data cache module 46 may be configured to read cached valid data according to the received data-read enable signal and send the cached valid data to the data calculating module 47. The data calculating module 47 may be configured to perform convolution calculation according to the received valid coefficient and the received valid data to obtain the reconstructed waveform and send the reconstructed waveform to the first communicating module 120. A convolution formula may be as follows:

$$\mathrm{DATA_VALID} = \sum_{k=0}^{15} \mathrm{COE}[k] * \mathrm{DATA_IN}[16 - k]$$

DATA_VALID represents a reconstructed point of the reconstructed waveform, COE represents a valid coefficient (16 valid coefficients in total) corresponding to a valid location of the reconstructed point, and DATA_IN represents valid data (16 points, including 8 forward points and 8 backward points of the valid location) corresponding to the valid location. After

16 times of multiplication and accumulation of the valid coefficient and the original waveform are performed, a corresponding reconstructed point of the reconstructed waveform may be obtained.

[0051] A value of the specified threshold quantity may not be unique and may be set as required. The first service decoding module 150 may be connected to the valid location calculating module 44, and configure the set step STEP and the initial phase PHASE. The digital resampling module may resample an initial waveform at a variable sampling frequency to the reconstructed waveform at the fixed maximum sampling frequency. In addition, since the digital resampling module performs digital resampling, phase adjustment of an output waveform may be further implemented, and adjustment precision may be up to 1ps.

[0052] Specifically, after the input waveform data cache module 43 receives the waveform data output from the low-pass filtering module 42, the waveform data may be cached in the internal cache unit (e.g., the FIFO). When the quantity of cached data is greater than the specified threshold quantity (e.g., 16), the input waveform data cache module 43 may send the start signal SINC_START to the valid location calculating module 44. After receiving the start signal SINC_START, the valid location calculating module 44 may start to operate, and perform valid location calculating according to the step STEP and the initial phase PHASE that are sent by the first service decoding module 150. The valid location may be understood as a location of a reconstructed waveform point, and the calculated valid location may include a 16-bit integer and a 48-bit decimal. An initial location of the reconstructed waveform may be determined by the initial phase PHASE, and the initial location may refer to a valid location

of a first point of the reconstructed waveform. A relationship between the location of the reconstructed waveform point and a location of an original waveform point may be as follows: the location of the reconstructed waveform point = (the location of the original waveform point - 1) * STEP + 1 + PHASE. The location of the original waveform point may be a location of a calibrated waveform data point, and DC calibration, AC amplitude calibration, and filtering processing may not change the location of the original waveform point.

[0053] The step STEP = the fixed maximum sampling rate (the frequency of the sampling clock) / a sampling rate (the frequency of the reconstructed waveform) set by the user the fixed. Since the sampling rate set by the user is less than or equal to the fixed maximum sampling rate, a value of the STEP may be greater than or equal to 1, which may be understood as a decimation operation with any multiple. The step STEP may include the 16-bit integer and the 48-bit decimal. Since the fixed maximum sampling frequency is set as 400 MHz and a 48-bit decimal is supported to uHz, the sampling rate of resampling may have a precision of uHz. uHz adjustment may be implemented to achieve sampling rate resolution. Assuming that A = 400 MHz = 400*2^10*2^10 Hz and B = 1uHz = (1/2^10*2^10) Hz, A/B = 400*2^10*2^10 Hz / (1/2^10*2^10) Hz = 400*2^40 = 49 bit. Since an SINC algorithm divides the coefficient into 1024 pieces, the minimum location information may need 400*2^40/1024 bit = 39 bit. In the present application, 48 bit may be selected. The initial phase PHASE = the quantity of the points in a waveform period / (360° / a phase of the reconstructed waveform), and an output result may be represented by the 16-bit integer and the 48-bit decimal, so that ps-level phase adjustment may be performed.

[0054] After obtaining the valid location information according to the set step STEP and the initial phase PHASE, the valid location calculating module 44 may output the valid location information to the valid coefficient generating module 45, and send the read enable signal to the input waveform data cache module 43 according to the obtained valid location. The input waveform data cache module 43 may read, according to the read enable signal sent by the valid location calculating module 44, one piece of data, and send the piece of data to the valid data cache module 46. In this case, the piece of data stored in the valid data cache module 46 may be valid data of the valid location. After the valid coefficient generating module 45 calculates the valid coefficient of the valid location, the valid data cache module 46 may read the valid data and send the valid data to the data calculating module 47 for calculation.

[0055] The valid coefficient generating module 45 may store multiple groups (e.g., 1024 groups) of coefficients (16 coefficients in each group) in an internal ROM (read-only memory) unit in advance. After receiving the valid location information, the valid coefficient generating module 45 may read two adjacent groups of coefficients according to integer location information of the valid location information, and calculate the two adjacent groups of coefficients by using a linear interpolation algorithm according to the decimal location information of the valid location information to obtain the valid coefficient.

[0056] Specifically, the valid coefficient generating module 45 may read a pre-stored coefficient from the ROM unit according to the valid location information. Since there are 1024 groups of pre-stored coefficients and 48-bit decimal precision cannot be met, in this case, the valid coefficient generating module 45 may read two adjacent groups of coefficients (16

coefficients in a group) according to the integer location information of the valid location information, and calculate the two groups of coefficients according to the decimal location information of the valid location information by the linear interpolation algorithm: Y_coe[n] = COE1[n]*tim_valid+COE2[n]* (1-tim_valid), n is set to 0-15 to obtain the most accurate valid coefficient (16 coefficients). COE1 represents a first group of coefficients in the two adjacent groups of coefficients that are read out, COE2 represents a second group of coefficients (both the first group of coefficients and the second group of coefficients include 16 coefficients) in two adjacent groups of coefficients that are read out, tim_valid represents the decimal location information of the valid location information, and y_coe represents the valid coefficient (16 coefficients) of the decimal position in actual valid location information that is obtained by the linear interpolation.

[0057] The valid data cache module 46 may store the valid data in a shift manner in parallel into continuous internal cache units (e.g., FIFO). Specifically, the valid data cache module 46 may store the valid data in 16 FIFOs in a shift manner in parallel. A specific representation of the parallel storage may be as follows: latest input data may be stored in FIFO1, original data in the FIFO1 may be stored in FIFO2, and original data in the FIFO2 may be stored in FIFO3, ⋯, i.e., 16 consecutive pieces of data may be stored in the 16 FIFOs.

[0058] After generating a valid coefficient, the valid coefficient generating module 45 may output the valid coefficient to the data calculating module 47, and simultaneously send a data-read enable signal to the valid data cache module 46. The valid data cache module 46 may simultaneously read 16 pieces of valid data in the 16 FIFOs according to the data-read enable

signal, and output the 16 pieces of valid data to the data calculating module 47. The data calculating module 47 may perform 16-order convolution calculation according to the valid coefficient output from the valid coefficient generating module 45 and the valid data output from the valid data cache module 46, to obtain the reconstructed waveform after resampling and output the reconstructed waveform to the subsequent first communicating module 120.

[0059] The following is an example for description. It is assumed that condition 1: the sampling rate (the frequency of the reconstructed waveform) is set by the user to 200 MHz, condition 2: a phase of the reconstructed waveform is set to 3.6°, and condition 3: the original waveform is an analog waveform with a signal frequency of 8 MHz. In this case, the data collected by the ADC may include 50 points in a waveform period (the quantity of sampling points in a waveform period = the fixed maximum sampling rate / signal frequency = 400 MHz / 8 MHz = 50). In this case, the step STEP = the fixed maximum sampling rate / the sampling rate set by the user = 400 M/200 M = 2, the initial phase PHASE = the quantity of points in a waveform period / (360° / the phase of the reconstructed waveform) = 50 / (360 / 3.6) = 0.5. Referring to FIG. 4, in the reconstructed waveform, the valid location of a first point may be determined according to the initial phase PHASE, and the reconstructed waveform point may be corresponding to the valid location in the original waveform. The relationship between the location of the reconstructed waveform point and the location of the original waveform point may be as follows: the location of the reconstructed waveform point = (the location of the original waveform point – 1) *STEP + 1 + PHASE = (the location of the original waveform point – 1) *2 + 1 + 0.5, such as 1----1.500, 2----3.500, 3----5.500, and

4-----7.500. Referring to FIG. 4, it is described that the effects of the frequency set by the user, the quantity of waveform points, and the initial phase on resampling, and a relationship between the frequency set by the user, the quantity of waveform points, the initial phase and the valid location.

[0060] In an embodiment, referring to FIG. 2, the main test unit 200 may further include a second service decoding module 240, the second service decoding module 240 may be connected to the host and the waveform receiving module 220, respectively, and the second service decoding module 240 may be configured to perform parameter configuration on the waveform receiving module 220 according to an instruction delivered by the host and perform waveform reading operation on the storage module 230 by the waveform receiving module 220. The second communicating module 210, the waveform receiving module 220, and the second service decoding module 240 may be disposed in the FPGA, and the storage module 230 may be located outside the FPGA. Both the first service decoding module 220 and the second service decoding module 240 may be directly controlled by the host, the host may independently send parameter configuration, and the first service decoding module 220 and the second service decoding module 240 may not affect each other and be two independent modules. The waveform receiving module 220 may specifically include a receiving control module 222 and a read-write control module 224. The receiving control module 222 may be connected to the second communicating module 210 and the read-write control module 224, respectively, and configured to receive the reconstructed waveform by the second communicating module 210 and send a write request instruction to the read-write control

module 224. The read-write control module 224 may be connected to the storage module 230, and configured to store the reconstructed waveform into the storage module 230 according to the write request instruction.

[0061] A port DTG_CTRL of the second service decoding module 240 may be connected to the receiving control module 222, and configured to perform parameter configuration on the receiving control module 222. A port DDR_RQE of the second service decoding module 240 may be connected to the read-write control module 224, and configured to perform waveform reading operation on the storage module 230 by the read-write control module 224. Specifically, after receiving the reconstructed waveform, the receiving control module 222 may initiate a write request instruction of the I channel and/or the Q channel to the read-write control module 224 according to information such as a sampling length and a storage address delivered by the second service decoding module 240, and the read-write control module 224 may write the reconstructed waveform of the I channel and/or the Q channel into the storage module 230 according to the write request instruction.

[0062] Referring to FIG. 2 and FIG. 3, the following describes a complete processing of the original waveform: after the signal receiving apparatus is powered on, the host may be in communication with the first service decoding module 150 and the second service decoding module 240, respectively, and deliver instructions. The first service decoding module 150 may perform parameter configuration on the waveform data processing module 114 and the external clock chip 130, so that the external clock chip 130 may output the sampling clock at the fixed frequency to the ADC 140, and the second service decoding module 240 may

perform parameter configuration on the receiving control module 222.

[0063] The synchronous receiving control module 1122 may receive the original waveform output by the ADC chip for caching, and after receiving the trigger signal TRIG sent from the first service decoding module 150, the synchronous receiving control module 1122 may output the original waveform to the acquired signal processing module 1124 for waveform synthesis, and input the synthesized original waveform into the waveform data processing module 114 for resampling. In the waveform data processing module 114, the DC calibrating module 40 and the AC amplitude calibrating module 41 may sequentially perform DC calibration and AC amplitude calibration on the original waveform according to a configured DC calibrating coefficient and an AC calibrating coefficient, and the low-pass filtering module 42 may perform low-pass filtering processing on the calibrated waveform according to a configured low-pass filtering parameter, and then send the low-pass filtered waveform to the input waveform data caching module 43 for caching. The input waveform data caching module 43 may send the start signal SINC _ START to the valid location calculating module 44 when the quantity of cached data is greater than the specified threshold quantity. The valid location calculating module 44 may obtain valid location information by calculation according to the set step and the initial phase after receiving the start signal SINC_START, send the valid location information to the valid coefficient generating module 45, and send the read enable signal to the input waveform data cache module 43. The input waveform data cache module 43 may read valid data corresponding to the valid location from the cached data according to the received read enable signal, and send the read valid data to the valid data

cache module 46 for caching. The valid coefficient generating module 45 may read the coefficient from the plurality of groups of pre-stored coefficients according to the valid location information, to obtain the valid coefficient and send the valid coefficient to the data calculating module 47, and send the data-read enable signal to the valid data cache module 46. The valid data cache module 46 may read cached valid data according to the received data-read enable signal and send the cached valid data to the data calculating module 47. The data calculating module 47 may perform convolution calculation according to the received valid coefficient and the received valid data to obtain the reconstructed waveform and send the reconstructed waveform to the first communicating module 120.

[0064] After receiving the reconstructed waveform through the second communicating module 210, the receiving control module 222 may send the write request instruction to the read-write control module 224 according to the parameter configured by the second service decoding module 240, and the read-write control module 224 may store the reconstructed waveform into the storage module 230 according to the write request instruction. The host may deliver an instruction to the read-write control module 224 to read the reconstructed waveform in the storage module 230.

[0065] In an embodiment, referring to FIG. 5, a signal receiving method is further provided, including step 110 to step 140.

[0066] Step 110 includes an external clock chip in a sub-test unit outputting a sampling clock to an ADC, and the sampling clock having a fixed frequency.

[0067] Step 120 includes a DGT in the sub-test unit receiving an original waveform at the

fixed frequency output by the ADC according to the sampling clock, performing resampling on the original waveform, generating a reconstructed waveform at any required frequency, and sending the reconstructed waveform to a first communicating module in the sub-test unit.

[0068] Step 130 includes a second communicating module in a main test unit receiving the reconstructed waveform sent from the first communicating module and sending the reconstructed waveform to a waveform receiving module in the main test unit.

[0069] Step 140 includes the waveform receiving module storing the received reconstructed waveform into a storage module in the main test unit.

[0070] It may be understood that a specific implementation of the above signal receiving method is explained in detail in the above signal receiving apparatus, and is not be repeated herein.

[0071] In an embodiment, an analog-to-digital mixed test board is further provided, including the foregoing signal receiving apparatus.

[0072] In an embodiment, a tester is further provided, including a communicating board, a back board, and the foregoing analog-to-digital mixed test board. The communicating board is connected to the analog-digital mixed test board by the back board. In addition, the tester may further include a host in communication with the communicating board, and the host may include, but not be limited to, various personal computers, notebook computers, smart phones, tablet computers and portable wearable devices, and the portable wearable devices may include smart watches, smart bracelets, head-mounted devices, etc.

[0073] The above signal receiving apparatus and method, the analog-to-digital mixed test

board, and the tester may have the following advantages.

[0074] 1. In the present application, the sampling clock of the ADC chip with fixed frequency may be used. After being powered on and initialized, the external clock chip may not need to be repeatedly configured, thereby reducing locking time of the clock chip generated by changing the sampling clock, and improving test efficiency.

[0075] 2. In the present application, the sampling clock of the ADC chip with fixed frequency may be used, and a resampling operation may be performed by a digital domain algorithm to implement design of any sampling rate, so that an adjustment of sampling rate with a resolution of uHz may be implemented. This indicator requirement is an indicator requirement that is difficult to be implemented in a conventional manner of adjusting the sampling rate by a clock chip.

[0076] 3. In the present application, both an IQ function and a non-IQ function may be implemented, and the use may be more flexible and convenient, thereby improving use efficiency of the apparatus.

[0077] 4. A control manner of the present application may facilitate extension, multiplexing, and transplantation of program channels, and may be directly configured in another project. For program updates, a channel may need to be added or reduced, thereby facilitating program code maintenance.

[0078] The various technical features of the embodiments described above may be combined arbitrarily, and in order to make the description concise, all possible combinations of the various technical features in the embodiments described above are not described, however, as

long as there is no contradiction between these combinations of technical features, they should be considered as the scope of the description.

[0079] The above embodiments only express several implementations of the present application, and the description thereof is more specific and detailed, but it cannot be understood as a limitation to the scope of the present application. It should be noted that a person of ordinary skill in the art may further make several variations and improvements without departing from the concept of this application, which all fall within the protection scope of this application. Therefore, the protection scope of the present application shall be subject to the appended claims.