THIN CHIP-SIZE INTEGRATED CIRCUIT PACKAGE AND METHOD OF FABRICATION

ABSTRACT

In accordance with the present invention, there is provided an electrically insulating substrate having first and second surfaces, an outline and an opening. A plurality of electrically conductive routing strips is integral with the substrate. A plurality of contact pads is disposed on the first surface, at least one of the pads being electrically connected with at least one of the routing strips. A semiconductor chip is adhered to the second surface of the substrate. The chip has an outline that is substantially the same as the outline of the substrate. The chip has at least one bonding pad. Wire bonding electrically connects the bonding pad to a routing strip.

At least one bus bar is integral with the substrate. The bus bar is positioned remote from the substrate opening and is electrically connected to a bonding pad of the chip and to a contact pad disposed on the first surface of the substrate. At least one grounding pad is disposed on the first surface of the substrate, the grounding pad being electrically connected to at least one bus bar. Encapsulating material fills the opening and covers the wire bonding and the bonding pads. Solder balls are disposed on the contact pads positioned on the first surface of the substrate to enable attachment to wiring boards or other devices or applications. The overall profile of the integrated circuit package of the present invention is preferably about 0.78 mm.

Figure 3

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