

Abstract of the Disclosure (FIG. 7)

"FEASIBLE, GAS-DIELECTRIC INTERCONNECT PROCESS"

Wires (W1) are provided on an insulating layer (25), reaching the source region (24a) and drain region (24b) of a MOS transistor. Each wire W1 is composed of a conductor (28a, 28b) and a barrier layer (27a, 27b) covering the surfaces of the conductor. An insulating layer (29) is mounted on the wires (W1), an insulating layer (30) on the insulating layer (29), and an insulating layer (32) on the insulating layer (30). Cavities (31) are provided among the wires (W1). The cavities (31) are filled with air or a mixture gas of oxygen and carbon dioxide. Wires (W2) are provided on the insulating layer (32). Cavities (38) are provided among the wires (W2). These cavities (31) are filled with air or a mixture gas of oxygen and carbon dioxide.