

"A multi-function electronic digital watch"

The present invention relates to a multi-function electronic digital watch of the dynamic logic type wherein timekeeping or displaying are performed by sequentially reading out a series of control instructions written in a read only memory (ROM), in accordance with predetermined timing pulses.

An electronic digital watch needs to have, not only the time indicating function, but also the stop watch function, the timer function, and the calendar function in order to meet present day demands. In order to meet all these functions with static logic, independent logic circuits are required for each respective individual function. This means that the size of the circuit arrangement becomes very large and that the manufacture of the circuit arrangement in the form of a single chip integrated circuit is difficult. In order to solve this problem, there has been employed the so-called dynamic logic system wherein a series of control instructions written in a ROM are sequentially read out according to predetermined timing pulses (for example, clock pulses of the order of 4KHz) defining machine cycles, and predetermined information

processings are completed according to the control instructions and within a fixed time interval (for example, 0.1 sec) making the time base of the watch, whereby timekeeping and displaying are executed.

5 With this system, however, in the case where the stop watch function is added which can measure down to, for example, the digit for 0.01 sec, the time base of the watch needs to be made 0.01 sec. Therefore, the predetermined information processings performed when the time base has been
10 0.1 sec and also information processings increased by the addition of the stop watch function must be completed within 0.01 sec. In order to cope with this situation, the frequency of the timing pulses needs to be made high. The high frequency is attended with increases in the charging and discharging
15 currents of capacitance elements, and stray capacitances of the circuitry, and results in various problems such as increase in the power dissipation and lowering in the speed margin in a low-voltage operation.

Moreover, since the frequency of an oscillator circuit
20 for a watch is a comparatively low frequency of, for example, 32.768 KHz, it is subject to limitation to make the frequency of the timing pulses high as described above. In order to complete all the necessary processings within 0.01 sec as stated above, a high frequency oscillator circuit is required,
25 and the whole circuit arrangement is put into a high frequency

circuit, resulting in problems such as complication of the circuit arrangement and increase in the power dissipation of the oscillator circuit.

It is therefore an object of the present invention to provide a multi-function digital watch which realizes time-keeping in a very short time whilst avoiding complication of a circuit arrangement and rendering the power dissipation of the whole circuit low.

According to the present invention there is provided a multi-function electronic digital watch of the dynamic logic type including: timing means which generates a time base signal; count means to receive a timing signal shorter in period than the time base signal; indication input means; temporary holding means to store an output of said count means upon an indication of said input means; first memory means in which a series of control instructions are written; arithmetic means which is controlled by the control instructions and which executes predetermined operations; second memory means which stores a time signal having a plurality of digits therein; control means coupled to said first and second memory means and to said timing means for sequentially reading out the control instructions of the first memory means, said control instructions being provided to renew a time signal of a less significant digit stored in the second memory means at each occurrence of the time base signal, and to renew a time signal of a more significant digit stored in the second memory means when a signal for renewing the more significant digit has been generated and to deliver a time signal

of a least significant digit determined by the period of said timing signal shorter in period than the time base signal on the basis of an output of said holding means and the time signals stored in
5 said second memory; and output means to deliver a signal including the time signal of the least significant digit.

The present invention will now be described in greater detail by way of example with reference
10 to the accompanying drawings, wherein:-

Figure 1 is a block circuit diagram showing one preferred embodiment of a multi-function electronic digital watch;

Figure 2(a) is a diagram for exemplifying
15 control instructions stored in a ROM;

Figure 2(b) is a diagram for explaining timekeeping which uses some addresses of a RAM;

Figure 3 is a diagram showing the arrangement of segments for indicating numerals
20 in a digital watch;

Figure 4(a) is a block circuit diagram showing the arrangement of an example of a time base circuit in Figure 1; and

Figure 4(b) is a waveform diagram showing
25 signals at various locations in the circuit of Figure 4(a).

Referring first to Figure 1, the digital watch includes: a crystal oscillator 1 which generates a reference frequency

signal of 32.768 KHz; a frequency divider 2 which generates a frequency division output of the reference frequency signal; a timing generating circuit 3 which receives the output signal of the frequency divider 2 and which generates control pulses necessary for dynamic logic operations and supplies them to various circuits; and a ROM 4 in which a series of control instructions necessary for timekeeping and displaying are stored.

The ROM 4 has a memory capacity of, for example, 2,048 words. One control instruction is allotted to one word, and control instructions totalling 2,048 ($=128 \times 16 = 2^7 \times 2^4$) are stored over 16 pages each including 128 control instructions. When the ROM 4 is activated by an output of a decoder 5, each control instruction is read out from the corresponding address into an instruction register 8. In the decoder 5, a page information of 4 bits stored in a page register 7a is decoded so as to select one of the 16 pages. Further, an address information of 7 bits stored in an address register 6a is decoded so as to select one of the 128 ($=2^7$) words included in the selected page.

An address appointment portion 6 comprises the address register 6a, a register 6b which adds "1" to the content of the register 6a, and registers 6c and 6d which store return addresses at the time when subroutine jumps are made due to an interrupt.

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A page appointment portion 7 comprises the page register 7a, a preset register 7b which stores a specified value to be given to the page register 7a, registers 7c and 7d which store return pages at the subroutine jumps, and a
5 buffer register 7e which temporarily stores the address of the ROM 4 stored in the instruction register 8.

The instruction register 8 sets the control instruction read out from the ROM 4. The information of an instruction part in the control instruction is decoded in a decoder 8a,
10 and becomes a control signal for ²executing a predetermined information processing to be performed within one time base. The information of an address part becomes an address of a random access memory (RAM) 9, and it is stored in the address register 6a and the buffer register 7e to become the jump
15 destination address of the ROM 4. It is also possible to ^{by}employ the information of the address part as a control signal or a literal value on the basis of appointment by the information of the instruction part. Time information such as dates, days of the week, and hours, minutes and seconds;
20 information on times to be measured by the stop watch function; information on set times for the timer function; alarm information, can be stored in the RAM 9 as desired. It is possible to read out data from the RAM 9 in accordance with the control instruction of the ROM 4 so as to perform an arithmetic
25 processing or a displaying processing, and also to write the

result of the arithmetic processing into the RAM 9.

The timekeeping by the RAM 9 will now be described with reference to Figures 2(a) and 2 (b). It is assumed that control instructions indicated in Figure 2(a) are success-
5 ively written from page 1, address 0 of the ROM 4. As they are sequentially read out and executed, a time in 0.1 second, a time in 1 second,... are sequentially counted in locations (1, 2), (1, 3), ... of the RAM 9 as indicated in Figure 2(b).

This operation will now be described in greater detail.

10 (i) By executing an instruction --Load 1, 2-- read out from page 1, address 0 of the ROM 4, a value (1, 2) for appointing the location (1, 2) of the RAM 9 is applied to a decoder 10.

15 (ii) By executing an instruction --Binary Add 1-- read out from page 1, address 1 of the ROM 4, the content of the location (1, 2) of the RAM 9 is read out and is stored in an accumulator 11 for operand 1 (hereinafter abbreviated to "ACC 11"), while a value 1 read out from the instruction register 8 is set in an accumulator 12 for operand 2 (here-
20 inafter abbreviated to "ACC 12"). The contents of the ACC 11 and the ACC 12 are added in an arithmetic logic unit 13 (hereinafter abbreviated to "ALU 13") and the result is stored in the location (1, 2) of the RAM 9 through a bus line 21 of 4 bits.

(iii) By executing an instruction --Less Than 10-- read out from page 1, address 2 of the ROM 4, the subtraction between the content A of the location (1, 2) of the RAM 9 and a value 10 from the instruction register 8 is performed in the ALU 13, and the borrow bit of the result is checked:

If borrow = 1 ($A - 10 < 0$), the operation proceeds to the next step (iv).

If borrow = 0 ($A - 10 \geq 0$) the operation proceeds to the next but one step (v).

(iv) By executing an instruction --Branch 20-- read from page 1, address 3 of the ROM 4, the operation branches to page 1, address 20 of the ROM 4 and an instruction --Halt-- stored therein is executed. Thereafter, unless interrupt or the like occurs, the state of "halt" is held until the next period of 0.1 sec begins.

(v) By executing an instruction --Transfer 0-- read out from page 1, address 4 of the ROM 4, a value 0 from the instruction register 8 is set in the location (1, 2) of the RAM 9 through the ALU 13. (As a result, the location (1, 2) of the RAM 9 is cleared.)

(vi) By executing an instruction --Load 1, 3-- read out from page 1, address 5 of the ROM 4, a value (1, 3) for appointing the location (1, 3) of the RAM 9 is applied to the decoder 10.

(vii) Likewise to step (ii), "1" is added to the location (1, 3) of the RAM 9. (This corresponds to the fact that a carry has occurred in a counter for the digit of 0.1 sec executed in the location (1, 2) of the RAM 9 as indicated in Figure 2(b), the timekeeping of the digit of 1 sec having been performed.) Thereafter, the timekeeping of the digit of 10 sec is performed in location (1, 4) of the RAM 9. Similarly, the timekeeping of the digit of 1 minute is performed in location (1, 5) of the RAM 9, that of the digit of 10 minutes in location (1, 6), etc.

That is, since the present register 7b is set to page 1, address 0 at intervals of 0.1 sec, the timekeeping in 0.1 sec is permitted by executing the flow described above. The instruction in each step of the flow is executed within 1 machine cycle (for example, 250 μ s). 'Content' and 'Value' in Figure 2(b) indicate an example of the content in the course of the timekeeping in each address of the RAM 9 and an example of the corresponding time.

In order to display a time formed in the RAM 9, the contents of the addresses of the RAM 9 corresponding to the respective digits of the time are read out by control instructions, and they are decoded by a display decoder 14 through the ACC 11 and then latched in a latch circuit 15. An output of the latch circuit 15 is applied to a display 20, and becomes an appointment for appointing segments

corresponding to a numeral to-be-displayed among numeral segments $S_1 - S_7$ which are illustrated in Figure 3 by way of example.

On the other hand, in case of appointing the digit to be displayed, a digit appointment instruction is read out from the ROM 4, and a signal obtained by decoding the instruction is applied as a digit appointment signal to the display 20 through a digit select circuit 19.

The display 20 is driven by the segment appointment signal and the digit appointment signal, and the segments corresponding to the appointed digit are driven. The timer function, for example, may be realized in such a way that a time to be externally set is stored in a location of the RAM 9 by means of a key input circuit 16, that the content of the location is counted down in units of 0.1 sec, 1 sec etc. from the least significant digit, and that when the content has become "0", a drive signal for, e.g., an alarm device (not shown) is generated.

The above operation has previously been performed. In this case, only the timekeeping in 0.1 sec is possible, and the timekeeping in units of a shorter time is difficult.

This invention makes possible the timekeeping, and the displaying in units of a very short time, for example, 0.01 sec.

By taking as examples the timekeeping and the displaying in 0.01 sec in the stop watch function, this invention

will now be described with reference to the operations of a time base circuit 17 and its peripheral circuitry.

As shown in Figure 4(a), the time base circuit 17 is made up of a decimal counter of 4 bits 41 which is caused to free run by pulses having a period of 0.01 sec, an AND gate 43 which produces a decimal output from the contents of the respective bits of the counter 41, and a latch circuit of 4 bits 44 which latches the contents of the counter. A time at the digit of 0.01 sec is stored in address 1, for example, of the RAM 9.

Timing pulses having a period of 0.01 sec (hereinafter called " T_{100} ") formed by the frequency divider 2 are applied to a clock terminal 42-1 of the counter 41 of the time base circuit 17. Timing pulses having a period of 0.1 sec (hereinafter called " T_{10} ") are produced from outputs of the respective bits of the counter 41 by means of the AND gate 43, and they are applied to a start circuit 18. In addition, a key signal such as start or stop signal generated in a key input circuit 16 is applied to the start circuit 18.

The start circuit 18 is a circuit according to which, when the start or stop signal has been received upon depression of a start or stop key, a signal is fed to the preset register 7b in synchronism with the timing T_{10} so as to set a predetermined value therein, and simultaneously, a starting pulse synchronized with the timing T_{10} is transmitted to the

timing generating circuit 3. This start circuit can be constructed from conventional logic circuits.

When the start key of the stop watch has been depressed, the start signal generated by the key input circuit 16 is applied to a key input terminal 42-2 in the time base circuit 17, and the content of the counter 41 is latched in the latch circuit 44. At the same time, the start signal is applied to the start circuit 18. In order to jump to that page in the ROM 4 in which is stored the first control instruction among a series of control instructions necessary for realizing the stop watch function, the output of the start circuit 18 based on the start signal becomes an interrupt signal for setting the jump destination page in the preset register 7b. In accordance with control pulses generated by the timing generating circuit 3, desired control instructions are read out from the corresponding pages of the ROM 4 on the basis of the pages set in the preset register 7b and are sequentially executed.

The processing is performed such that the content of the latch circuit 44 of the time base circuit 17 immediately after the start signal has turned "on" is stored in a predetermined address of the RAM 9 (location 1, 1) in the example of Figure 2 (b)) through the bus line of 4 bits 21. Thereafter, lapsed times are stored in predetermined addresses of the RAM 9 (location (1, 2) and succeeding locations in

the example of Figure 2(b)) in units of 0.1 sec.

While performing the above timekeeping, and by occupying several machine cycles within the 0.1 sec interval, the displaying is performed in such a way that the contents of addresses corresponding to the respective digits are read out from the RAM 9, that they are decoded by the display decoder 14 and that the decoded results are latched in the latch circuit 15 so as to appoint segments of a numeral to-be-displayed, and besides, that a digit appointment instruction is read out from the ROM 4 and is executed so as to appoint a digit, signals of the appointments being delivered to the display 20. During the timekeeping of the stop watch, even when the digit of 0.01 sec is displayed the display is difficult to be visually discerned, and hence, the digit of 0.01 sec may be displayed, for example, as numeral "8" by selecting all the display segments $S_1 - S_7$.

When the stop key has been subsequently depressed, the content of the counter 41 in the time base circuit 17 is latched in the latch circuit 44 by the stop signal generated in the key input circuit 16. At the same time, the stop signal is applied to the start circuit 18 likewise to the start signal described above. The output of the start circuit 18 based on the stop signal becomes an interrupt signal for setting a jump destination page in the preset register 7b. Using this page, the operation is caused to jump to that page of the ROM 4 in which is stored the first

control instruction among a series of control instructions necessary for correcting a time in the RAM 9 at the stop of the stop watch down to the digit of 0.01 sec and then displaying the corrected time.

5 In accordance with control pulses generated by the timing generating circuit 3, desired control instructions are read out from the corresponding pages of the ROM 4 on the basis of the pages set in the preset register 7b and are sequentially executed.

10 The content of the latch circuit 44 of the time base circuit 17 immediately after the stop signal has turned "on" is stored in a previously appointed address of the RAM 9 through the bus line of 4 bits 21.

 Subsequently, the time of the digit of 0.01 sec at the
15 stop as stored in the RAM 9 and the time of the digit of 0.01 sec at the start as stored in the location (1, 0) of the RAM 9 are read out, and the difference between the times is calculated in the ALU 13, whereby the correction for the digit of 0.01 sec is made. The time of the digit
20 of 0.01 sec after the correction is decoded by the display decoder 14, the decoder output is latched in the latch circuit 15 and becomes a display segment appointment signal, and simultaneously with the execution of a digit appointment instruction, the exact time of the digit of 0.01 sec is displayed.
25 Thereafter the time of the digit of 0.1 sec, the

time of the digit of 1 sec, the time of the digit of 10 sec ...
are sequentially displayed, and an exact stop watch function
is realized in unit of 0.01 sec.

Assuming by way of example that the content of the counter
41 at the start is (1000), i.e., 0.08 second and that the
measured time at the stop as includes the digit of 0.01 sec
is '11 minutes 25.03 seconds', the ALU 13 executes the operation:

$$\begin{aligned} & 11 \text{ minutes } 25.03 \text{ seconds} - 0.08 \text{ second} \\ & = 11 \text{ minutes } 24.95 \text{ seconds} \end{aligned}$$

and an exact timekeeping is performed in unit of 0.01 sec.

It is also possible to perform the lap operation of the
stop watch in unit of 0.01 sec.

Assuming by way of example that the content of the
counter 41 of the time base circuit 17 at the start is
B = (0101), i.e., 0.05 sec and that the measured times at
the first, second ... laps are A A_1 = 1 minute 15.06
seconds, A_2 = 11 minutes 25.03 seconds, ... in succession,
the content B has the minus sign (-) assigned and is added
to the times A_1 , A_2 , ... in the ALU 13 as follows:

$$\begin{aligned} A_1 + (-B) &= 1 \text{ minute } 15.01 \text{ seconds} \\ A_2 + (-B) &= 11 \text{ minutes } 24.98 \text{ seconds} \end{aligned}$$

In this way, correct lap times are obtained in unit of
0.01 sec.

Since the lap operation can be executed by the interrupt
processing as in the foregoing cases of start and stop, it

is easily realizable merely by adding a subroutine for the lap operation to the ROM 4.

Further, two or more stop watch functions can be realized merely by adding subroutines to the ROM 4 and adding new
5 addresses for storing times to the RAM 9.

As described above in detail, according to this invention, while the time base remains long, for example, at 0.1 sec, the timekeeping of the digit of 0.01 sec and the displaying of the result can be performed.

10 Various timing pulses necessary for executing instructions may be signals of comparatively low frequencies. As a result, charging and discharging currents for stray capacitances can be reduced to achieve lowering of the power dissipation, and a high frequency oscillator circuit can be dispensed with
15 to achieve simplification of the whole circuit.

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CLAIMS

1. A multi-function electronic digital watch of the dynamic logic type including: timing means which generates a time base signal; count means to receive a timing signal shorter in period than
5 the time base signal; indication input means; temporary holding means to store an output of said count means upon an indication of said input means; first memory means in which a series of control instructions are written; arithmetic means which
10 is controlled by the control instructions and which executes predetermined operations; second memory means which stores a time signal having a plurality of digits therein; control means coupled to said first and second memory means and to said timing
15 means for sequentially reading out the control instructions of the first memory means, said control instructions being provided to renew a time signal of a less significant digit stored in the second memory means at each occurrence of the time base
20 signal, and to renew a time signal of a more significant digit stored in the second memory means when a signal for renewing the more significant digit has been generated and to deliver a time signal of a least significant digit determined by the period
25 of said timing signal shorter in period than the time base signal on the basis of an output of said holding means and the time signals stored in said second memory; and output means to deliver a signal including the time signal of the least significant
30 digit.



2. A digital watch according to Claim 1, wherein said time base signal is generated on the basis of said output of said count means.
3. A digital watch according to Claim 1 or 2,
5 wherein said output means comprises display means to display said signal including the time signal of the least significant digit.
4. A digital watch according to any one of the preceding claims, wherein said first and second memory
10 means are respectively constructed of a ROM and a RAM.
5. A multi-function electronic digital watch of the dynamic logic type, constructed and arranged to operate substantially as herein described with reference to and as illustrated in the accompanying
15 drawings.

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