FILM CARRIER TAPE

TECHNICAL FILED

The invention relates to a film carrier tape and particularly to Chip Size/Scale Package (CSP) fabrication technology and mounting technology for CSP.

BACKGROUND ART

There is no formal definition of Chip Size/Scale Package (hereinafter called CSP), but generally this refers to a semiconductor package (IC package) in which the package size is the same as or only very slightly larger than the chip size. The development of CSP technology is very important for promoting high-density mounting.

One prior art publication relating to CSP is International Publication WO95/08856. In this publication, the method is adopted in which a lead frame is mounted on a lead frame support (special-purpose jig), and the leads are cut respectively (one by one) by a special tool, while at the same time the severed leads are bent downward, and are connected to bonding pads of the IC chip.

With this method, a special jig or equipment is required, and additionally leads may easily be made bent during the bonding to the IC chip by the cutting of the leads.

The object of the invention is use, as far as possible, prior production lines and existing technology, reducing the burden of equipment and the burden of developing special technology, reducing the occurrence of bent leads during the making process, and making a chip-size package with high reliability, while increasing the yield.

DISCLOSURE OF INVENTION

According to the invention, as far as possible a prior TAB (Tape Automated Bonding) production line and existing technology are used, reducing the burden of equipment and the development burden of special technology.

The film carrier tape of the invention comprises:

an insulating film having a lead hole formed therein;

a lead on the insulating film, the lead having one end which extends into an area of the lead hole to be a free end; and

a marking for bending detection of the lead formed on the insulating film and positioned on an extended line from the free end.

A pad portion for forming an external connection terminal may be formed at another end of the lead.

The film carrier tape of the invention is obtained by:

making an insulating film having a lead hole formed therein;

forming a conductor pattern on the insulating film having a plurality of leads for connection to a semiconductor chip, a link portion linking together the plurality of leads and provided within a mounting area of the semiconductor chip, and a frame electrically connected to all of the leads through the link portion; and

forming a hole in the link portion of the conductor pattern.

The film carrier tape of the invention comprises:

an insulating film;

a plurality of leads formed in parallel on the insulating film;

a pair of leads positioned adjacent to the plurality of leads, separated by a predetermined distance, and mutually connected together; and

another lead formed between the pair of leads.

BRIEF DESCRPTION OF DRAWINGS

Fig. 1 is a cross-sectional view of a film carrier tape, showing the first step in the method of making a semiconductor device of the invention; Fig. 2 is a cross-sectional view of a film carrier tape, showing the second step in the method of making a semiconductor device of the invention; Fig. 3 is a

cross-sectional view of a film carrier tape, showing the third step in the method of making a semiconductor device of the invention; Fig. 4 is a cross-sectional view of a film carrier tape, showing the fourth step in the method of making a semiconductor device of the invention; Fig. 5 is a cross-sectional view of a film carrier tape, showing the fifth step in the method of making a semiconductor device of the invention; Fig. 6 is a cross-sectional view of a film carrier tape, showing the sixth step in the method of making a semiconductor device of the invention; Fig. 7 is a cross-sectional view of a film carrier tape, showing the seventh step in the method of making a semiconductor device of the invention; Fig. 8 is a cross-sectional view of a film carrier tape, showing the eighth step in the method of making a semiconductor device of the invention; Fig. 9 is a cross-sectional view of a film carrier tape, showing the ninth step in the method of making a semiconductor device of the invention; Fig. 10 is a cross-sectional view of a film carrier tape and semiconductor chip, showing the ninth step in the method of making a semiconductor device of the invention; Fig. 11 is a cross-sectional view of a film carrier tape and semiconductor chip, showing the tenth step in the method of making a semiconductor device of the invention; Fig. 12 is a cross-sectional view of a film carrier tape and semiconductor chip, showing the eleventh step in the method of making a semiconductor device of the invention; Fig. 13 is a cross-sectional view of a device showing a variant example of the semiconductor device of the invention; Fig. 14 is a plan view of the film carrier tape in the step of Fig. 2; Fig. 15

is a plan view of the film carrier tape in the step of Fig. 6; Fig. 16 is a plan view of the film carrier tape in the step of Fig. 10; Fig. 17 is a plan view of the film carrier tape in the step of Fig. 11; Fig. 18 is a plan view of an individualized semiconductor device of the invention; Fig. 19 is an explanatory diagram showing characteristics of the method of making a film carrier tape (method of making a semiconductor device) of the invention; Fig. 20 is an explanatory diagram showing other characteristics of the method of making a film carrier tape (method of making a semiconductor device) of the invention; Figs. 21A to 21D are explanatory diagrams showing yet further characteristics of the method of making a film carrier tape (method of making a semiconductor device) of the invention; Fig. 22 is a diagram showing a variant example of the method of making a film carrier tape (method of making a semiconductor device) of the invention; Fig. 23 is a cross-sectional view of the mounted board of the invention; and Fig. 24 is a diagram showing the interior of the electronic device of the invention.

The embodiments pertaining to the invention are now described with reference to the drawings.

(1) First Embodiment

In this embodiment, TAB (Tape Automated Bonding) technology is used in implementing the fabrication of a chip-sized semiconductor device. In the process of this embodiment, as far as possible an existing TAB production line and existing technology are used, reducing the burden of equipment and the

development burden of special technology, and fabricating a chip-size package with high reliability, while increasing the yield.

(Principal Characteristics of the Embodiment)

Before discussing the embodiment, principal characteristics thereof are described with reference to Figs. 19 to 21D.

(a) As shown in Fig. 19, on a polyimide film 10 in which are provided certain openings (lead holes 40a to 40c, a resin injection hole 42, and so forth), is provided a conducting material being copper or the like, in the form of foil, and a conductor pattern is formed therein by for example etching. This conductor pattern may be formed on the front or reverse side of the polyimide film. It is also possible for the conductor pattern to be formed on both sides. In this case, although not shown in the drawings, through holes may be formed in the polyimide film and may be used to provide electrical conduction between both sides.

This conductor pattern comprises frames 59a, 59b and 59c, leads (54a to 54x, 54y, and so forth), pads 55 having unitary or integral electrically conducting projections, a plurality of link portions (57a to 57x, 57y, and so forth) linking each lead (and each pad) mutually, and suspension leads (TR1 to TR3, and so forth) electrically connecting the frame and a group of leads.

It should be noted that it is not essential that the pads are formed with electrically conducting projections, and according to requirements projections may equally be formed on the mounting side, that is, on a motherboard, for example.

Even in the case that the pads are formed with electrically conducting projections, they may without restriction be formed in advance when the tape is formed, or at a later stage, for example during the formation of the package or after that.

The extremities of the leads (54a to 54x, 54y, and so forth) which connect to the IC chip are termed "fingers". Each finger is a free end, terminating over a lead hole (40a to 40c) (that is within the lead hole). In other words, a finger positioned within the lead hole is already terminated when the pattern is formed, and undergoes no further process until the final connection (bonding) to the bonding pads of the IC chip. Even during the bonding to the bonding pads of the IC chip, since the finger is a free end, there is no necessity of cutting, and as a result, finger bending due to the stress of cutting does not occur. For this reason, the accurate positioning and bonding of the leads to the IC chip is possible.

However, in order to carry out electroplating in a single operation on all of the plurality of leads (54a and so forth) which are formed on the insulating film of polyimide or the like, it is necessary for all of the leads to be electrically connected to the frame (59a, 59b, and 59c). Here, in this embodiment, a plurality of link portions (57a to 57x, 57y, and so forth) are disposed within the area of mounting the semiconductor chip, and link a number of leads within the area of mounting the semiconductor chip, and through the link portions (57a to 57x, 57y, and so forth) electrical connections to the frame 59a, 59b and 59c are made. By this means, by connecting the frame 59a, 59b and 59c to one pole of a

battery 800, electroplating of the conductor pattern including the leads (54a and so forth) can be carried out in a single operation. It should be noted that the "area of mounting the semiconductor chip" and the "mounting area of a single IC chip" both correspond substantially to the CSP end 700 outlined by a dot-dash line in Fig. 19.

Some of the link portions (57a to 57x, 57y, and so forth) which are no longer needed are cut away by die-stamping-out, together with the insulating film, so that the leads (54a to 54x, 54y, and so forth) are electrically isolated. This die-stamping can be carried out in a single operation, and does not complicate the fabrication process. Although involving a complication of the process, the insulating film portion does not necessarily have to be cut out, and it is sufficient at least to cut out the lead portions to provide electrical isolation of each lead. The link portions (57a to 57x, 57y, and so forth) are disposed within the mounting area of a single IC chip, and are therefore away from the extremities (fingers) of the leads positioned at the boundary of the chip mounting area. As a result, the cutting of the link portions (57a to 57x, 57y, and so forth) has no effect on the lead extremities (fingers).

Besides, in this embodiment, a plurality of the link portions 57a and so forth are provided, but by making this number as small as possible, the die-stamping operation can be made simpler.

It should be noted that the holes formed by die-stamping out the link portions 57a and so forth can be used as injection holes for epoxy resin or the like (see Fig. 12), and in

particular, if a hole is positioned in the center when seen in plan view, the epoxy resin can be injected efficiently.

Furthermore, when the strength of the polyimide film 10 is considered, it is preferable for the positions of the plurality of link portions 57a to be dispersed. In this case, the holes formed by die-stamping out the link portion 57a can be used as an air escape hole when the epoxy resin is injected, or as a steam escape hole in the completed semiconductor device.

In this way, without making the fabrication process complicated, lead bending is prevented, and reliable bonding is made possible. Besides, electroplating can be carried out in a single operation.

Although in Fig. 19 only a part of the circuit pattern is shown, in practice the circuit pattern is formed continuously over the film.

(b) This embodiment aims to use conventional TAB technology, and to exploit an existing production line and existing technology. Specifically, as shown in Fig. 20, the insulating film 10 in the mounting area of a single IC chip is supported by support bars 800a, 800b, 800c, and 800d, and unites with other parts of the insulating film. Therefore, continuous process in a single operation is possible for each insulating film as a processing unit. It should be noted that in Fig. 20 four support bars 800a to 800d are provided, but it is sufficient for at least two support bars to be provided. It is preferable for the two support bars to be disposed in opposing positions, for example from two parallel sides.

However, in the case of a conventional film carrier tape

there is no marking with respect to the bending of the extremities (fingers) of the lead 54a, and for this reason in this embodiment markings for bending detection of leads (as a concrete example, dummy leads) are additionally provided. That is to say, dummy leads (52a and so forth) are provided, serving as a standard for determining finger bending.

The dummy leads (52a and so forth) are provided on the extended lines of the fingers. In this way, finger bending can be detected, and it is made possible to separate faulty products. In particular, the dummy lead 52a in Fig. 20 has a finely point end, making detection of the bending of the leads 54a easy, and allowing the number of steps required for inspection to be reduced. However, even without the end made finely pointed, the dummy lead 52a can be used for the detection of finger bending.

It is preferable for the dummy leads (52a and so forth) to be formed at the same time as the conductor pattern is formed. However, without limitation to this, the dummy leads may equally be formed separately, using a different material, such as for example solder resist. It should be noted that in this case the dummy leads are formed using well-known technology.

It should be noted that in the above-mentioned "dummy lead" is an example of a marking for lead bending detection, and another marking may be used. For example, by forming slits by die- stamping out the insulating film at particular positions, these slits may be used as markings for bending detection.

(c) In principle, in the invention the extremities

(fingers) of the leads are terminated and left as free ends.

However, as shown in Figs. 21A to 21D, in order to correspond to the positions of the bonding pads of the IC chip, for example it may be necessary for a plurality of the extremities (fingers) of the leads to be disposed on a single line. For example, as shown in Fig. 21A, bonding pads 240c and 240d of the IC chip (CP) are on the same line.

In such a case, it is necessary for the leads 54 to be in a radiating pattern as shown in Fig. 21B, or to be bent as shown in Fig. 21C.

However, a radiating pattern of leads does not fit an orthogonal coordinate system, and causes problems in the fabrication of the film carrier tape, and if the ends of the leads are bent free ends, unnecessary moment due to gravity works, and the twisting of leads tends to occur.

In such a case, the lead shape shown in Fig. 21D is adopted. That is to say, a lead LR2 is provided encircling another lead LR1. This lead LR2 comprises lead portions A, B and C extending in the direction which fits an orthogonal coordinate system. In other words, the lead LR2 is not a free end, but is in the "U shape".

The Y portion of the lead LR1 is connected to bonding pad 240d of the IC chip (CP) in Fig. 21A, and the x portion of the lead LR2 is connected to bonding pad 240c. In other words, the point of contact (point x) with the IC chip is supported by two lead portions (A, C). By this means, no twisting moment acts. The shape of the lead LR2 is preferably bilaterally symmetrical, in order to maintain the lateral balance.

(Example of The Method of Making a Semiconductor Device)

Next an example of the method of making a semiconductor device pertaining to the embodiment is described, with reference to Figs. 1 to 12 (sectional views) and Figs. 14 to 18 (plan views). Fig. 14 corresponds to Fig. 2, Fig. 15 corresponds to Fig. 5, Fig. 16 corresponds to Fig. 10, and Fig. 17 corresponds to Fig. 11. In particular, Figs. 1 to 10 show steps of forming a flexible substrate, Fig. 11 shows a bonding step, and Fig. 12 shows a step of injecting resin.

Step 1

As shown in Fig. 1, an insulating film (actually a polyimide film) 10 is provided, and on the reverse side of this insulating film 10 is applied an adhesive 12. It should be noted that as the insulating film, in place of a kind of polyimide may be used for example a kind of polyester or a kind of BT resin, or a kind of glass epoxy or another kind of film material. In any case, the insulating film is a flexible material. It should be noted that in the following description, polyimide film is used as an example for the insulating film.

Step 2

Using a desired means of making holes, for example, stamping-out by a press, laser process, or chemical etching process, as shown in Figs. 2 and 14, openings are selectively formed in the polyimide film 10, to provide via holes 30 (30a to 30x, and so forth), lead holes 40 (40a, 40b, and so forth), a resin injection hole 42, and resin stopping holes (44a and 44b). Here the lead holes 40a and 40b are formed of a size permitting insertion of a bonding tool 5000 as shown in Fig. 11.

It should be noted that the necessity of the via holes 30 is determined by the side of the polyimide film on which the wiring is formed. Also, the resin stopping holes (44a and 44b) are ancillary elements, and are not essential. The resin injection hole 42 may also be omitted by using for example the lead holes 40. However, when the speed of resin injection and the reliability of the injection are considered, the positive use of a resin injection hole 42 is preferable.

Step 3

As shown in Fig. 3, copper foil 50 is applied to the reverse side (the underside in this figure) of the polyimide film 10. If an adhesive is applied to the copper foil side, it is not necessary to apply an adhesive 12 to the polyimide film 10 in Step 1.

Step 4

As shown in Fig. 4, photoresist layers 60 and 62 are formed on both sides of the substrate including on the copper foil 50. In this figure, the front surface (the upper surface in the drawing) side is completely covered with photoresist, whereas on the reverse surface side, there are regions where the photoresist is not provided, in order to form a pattern.

Step 5

As shown in Fig. 5, the copper foil 50 is etched to form a particular conductor pattern, and then the photoresist layer 62 is removed. The plan view of this state is Fig. 15.

As shown in Fig. 15, the conductor pattern of for example copper comprises a frame 59a, 59b and 59c, leads (54a, 54b, LR1, LR2 and so forth), pad portions (55a to 55x and so forth) for forming electrically conducting projections, link portions

(57a to 57j), and dummy leads (52a, 52b and so forth). In Fig. 15, portions being the same as portions already described in Figs. 19, 20, and 21D are given the same reference numerals. In Fig. 15, the portion Q surrounded by a dotted line corresponds to Fig. 21D.

In this state, the various elements excluding the dummy leads (52a, 52b and so on), that is to say, the frame 59a, 59b and 59c, leads (54a, 54b, LR1, LR2 and so forth), pad portions (55a to 55x and so forth) for forming electrically conducting projections, and link portions (57a to 57j) all have electrical continuity.

Step 6

In order to make the extremities (the portions connecting to the IC chip, the fingers) of the leads 54a and so forth project, and to form bumps for connection (Fig. 8), first as shown in Fig. 6, photoresist layers 70, 72 and 74 are formed in particular positions on the conductor pattern on the reverse side. It should be noted that the lengths of the leads 54a, 54b, LR1 and LR2 are related to the positions of Al-electrodes 240a to 240d of an IC chip 200. Moreover, when as in this embodiment the leads 54a, 54b, LR1 and LR2 are formed on the side of the polyimide film 10 opposing the IC chip 200, they can be bonded to the Al-electrodes 240a to 240d without bending. As a result, since there is no necessity of considering a forming amount, the minimum length is sufficient. On the other hand, if the leads 54a, 54b, LR1 and LR2 are formed on the side of the polyimide film 10 opposite to the side facing the IC chip 200, it is necessary for them to be bent and bonded to the Al-electrodes 240a to 240d, and therefore it is

preferable for a forming amount to be considered, and for the leads to be lengthened.

Step 7

As shown in Fig. 7, on the reverse side, the conductor pattern is half-etched in the thickness direction.

Step 8

As shown in Fig. 8, the photoresist layers 60, 70, 72 and 74 are removed. As shown in the drawing, at the extremities (the portions connecting to the IC chip, the fingers) of the leads 54a and so forth are formed projections 56a. These projections 56a are connected to the Al-electrodes of the semiconductor chip in a subsequent bonding step.

It should be noted that at this time, portions other than the fingers may also have projections 56b formed appropriately. For example, the projections 56b may be used to form a gap between the conductor pattern and the IC chip for filling the resin.

It should be noted that in the TAB step, in some cases for connection of the TAB leads and the semiconductor chip, metallic bumps (projections) may be formed on the semiconductor chip. In this case, the bumps are formed on the electrodes on the semiconductor chip. The material used is normally gold or solder or the like. Besides, in this case the projections 56a are not required on the lead 54a sides. Therefore, in this case the steps in Figs. 6 to 8 are not required.

On the other hand, this embodiment is described as an example in which, in place of forming bumps on the semiconductor chip, bumps (projections) are formed on the TAB lead sides. The technology for forming these lead extremities is an

established technology already developed by the present applicant, and allows an existing TAB production line to be used. Besides, in this case, the aluminum pads on the semiconductor chip side may simply be exposed, and the process can be simplified since the metallic bumps are not required.

Step 9

As shown in Fig. 9, after photoresist layers 80a and 80b are formed on the surface of the conductor pattern, electroplating is applied to the surface of the conductor pattern, and plating layers (90a to 90b) made of Ni/Au are formed. The nickel (Ni) functions as a barrier metal. This electroplating, as also described in Fig. 19, is carried out by applying a voltage to the frame 59a, 59b and 59c. For example, one electrode (generally the anode) is connected to the frame to allow a unified operation.

It should be noted that this is not restricted to electroplating. For example, electroless plating may be used to carry out the plating of the pattern. After the plating process is completed, the photoresist layers 80a and 80b are removed.

Step 10

First, as shown in Fig. 16, die-stamping of the link portions 57a to 57j is carried out. The die-stamping operation should preferably be carried out in a single operation when operating efficiency is considered, but may equally be split into a number of separate operations. By this means, the leads 54a are electrically isolated.

Next, as shown in Fig. 10, the via holes 30 are filled with a metal (nickel or the like) 98, and next external

connection terminals (solder balls) 100 are formed. It should be noted that to obtain height precision a metal other than solder, such as aluminum is inserted in the via holes, but to reduce the number of steps in the fabrication process the via holes may be filled with solder and used in that state for forming the external connection terminals, thus allowing single-operation (integral) forming. By this, the film carrier tape for the CSP is completed (Fig. 16).

It should be noted that if electroless plating is used, the die-stamping need not be carried out.

At this stage, using the marking for lead bending detection such as the dummy leads as a reference, inspection for bent fingers is carried out to select bad and good items.

Besides, in this embodiment, the step of forming the external connection terminals is carried out within the process of forming the flexible substrate, but this is not limiting. For example, there is a possibility of formation at any time after the bonding with the semiconductor chip. Besides, at this time, portions inside the via holes only may be formed beforehand in the process of forming the flexible substrate, and in a separate later step the external connection terminals (solder balls) 100 may be formed. These selections may be made as a matter of convenience. In particular, in the case that solder is used for the external connection terminals, when the effect of heat from the tool during bonding is considered, it is preferable to form the external connection terminals after the bonding.

Step 11

Next, as shown in Figs. 11 and 17, the Al-electrodes

(bonding pads) 204 (204a to 240d and so forth) of the IC chip 200 are connected (bonded) to the extremity of each lead. This connection is carried out by applying heat and pressure from the bonding tool 5000 to the projections 56a, to create a Au/Al alloy. In Fig. 17, a heavy line indicates the IC chip 200. It should be noted that the free ends of the pattern are positioned within the area of the semiconductor chip.

Step 12

Next, an epoxy resin is injected. For example, as shown in Fig. 12, this is injected through a resin injection hole (reference numeral 42 in Fig. 17). It should be noted that in place of the resin injection hole, for example the lead holes 40 can be used for resin injection, so that the provision of the resin injection hole is not necessarily essential. However, when the speed of resin injection and the reliability of the injection are considered, the result obtained is that the use thereof is preferable.

The resin covers the whole of the surface of the IC chip on which the Al-electrodes are formed (the active surface). In particular, the portion of connection of the IC chip 200 and the leads (54a and so forth) is completely covered. On the other hand, if the resin stopping holes 44a and 44b are provided, by their existence they restrict the lateral spread. In Fig. 12, reference numerals 300a, 300b and 300c indicate a resin coating layer. As a result of positioning the finger extremities within the area of the semiconductor chip, the lateral surfaces of the extremities are also sealed by the resin 300a. Besides, the sides of the fingers on which the projections 56 are not provided are also filled with resin,

and it is possible for the whole finger to be immersed in resin. However, in this case, it is necessary for the highest position of the resin to be set to be a position lower than the outer surface of the polyimide film 10. If this is not done, the connection of the external connection terminals 100 is impaired.

Next the injected resin is hardened by heat. At this time, the holes formed in the polyimide film 10 when the link portions (57a to 57j) were die-stamped out in Step 10, for example, act as gas escape holes for steam and the like generated by heating the package, and assist in improving the reliability of the package. Besides, it is also possible to use some of the holes formed when the link portions (57a to 57j) were die-stamped for resin injection. It is not, however, preferable that the holes are all used simultaneously as holes for resin injection.

By means of the above steps, a tape carrier semiconductor device assembly is fabricated, having a plurality of IC chips connected.

It should be noted that in the example above, after the external connection terminals 100 are formed as shown in Fig. 10, through the steps in Figs. 11 and 12 the tape carrier semiconductor device assembly is fabricated, but this is not limitative.

As partially already noted above, for example, the external connection terminals 100 may be formed after the resin sealing step of Fig. 12. In this case, if the external connection terminals are formed after the IC chip 200 and the connection portions between the leads 54a and the IC chip 200

are covered by resin, there is no danger of contaminating the chip area when the external connection terminals are formed, and therefore there is the advantage that the reliability can be improved.

Step 13

The polyimide film 10 is die-stamped out along the CSP end 700 shown surrounded by a dot-dash line in Fig. 17. By this means a chip-size semiconductor device (CSP) 1000 as shown in Fig. 18 is completed. In Fig. 18, the hatched area is the area covered by resin.

As shown in the drawings, only the cut surfaces of the suspension leads TR1 and TR2 are exposed, and the damp resistance is excellent. Also because it takes the form of a package, burn-in and other testing is possible.

It should be noted that in the above example the conductor pattern is formed on the reverse side of the insulating film 10, but this is not limitative, and application is also possible when formed on the front side of the insulating film 10, and moreover a similar benefit is obtained.

(2) Second Embodiment

As shown in Fig. 13, not only in the interior of the IC chip 200, but external connection terminals (solder balls) 100b may also be formed on the exterior.

In this embodiment, the IC chip 200 is disposed within a concavity of a can container 300, and leads 50 extend over the can container 300. Then metal electrodes 98b are formed within the via holes, and solder balls 100b are connected to these metal electrodes 98b.

According to this embodiment, with no restrictions from

the size of the IC chip 200, the number of external connection terminals (solder balls) can be freely increased.

(3) Third Embodiment

When the demands of package size are relatively soft, as shown in Fig. 22, the method of fabrication can be adopted in which after the connection (bonding) of the IC chip 200 and the leads 54 is completed, die-stamping is carried out on the outside of the connection points with the chip (in Fig. 22, die-stamping at the CSP end 900 shown by a double-dot-dash line), and the leads 54 are cut away from the frame 59.

By means of this method of manufacture, since the leads are cut away from the frame in the last step of the process, there is no danger of bonding defects due to lead bend.

(4) Fourth Embodiment

Fig. 23 shows a state in which a chip-size semiconductor device (CSP) 1000 is mounted on a printed wiring board 2000.

The external connection terminals (solder balls) 100a and 100b of the chip-size semiconductor device (CSP) 1000 are connected to a conductor pattern 2100a and 2100b on the printed wiring board 2000 (mounting substrate). Since the package size is chip size, an extremely high mounting density is possible. It should be noted that in Fig. 23, reference numeral 202 indicates another IC mounted on the printed wiring board 2000.

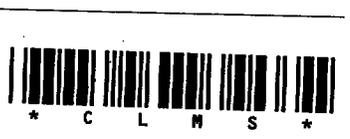
(5) Fifth Embodiment

Fig. 24 is a view showing the interior of a camera integrated VTR incorporating mounting substrates with chip-size semiconductor devices (CSP) mounted thereon of the invention.

The camera integrated VTR 3000 incorporates two mounting substrates 2000a and 2000b, and on each of the mounting substrates are mounted CSPs 1000 and 1002 of the invention.

In Fig. 24, reference numeral 3100 indicates a lens, reference numeral 3200 indicates a lens unit, reference numeral 3300 indicates a battery box, and reference numeral 3310 indicates a battery.

In this way, since the semiconductor device (CSP) of the invention is chip size, it can be applied to a camera integrated VTR and other portable instruments in which compact and lightweight design is of the essence. Furthermore, the semiconductor device (CSP) of the invention has high reliability in respect of its resistance to moisture and resistance to heat, and this leads to the improvement of the reliability of an electronic instrument.



CLAIMS:

1. A film carrier tape comprising:

an insulating film having a lead hole formed therein;

a lead on the insulating film, the lead having one end which extends into an area of the lead hole to be a free end; and

a marking for bending detection of the lead formed on the insulating film and positioned on an extended line from the free end.

2. The film carrier tape of claim 1, wherein a pad portion for forming an external connection terminal is formed at another end of the lead.

3. A film carrier tape obtained by:

making an insulating film having a lead hole formed therein;

forming a conductor pattern on the insulating film having a plurality of leads for connection to a semiconductor chip, a link portion linking together the plurality of leads and provided within a mounting area of the semiconductor chip, and a frame electrically connected to all of the leads through the link portion; and

forming a hole in the link portion of the conductor pattern.

4. A film carrier tape comprising:

an insulating film;

a plurality of leads formed in parallel on the insulating film;

a pair of leads positioned adjacent to the plurality of leads, separated by a predetermined distance, and mutually connected together, and

another lead formed between the pair of leads.