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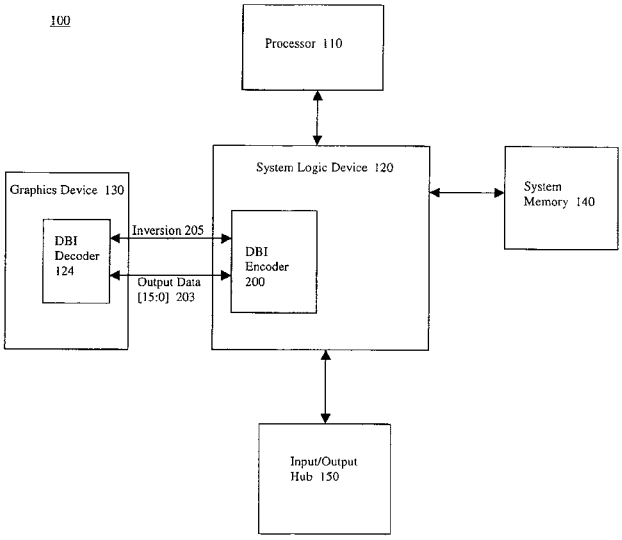
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(54) Title: METHOD AND APPARATUS FOR REDUCING SIMULTANEOUS SWITCHING OUTPUT NOISE USING DYNAMIC BUS INVERSION



(57) Abstract: An embodiment of a computer system implementing dynamic bus inversion includes a first system logic device having a dynamic bus inversion encoder and also includes a second system logic device having a dynamic bus inversion decoder. The first and second system logic devices are coupled via a data bus. The encoder compares a group of data bits currently placed on the data bus with a next group of data bits to be placed on the data bus. If the encoder determines that greater than a predetermined number of bit transitions would occur between the current and next group of data bits, the encoder inverts the next group of data bits before placing the next group of data bits onto the data bus. The encoder also asserts an inversion signal that is received by the decoder. In response to the assertion of the inversion signal, the decoder inverts the previously inverted next group of data bits to restore the original data.

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