

SPECIFICATION

Solid-state switching device

This invention relates to solid-state devices and in particular to switching devices.

In an article entitled "A Field Terminated Diode" by Douglas E. Houston et al, published in *IEEE Transactions on Electron Devices*, Vol. ED-23, No. 8, August 1976, there is described a discrete solid-state high voltage switch that has a vertical geometry and which includes a region which can be pinched off to provide an "OFF" state or which can be made highly conductive with dual carrier injection to provide an "ON" state. "Dual carrier injection" refers to the injection of both holes and electrons to form a conductive plasma in the semiconductor. One problem with this switch is that it is not easily manufacturable with other like switching devices on a common substrate. Another problem is that the spacing between the grids and the cathode should be small to limit the magnitude of the control grid voltage; however, this limits the useful voltage range because it reduces grid-to-cathode breakdown voltage. This limitation in turn limits to relatively low operating voltages the use of two devices connected in antiparallel; i.e. with the cathode of each coupled to the anode of the other. Such a circuit would be useful as a high voltage bidirectional solid-state switch. An additional problem is that the base region should ideally be highly doped to avoid punch-through from the anode to the grid; however, this leads to a low voltage breakdown between anode and cathode. Widening of the base region limits the punch-through effect; however, it also increases the resistance of the device in the "ON" state.

It is desirable to have a solid-state switch which is easily integratable such that two or more switches can be simultaneously fabricated on a common substrate and wherein each switch is capable of bilateral blocking of relatively high voltages.

According to the present invention there is provided a solid-state switching device comprising: a semiconductor body having a bulk portion of a first conductivity type and having first and second mutually opposed major surfaces; a first region of the first conductivity type; a second region of a second conductivity type opposite to the first conductivity type; and a gate region of the second conductivity type; the first, second and gate regions being mutually disjoint regions within the body and having resistivities lower than the resistivity of the bulk portion; the first and second regions being at the first major surface and the gate region being at the second major surface; there being no substantial recess in the first major surface laterally separating the first and second regions; whereby in operation by application of a suitable potential to the gate region current flow between the first and the second regions can be substantially interrupted and inhibited and with a different suitable potential applied to the gate region current flow between the first and second

regions can be established, the said current flow being facilitated by injection of majority carriers into the bulk portion from the first region and injection of minority carriers into the bulk portion from the second region.

Switches according to the invention, which are to be denoted as gated diode switches (GDSs), can be made which are capable of blocking relatively large potential differences between anode and cathode in the OFF state, independent of polarity, and are capable of conducting relatively large currents with a relatively low voltage drop between anode and cathode in the ON state.

The bilateral blocking characteristic of these GDS structures makes them particularly useful in many applications. Two of the above-described GDSs can be coupled together with the gates being common and the cathode of each coupled to the anode of the other. This combination forms a bidirectional high voltage switch. Arrays of the GDSs can be fabricated on a common semiconductor wafer to form crosspoints, or two GDSs can be fabricated with a common gate to form a bidirectional switch.

Some embodiments of the invention will now be described by way of example with reference to the accompanying drawings of which:—

FIG. 1 illustrates a switch in accordance with the invention;

FIG. 2 illustrates a proposed electrical symbol for the switch of FIG. 1;

FIG. 3 illustrates a top view of another switch in accordance with the invention; and

FIGS. 4 to 7 illustrate various other switches in accordance with the invention.

Referring now to FIG. 1, there is illustrated a semiconductor structure 10 comprising two essentially identical gated diode switches GDS1 and GDS2 which are illustrated within dashed line rectangles and are both formed in a semiconductor wafer or substrate 12. Semiconductor structure 10 has a major surface 11. Substrate 12 is of the one conductivity type and acts as a common gate and support for GDS1 and GDS2.

An epitaxial layer of the opposite conductivity type to substrate 12 is partitioned by semiconductor regions 20 into mutually isolated semiconductor bodies 16 and 16a. Many bodies similar to 16 and 16a can be formed on substrate 12 in addition to the two illustrated. Regions 20 are of the same conductivity type as substrate 12 but have a higher impurity concentration and extend from major surface 11 down to substrate 12. Within body 16 is also included a semiconductor anode region 18 of the same conductivity type as body 16 but of higher impurity concentration. A semiconductor region 22 is of the same conductivity type as body 16 but of lower resistivity than body 16. A semiconductor cathode region 24 is included in a portion of region 22 and has a portion which extends to major surface 11. Region 24 is of the same conductivity type and essentially the same

impurity concentration as regions 20. Electrodes 28, 32 and 30 make low resistance contact to regions 18, 24 and 20, respectively. Region 20 makes low resistance contact to substrate 12.

Thus, electrode 30 makes low resistance contact to substrate 12 and serves as a common gate electrode for GDS1 and GDS2. An electrode 38 of a metal or semiconductor material, is located between anode electrode 28 and cathode electrode 32. Electrode 38 is electrically coupled to the substrate by an electrical connection to electrode 30.

Body 16a has contained therein semiconductor regions 18a, 22a, and 24a. Electrodes 28a, 32a, and 30 are coupled to regions 18a, 22a, and 24a, respectively. These regions are essentially the same as the corresponding regions of body 16. An insulator layer 26 electrically isolates all of the above-described electrodes from portions of structure 10, except those portions which are meant to be electrically contacted.

In one illustrative embodiment, substrate 12 is of *n* type conductivity, regions 20 and 24 (24a) are of *n*+ type conductivity, body 16 (16a) is of *p*-type conductivity, region 18 (18a) is of *p*+ type conductivity, region 22 (22a) is of *p* type conductivity and of lower resistivity than body 16 (16a), and electrodes 28 (28a), 32 (32a), and 30 are aluminum. In this embodiment anode electrode 28 is electrically coupled to cathode electrode 32a, and cathode electrode 32 is coupled to anode electrode 28a.

Proposed electrical symbols for GDS1 and GDS2 are illustrated in FIG. 2. The anode, cathode, and gate electrode terminals of GDS1 are 28, 32 and 30, respectively. The corresponding terminals of GDS2 are 28a, 32a, and 30. This combination of GDS1 and GDS2 acts as a bidirectional switch which is capable of bilateral blocking of potentials independent of whether the anode or cathode of either gated diode switch is at the more positive potential.

GDS1 and GDS2 are both essentially identical and operate in essentially the same manner.

Accordingly, the below description of GDS1 is equally applicable to GDS2. GDS2 has relatively low resistance path between anode region 18 and cathode region 24 when in the ON (conducting) state and by a substantially higher impedance when in the OFF (blocking) state. In the ON state the potential of the gate electrode 30 is typically at or below that of the anode 28. Holes are injected into body 16 from anode region 18 and electrons are injected into body 16 from cathode region 24. These holes and electrons can be in sufficient numbers to form a plasma which increases the conductivity of body 16 so that the resistance between anode region 18 and cathode region 24 is relatively low when GDS1 is operating in the ON state. This type of operation, in which both holes and electrons act as current carriers, is called dual carrier injection.

Region 22 helps limit the punch-through of a depletion layer formed during operation between region 20 and substrate 12 and cathode region

24. Region 22 also helps inhibit formation of a surface inversion layer between regions 24 and 20. In addition, it allows anode region 18 and cathode region 24 to be relatively closely spaced. This results in relatively low resistance between anode region 18 and cathode region 24 during the ON state.

Conduction between anode region 18 and cathode region 24 is inhibited or cut off if the potential of gate electrode 30 is sufficiently more positive than that of anode electrode 28 and cathode electrode 32. The amount of excess positive potential needed to inhibit or cut off conduction depends on the geometry and impurity concentration levels of structure 10. This positive gate potential causes the portion of body 16 between gate region 12 and a portion of oxide layer 26 to be depleted so that the potential of this portion of body 16 is more positive than that of the anode 18 and cathode 24 regions. This positive potential barrier inhibits the conduction of holes from anode region 18 to cathode region 24. It also serves to collect electrons emitted at cathode region 24 before they can reach anode region 18. This essentially pinches off body 16 against dielectric layer 26 in the bulk portion thereof which is between the anode and cathode regions (18, 24) and extends from region 12 to dielectric layer 26.

The electrode 38 reduces the magnitude of the potential needed to inhibit or cut off conduction. In the OFF state GDS1 is capable of bilateral blocking of relatively large potentials between anode and cathode regions, independent of which region is at the more positive potential.

During the ON state of GDS1, the *p-n* junction diode comprising body 16 and region 20 becomes forward-biased. Current limiting means (not illustrated) may be used to limit the conduction through the forward-biased diode.

GDS1 and GDS2 need not have the anodes and cathodes connected together. GDS1 or GDS2 can be used individually but the gates are common.

Referring now to FIG. 3, there is illustrated a top view of a dual GDS semiconductor structure 100 which has been fabricated. Structure 100 is similar to structure 10 except the anode and cathode regions are curved. This geometry tends to limit localized voltage field concentration which causes voltage breakdown and adds additional perimeter common to the anode and cathode regions in order to facilitate low ON resistance and thereby facilitate high current operation. Structure 100 has been fabricated on an *n* type substrate having a thickness of 457 to 559 microns and an impurity concentration 10^{15} to 10^{16} impurities/cm³. Bodies 160 and 160a are of *p*-type conductivity with a thickness of 30 to 40 microns, a width of 720 microns, a length of 910 microns, and an impurity concentration in the range of 5×10^{13} to 9×10^{13} impurities/cm³. Curved anode regions 180 and 180a are of *p*+ type conductivity with a thickness of 2 to 4 microns, and an impurity concentration of 10^{19} impurities/cm³. Curved cathode regions 240 and

240a are of n+ type conductivity with a thickness of 2 to 4 microns, and an impurity concentration of 10^{19} impurities/cm³. The overall length and width of the fabricated circuit is 1910 microns by 1300 microns. The spacing between anode and cathode is 120 microns.

Some of the fabricated structures contained conductor regions 380, 380a which were 60 microns wide and others did not. The structures fabricated without regions 380, 380a required a potential of 22 more volts on the gate than the anode to inhibit or cut off conduction between anode and cathode. The structures fabricated with conductor regions 380, 380a required the gate potential to have an excess of only 7.5 volts over the anode potential to effect turnoff. The fabricated structure was able to block 300 volts and conduct 500 milliamperes with a voltage drop between anode and cathode of 2.2 volts. This structure was able to operate under current surges of 10 amperes for a duration of one millisecond.

Referring now to FIG. 4 there is illustrated a structure 1000 which is very similar to structure 10 and all components thereof which are essentially identical or similar to those of structure 10 are denoted by the same reference number with the addition of two "O"s at the end. This basic difference between structures 1000 and 10 is the elimination from structure 1000 of semiconductor regions 22, 22a of structure 10 of FIG. 1. Appropriate spacing of regions 2400, 2400a from region 2000 provides sufficient protection against depletion layer punch-through to regions 2400, 2400a and allows operation of structure 1000 as a high voltage switch.

Referring now to FIG. 5, there is illustrated a structure 10,000 which is very similar to solid-state structure 10 and all components thereof which are essentially identical to those of structure 10 are denoted by the same reference number with the addition of three "O"s at the end. The basic difference between structures 10,000 and 10 is the use of semiconductor guard ring regions 40, 40a encircling regions 24,000, 24,000a and being separated therefrom by portions of bodies 16,000, 16,000a. Guard ring regions 40, 40a provide the same type of protection against surface layer inversion as region 22, 22a of structure 10. Guard rings 40, 40a are of the same conductivity type as bodies 16,000, 16,000a but of lower resistivity. Guard rings 40, 40a can be extended (as is illustrated by the dashed lines) so as to contact cathode regions 24,000, 24,000a.

Referring now to FIG. 6, there is illustrated a structure 100,000 which is similar to structure 10. All portions of structure 100,000 which are similar or essentially identical to corresponding portions of structure 10 are denoted by the same reference number with the addition of four "O"s at the end. One difference between structure 100,000 and structure 10 is the use of semiconductor guard ring regions 400, 400a encircling cathode regions 240,000, 240,000a. Guard rings 400, 400a are similar to

semiconductor guard ring regions 40, 40a of structure 10,000. The dashed line portion of guard rings 400, 400a illustrates that they can be extended so as to contact cathodes 240,000, 240,000a. The combination of regions 220,000, 220,000a and guard rings 400, 400a provides protection against inversion of bodies 160,000, 160,000a, particularly between gate region 200,000 and cathode region 240,000, 240,000a, and provides protection against depletion layer punch-through to cathode region 240,000, 240,000a. This type of dual protection around cathode region 240,000, 240,000a is the preferred protection structure. Regions 220,000, 220,000a, and 400, 400a are all of the same conductivity type as bodies 160,000, 160,000a but of low resistivity. Regions 400, 400a have lower resistivity than regions 220,000, 220,000a. Another difference between structure 100,000 and structure 10 is semiconductor regions 70, 70a, which are of the same conductivity type as cathode regions 240,000, 240,000a. Regions 70, 70a are in electrical contact with electrodes 380,000, 380,000a and act as top gates. The use of gate regions 70, 70a results in a reduction in the magnitude of the potential necessary to cut off or inhibit conduction between anode regions 180,000, 180,000a and cathode regions 240,000, 240,000a.

Now referring to FIG. 7, there is illustrated a semiconductor structure 42 which comprises a plurality of essentially identical gated diode switches (GDSs) of which only two GDS3 and GDS4 (illustrated within dashed line rectangles), are shown. Semiconductor structure 42 comprises a semiconductor support member (substrate) 44 which is of a first conductivity type and has a major surface 46. Within a portion of substrate 44 are located separate regions 48 and 48a which are of the opposite conductivity type of substrate 44 and are separated from each other by portions of substrate 44 and by regions 50 which are of the same conductivity type as substrate 44 but of higher impurity concentration. Regions 50 are optional. Essentially identical semiconductor bodies 52 and 52a are contained within regions 48 and 48a, respectively.

Bodies 52 and 52a are of the same conductivity type as substrate 44. Within body 52 exists an anode region 54 which is of the same conductivity type as body 52 but of higher impurity concentration. Also within body 52 exists a region 56 which is of the same conductivity type as body 52 but of higher impurity concentration and which is separated from region 54 by portions of body 52. A cathode region 58 exists within a portion of region 56 and is separated from body 52 by portions of region 56. Cathode region 58 is of the same conductivity type as region 48. Electrodes 60, 62, 64 and 66 make low resistance contact to regions 48, 54, 58, and 50, respectively. If regions 50 are eliminated, electrode 66 makes contact to region 44 directly or through a low resistivity semiconductor region (not illustrated) like region 54, but contained in a portion of substrate 44. An

insulating layer 68, typically silicon dioxide, electrically isolates all of the electrodes of structure 42 from major surface 46 except in the regions in which it is desired to make low resistance contact.

Body 52a, regions 54a, 56a, and 58a and electrodes 60a, 62a, and 64a of GDS4 are essentially identical to the corresponding regions of GDS3.

Substrate 44 is typically held at the most negative potential available. This serves to reverse bias the p-n junctions formed by regions 48, 48a and substrate 44 such that all the GDSs contained within substrate 44 are junction isolated from each other.

GDS3 and GDS4 operate in essentially the same manner as described for the operation of GDS1 and GDS2 of FIG. 1. Region 48 serves as the gate, with regions 54 and 58 serving as anode and cathode, respectively. It is to be noted that gate regions 48 and 48a are physically and electrically separate and, accordingly, GDS3 and GDS4 can be operated essentially completely independently of each other since the respective gates, anodes, and cathodes are electrically separate. Thus, structure 42 facilitates the fabrication of an array of GDSs with each GDS being capable of being operated independently of all other GDSs of the array.

Various modifications of the embodiments described will now be apparent to a person skilled in the art to which this invention relates. For example, the impurity concentration levels, spacings between regions, and other dimensions of the regions can be adjusted to allow significantly higher operating voltages and currents than have been disclosed. A dielectric layer can be inserted between regions 48 and 48a and region 44 or said dielectric layer can be substituted for regions 44 and 50. Additionally other types of dielectric materials, such as silicon nitride, can be substituted for silicon dioxide.

CLAIMS

1. A solid-state switching device comprising: a semiconductor body having a bulk portion of a first conductivity type and having first and second mutually opposed major surfaces; a first region of the first conductivity type; a second region of a second conductivity type opposite to the first conductivity type; and a gate region of the second conductivity type; the first, second and gate regions being mutually disjoint regions within the body and having resistivities lower than the resistivity of the bulk portion; the first and second regions being at the first major surface and the

gate region being at the second major surface there being no substantial recess in the first major surface laterally separating the first and second regions; whereby in operation by application of a suitable potential to the gate region current flow between the first and second regions can be substantially interrupted and inhibited and with a different suitable potential applied to the gate region current flow between the first and second regions can be established, the said current flow being facilitated by injection of majority carriers into the bulk portion from the first region and injection of minority carriers into the bulk portion from the second region.

2. A device as claimed in claim 1, including a further region of the first conductivity type surrounding the second region, the further region having a resistivity intermediate between the resistivities of the first region and the bulk portion.

3. A device as claimed in claim 1 including an annular region of the first conductivity type at the first major surface laterally surrounding the second region, the annular region having a lower resistivity than the bulk portion.

4. A device as claimed in claim 2 including an annular region of the first conductivity type within the further region at the first major surface laterally surrounding the second region, the annular region having a lower resistivity than the further region.

5. A device as claimed in any of the preceding claims including a conductor connected to the gate region and overlying but not making electrical contact with a part of the bulk portion of the body at the first major surface which separates the first and second regions.

6. A device as claimed in any of the preceding claims wherein the semiconductor body is on a wafer substrate of the first conductivity type, the second major surface is the interface between the body and the substrate, and the gate region separates the bulk portion of the body from the substrate.

7. A bidirectional switching device comprising a pair of devices as claimed in any of the preceding claims sharing a common gate region, the first region of each device of the pair being connected to the second region of the other device of the pair.

8. A plurality of devices as claimed in claim 6 sharing a common substrate and including means for making electrical contact to the substrate.

9. A switching device substantially as herein described with reference to FIG. 1 or any of FIGS. 3 to 7 of the accompanying drawings.

insulating layer 68, typically silicon dioxide, electrically isolates all of the electrodes of structure 42 from major surface 46 except in the regions in which it is desired to make low resistance contact.

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GDS3 and GDS4 operate in essentially the same manner as described for the operation of GDS1 and GDS2 of FIG. 1. Region 48 serves as the gate, with regions 54 and 58 serving as anode and cathode, respectively. It is to be noted that gate regions 48 and 48a are physically and electrically separate and, accordingly, GDS3 and GDS4 can be operated essentially completely independently of each other since the respective gates, anodes, and cathodes are electrically separate. Thus, structure 42 facilitates the fabrication of an array of GDSs with each GDS being capable of being operated independently of all other GDSs of the array.

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gate region being at the second major surface there being no substantial recess in the first major surface laterally separating the first and second regions; whereby in operation by application of a suitable potential to the gate region current flow between the first and second regions can be substantially interrupted and inhibited and with a different suitable potential applied to the gate region current flow between the first and second regions can be established, the said current flow being facilitated by injection of majority carriers into the bulk portion from the first region and injection of minority carriers into the bulk portion from the second region.

2. A device as claimed in claim 1, including a further region of the first conductivity type surrounding the second region, the further region having a resistivity intermediate between the resistivities of the first region and the bulk portion.

3. A device as claimed in claim 1 including an annular region of the first conductivity type at the first major surface laterally surrounding the second region, the annular region having a lower resistivity than the bulk portion.

4. A device as claimed in claim 2 including an annular region of the first conductivity type within the further region at the first major surface laterally surrounding the second region, the annular region having a lower resistivity than the further region.

5. A device as claimed in any of the preceding claims including a conductor connected to the gate region and overlying but not making electrical contact with a part of the bulk portion of the body at the first major surface which separates the first and second regions.

6. A device as claimed in any of the preceding claims wherein the semiconductor body is on a wafer substrate of the first conductivity type, the second major surface is the interface between the body and the substrate, and the gate region separates the bulk portion of the body from the substrate.

7. A bidirectional switching device comprising a pair of devices as claimed in any of the preceding claims sharing a common gate region, the first region of each device of the pair being connected to the second region of the other device of the pair.

8. A plurality of devices as claimed in claim 6 sharing a common substrate and including means for making electrical contact to the substrate.

9. A switching device substantially as herein described with reference to FIG. 1 or any of FIGS. 3 to 7 of the accompanying drawings.

