Claims

1. A method of forming a multilayer structure, the method comprising:
forming a recess in a dielectric level;
forming a seed layer comprising tungsten and silicon in the recess; and
forming a tungsten fill over the seed layer, wherein a majority of the tungsten of the tungsten fill has a grain size having a longest dimension of at least 20 nm.

2. The method of claim 1, wherein an amount of the silicon in the seed layer is between about 4-28% by atomic weight of the seed layer.

3. The method of claim 1, wherein tungsten of the seed layer comprises both alpha and beta phase tungsten.

4. The method of claim 3, wherein the seed layer is about 10-60% beta phase tungsten by atomic weight.

5. The method of claim 1, wherein the seed layer contacts both the dielectric level and the tungsten fill in the recess.

6. The method of claim 1, wherein forming the seed layer comprises doping the tungsten with silicon to form a silicon-doped tungsten seed layer.

7. The method of claim 1, wherein forming the seed layer comprises depositing silicon and tungsten simultaneously.

8. The method of claim 1, wherein the majority of the tungsten in the tungsten fill is alpha phase tungsten and has a grain size between 30 and 50 nm.

9. The method of claim 8, wherein forming the seed layer comprises depositing tungsten by physical vapor deposition (PVD).

10. The method of claim 1, further comprising performing processing to deposit the tungsten fill at temperatures of 300° C. or greater, after deposition of the silicon-containing tungsten seed layer.

11. The method of claim 10, wherein the tungsten fill is deposited by chemical vapor deposition (CVD).

12. A multilayer structure, comprising:

a first dielectric level;

a second dielectric level disposed on the first dielectric level, the second dielectric level comprising recesses formed therein, at least some of the recesses extending to the first dielectric level;

a seed layer comprising tungsten and silicon disposed in the recesses and contacting both the first dielectric and the second dielectric level in the recesses; and

a tungsten fill disposed on the seed layer and filling the recesses in which the seed layer is present, the majority of the tungsten in the tungsten fill having a grain size with a maximum dimension of at least about 20 nm.

13. The multilayer structure of claim 12. wherein an amount of the silicon in the seed layer is between about 4-28% by atomic weight.

14. The multilayer structure of claim 13, wherein the tungsten of the seed layer comprises both alpha and beta phase tungsten, the seed layer containing about 10-60% beta phase tungsten by atomic weight.

15. The multilayer structure of claim 13, wherein the tungsten fill comprises at least about 40% alpha phase tungsten having a grain size with a maximum dimension between 30 nm and 50 nm.

16. The multilayer structure of claim 13, wherein a resistivity of the seed layer is higher than that of the alpha phase tungsten and a resistivity of a combination of the seed layer and the tungsten fill is less than that of alpha phase tungsten without the silicon-doped tungsten seed layer deposited under similar processing conditions.

17. The multilayer structure of claim 13, wherein a resistivity of the tungsten fill material is 2-4 f/sq for a recess of about 10-20 nm in width and between 50-100 nm in depth.

18. The multilayer structure of claim 13, wherein the first dielectric level is a nitride, the second dielectric level is an oxide, and the recesses terminate at the nitride.

19. A memory device, comprising:

an oxide level comprising recesses;

a silicon-containing tungsten seed layer disposed in the recesses; and

a tungsten fill material disposed in the recesses on the silicon-containing tungsten seed layer, an upper surface of the tungsten fill material in the recesses planar with an upper surface of the oxide level outside the recesses, the silicon-containing tungsten seed layer disposed between the tungsten fill material and the oxide level, the majority of the tungsten fill material having a grain size of about 30-50 nm.

20. The memory device of claim 19, wherein the recesses extend along a length of the memory device to form word lines or bit lines of the memory device, the recesses being between about 50-200 nm in depth and about 20 nm in width.

21. The memory device of claim 19, wherein:

an amount of the silicon in the silicon-containing tungsten seed layer is between about 4-28% by atomic weight.

22. The memory device of claim 19, wherein:

the silicon-containing tungsten film includes a mixture of alpha and beta phase tungsten, the silicon-doped tungsten film containing about 10-60% beta phase tungsten by atomic weight,

a majority of the tungsten fill material is alpha phase tungsten, and

a resistivity of the tungsten fill material is 2-4 Ω/sq for a recess of about 20 nm wide and between 50-100 nm in depth.

23. A method of forming a semiconductor device, comprising:

forming a seed layer comprising tungsten and silicon over a support surface of the semiconductor device; and

forming a tungsten structure over the doped tungsten-comprising seed layer, the tungsten structure forming a conductive line in which at least 50% of the tungsten is in alpha phase; and wherein at least 50% of the tungsten has a grain size with a maximum dimension of at least about 20 nm

24. The method of claim 23, wherein forming the seed layer comprises doping tungsten with silicon.

25. The method of claim 23, wherein forming the seed layer comprises depositing an alloy comprising tungsten and silicon.

26. The method of claim 25, wherein forming the seed layer comprises co-depositing silicon and tungsten by plasma vapor deposition.