

In the transmission and particularly the recording of a digital signal, it is known to mark the beginning of a data block with a synchronous signal. It is also often necessary to transmit an additional piece of information which does not belong to the actual data stream. A transmission system of this type is known from EP-A-0 146 636.

Fig. 1 shows an example of R-DAT (rotational digital audio tape) block format. Here the time of 8 data bits is reserved for the synchronous word. This is followed by twice 8 bits for the additional information and 8 bits of parity signal for recognition of errors in the additional information. The rest of the block is formed by the actual data stream of 32×8 bits. Transmission is effected with 8/10 modulation, i.e. a 10-bit word is formed from each 8-bit one. The transmission signal thereby becomes free from DC voltage and limited in its run length. The coding tables are drawn up so that the 10-bit synchronous pattern does not appear elsewhere in the bit stream.

This method of transmitting synchronous and additional information has the following disadvantages:

1. Reservation of an exclusive 10-bit pattern for the synchronous signal limits the choices available when drawing up the coding table.
2. The short synchronous pattern can easily be simulated when bit errors occur.
3. Before the additional information can be evaluated, block synchronisation has to be established by means of the synchronous word. Only then can the additional information be demodulated and checked by means of the parity word.

As a means of avoiding the disadvantages mentioned in points 1. and 2., the following method has already been proposed for signal recording in subdivided tracks:

a) The incoming signal at the beginning of the track contains a piece of information which enables block synchronisation to be established with a high degree of certainty, even during the incoming signal (DE-OS 35 33 962).

b) The synchronising words in the actual signal are selected so as to make the simulation of a synchronous word, which is shifted one or only a few bits, as improbable as possible (P 36 39 886).

Since synchronisation errors only occur as a result of bit slips, i.e. shifting of the counting phase for block synchronisation through one or only a few bits, when block synchronisation has been established by means of the incoming signal, it is sufficient to monitor the counting phase within a limited time window by means of the synchronous words transmitted. Hence it is also unnecessary to reserve certain bit patterns exclusively for synchronous words. The time window must be as large as possible, to enable extreme bit slips to be corrected. To make the simulation of a synchronous word which is shifted within that time window highly improbable, the synchronous word must be correspondingly long.

The problem underlying the invention is to make the possibility of evaluating the synchronous information and additional information as simple and certain as possible, with minimum expenditure on transmission capacity.

The problem is solved by the invention described in claim 1. Other advantageous embodiments of the invention are described in the sub-claims.

A modulation method is also known (US-A-4 389 636), wherein complementary bit pairs are provided, constituting either an O or an L (two demodulation).

The invention is based on the realisation that a relatively long synchronous word, and hence one where there is only a slight probability that it can be simulated, can transmit by double

modulation, a piece of additional information as well as the synchronous information.

In a matrix-type recording in blocks with tracks extending parallel with the edge of the tape in accordance with DE-OS 35 09 584, the additional information may e.g. comprise the number of a data block within a track and the track number within a track block.

The invention will now be explained with reference to Figs 2 and 3 of the accompanying drawings. In these:

Fig. 2 shows the bit pattern for the synchronous information and the additional information, and
Fig. 3 is a circuit diagram for the evaluation.

Fig. 2a shows simultaneous transmission of synchronous and additional information within a signal section S which is 40 bits long. The length of the signal section S corresponds to the example shown in Fig. 1. After 8/10 modulation the 4 x 8 bits of synchronous and additional information give 40 bits for transmission. The synchronous pattern S obtained by demodulation of the synchronous word is shown in Fig. 2b. This bit pattern is obtained by demodulation of the signal in Fig. 2a with a biphas mark demodulator. In the case of biphas each data bit is represented by two transmission bits. In the case of biphas mark the "1" is formed by two non-identical bits and the "0" by two identical bits. Fig. 2c shows the additional information obtained from the signal in Fig. 2a. The additional information A1, A2 is obtained by demodulation of the signal in Fig. 2a with a biphas level demodulator. In the case of biphas level the bit pairs always consist of non-identical bits. The information is contained in the "0" and "1" sequence within a bit pair.

The signal transmitted in the region S in Fig. 2a is free of DC, if the "0" always appears in pairs in the synchronous pattern S (Fig. 2b). The maximum run length is 3. The bit patterns for synchronous and additional information shown in Fig. 2a are

therefore appropriate for use within transmission codes which are free of DC voltage and which have a limited run length. They may also be used within bit streams which are not subject to these restrictions.

In the example shown in Fig. 2 each "1" in the synchronous pattern S (Fig. 2b) corresponds to an information bit of the additional signals (Fig. 2c). Two additional signals A1 and A2 are being transmitted here. The two signals are separated by 2 bit pairs which do not correspond to the biphase level signal. The non-identical word length for A1 and A2 makes it difficult to simulate a shifted synchronous pattern resulting from disturbed bits. The length of the synchronous pattern is desirably a whole-number multiple of the word length of the remaining signal.

Fig. 3 shows an example of an evaluating circuit for the synchronous signal in Fig. 2. A 40-bit long section of the signal in Fig. 2a is always available at the outputs of the shift register 1. These 40 bits are fed in pairs to the inputs of 20 EXOR gates 2. When the bit pattern S appears at the 20 outputs of the EXOR gates 2, the gate arrangement 3 generates a negative synchronous pulse at its output 8.

While the bit pattern S appears, the data words A1 and A2 of the additional information are applied to the outputs c of the shift register 1. A control circuit 7 decides whether these data words are transmitted to the counting circuits 5,6. The control has to be set up so as to ensure that operation is as trouble-free as possible. If satisfactory block synchronisation took place e.g. at the beginning of a track by means of the incoming signal, then resetting of the counters 4,5,6 during the track only takes place when a shifted synchronous signal is found within a time window in which the simulation of a synchronous signal is highly improbable. If block synchronisation could not take place by means of the incoming signal, the time window is switched off. As soon as the synchronous patterns are found to be appearing at the prescribed intervals, there is a high degree of certainty

that the correct operating state has been attained. The time window can be switched on again.

The signal in Fig. 2 may be used as synchronous and additional information for the said matrix-type recording in blocks. In the Fig. 3 circuit the counter 4 then counts the bits per data block. The counter 5 counts the data blocks per track, and the counter 6 counts the tracks or pairs of tracks per track block. The counters 4,5,6 must be set at the beginning of a playback section, a track block and a track respectively. The counter readings are corrected only if it is highly probable that the result of evaluating the synchronous and additional information is correct. The position of the said matrix-type recording in blocks within the recording pattern is determined, accurately to the exact bit, by the numerical values A0, A1 and A2.

The number of data blocks per track is restricted to 64 here by the number of bits in the data word A1. Given the relatively short tracks of the matrix-type recording, this is sufficient, particularly as with short data blocks the proportion of transmission capacity required for synchronous and additional information is correspondingly high. The data word A2 is sufficient to count 256 pairs of tracks or 512 tracks. Since adjacent tracks with opposing azimuth angles are recorded, the counting of pairs of tracks leads to clear track marking.

The synchronous signal in Fig. 2, containing the additional information, enables the additional information A1, A2 to be made available simultaneously with the recognition of the synchronous pattern S. Provided that the synchronous pattern is recognised, it is highly probable that the additional information will be free of errors.

CLAIMS

1. A method of transmitting a digital signal containing a synchronisation with a synchronous word and a piece of additional information, particularly for a recording, characterised in that the synchronous word also contains the additional information, parts of the signal, in each case with at least two successive binary signal states, representing both one bit (00,LL/L0,01) of the synchronous word corresponding to a first modulation and one bit (0L,L0) of the additional information corresponding to a second modulation, that the synchronous pattern (S) can be recognised only after demodulation of the synchronous word, and that a second demodulation of the synchronous word provides the additional information, the place value of the bits obtained by the second demodulation being determined by a clock signal (L) obtained from the synchronous information.

2. A method according to claim 1, characterised in that the synchronous pattern (S) is obtained through demodulation of the synchronous word by means of a biphase mark or biphase space demodulator, and the additional information is obtained by means of a biphase level demodulator.