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ABSTRACT OF THE DISCLOSURE

INVERSE TRANSPORT PROCESSOR WITH MEMORY ADDRESS CIRCUITRY

An inverse transport processor system for a TDM packet signal TV receiver includes apparatus for selectively extracting desired payloads of program component data and coupling this data to a common buffer memory data input port. A microprocessor (19) associated with the system also couples data to the common buffer memory (18) data input port. The respective component payloads and data generated by the microprocessor are stored in respective blocks of the common buffer memory in response to associated memory address which are applied to a memory address input port by an address multiplexer (17). A decryption device (16) is included to decrypt payload data according to packet specific decryption keys. In addition a detector (15) is included to detect payloads including entitlement data. Payloads containing entitlement data are directed via the common buffer memory to a smart card which generates the packet specific decryption keys. A memory data output port is coupled to a bus interconnected with the respective program component processors (21-24). Responsive to data requests from the respective program component processors, and data write requests from the component payload source, memory access for read and write functions is arbitrated (17) so that no incoming program data is lost, and all component processors are serviced.

Fig 3

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