WHAT IS CLAIMED IS:

1. An electronic device including a semiconductor memory, the semiconductor memory comprising:

a first memory cell having a first current path coupled to a first contact plug, the first current path having a first resistance; and

a second memory cell having a second current path coupled to a second contact plug, the second current path having a second resistance, the second resistance being higher than the first resistance,

wherein a resistance of the first contact plug is higher than a resistance of the second contact plug to compensate for a difference between the first and second resistances.

2. The electronic device of claim 1, further comprising:

a plurality of conductive lines including row lines and column lines;

a plurality of contact plugs including row contact plugs and column contact plugs, the row contact plugs respectively coupled to the row lines, the column contact plugs respectively coupled to the column lines; and

a plurality of memory cells provided in a cell region and including the first and second memory cells, each memory cell having a current path coupled to a row contact plug and a column contact plug, the current path including a portion of a column line coupled between a corresponding memory cell and the column contact plug and a portion of a row line coupled between the corresponding memory cell and the row contact plug.

3. The electronic device of claim 2, further comprising:

third and fourth contact plugs disposed in a periphery of the cell region,

wherein the first current path includes a portion of a first conductive line coupled between the first memory cell and the third contact plug,

wherein the second current path includes a portion of a second conductive line coupled between the second memory cell and the fourth contact plug, and

wherein the portion of the first conductive line is shorter than and has a lower resistance than the portion of the second conductive line.

4. The electronic device of claim 3, wherein the cell region comprises a first area adjacent to the first and second contact plugs and a second area adjacent to the first area,

wherein the first conductive line is disposed in the first area and not disposed in the second area, and

wherein the second conductive line is disposed in the second area.

5. The electronic device of claim 3,

wherein the cell region comprises:

a first area adjacent to a first side of the cell region, the first side being adjacent to the first and second contact plugs, and

a second area adjacent to a second side of the cell region, the second side being opposite the first side;

wherein the first conductive line is disposed in the first area and not disposed in the second area, and

wherein the second conductive line is disposed in the second area.

6. The electronic device of claim 1, wherein the first contact plug includes a region having an oxygen concentration higher than that of a corresponding region of the second contact plug to increase the resistance of the first contact plug.

7. The electronic device of claim 1, wherein the first contact plug includes an oxide pattern disposed on a surface of the first contact plug to increase the resistance of the first contact plug.

8. The electronic device of claim 7, wherein the first contact plug includes a first conductive portion and a second conductive portion disposed over the first conductive portion, and the oxide pattern is disposed over a surface of the first conductive portion.

9. The electronic device of claim 1, further comprising:

a plurality of conductive lines including row lines and column lines;

a plurality of contact plugs including row contact plugs and column contact plugs, the row contact plugs respectively coupled to the row lines, the column contact plugs respectively coupled to the column lines; and

a plurality of memory cells provided in a cell region and including the first and second memory cells, each memory cell having a current path coupled to a row contact plug and a column contact plug, the current

path including a portion of a column line coupled between a corresponding memory cell and the column contact plug and a portion of a row line coupled between the corresponding memory cell and the row contact plug,

wherein the first contact plug and the second contact plug are each disposed along a first side of the semiconductor memory,

wherein at least one contact plug is disposed along a second side of the semiconductor memory, the second side being orthogonal to the first side,

wherein the first contact plug is closer to the second side than the second contact plug,

wherein contact plugs disposed along the first side are grouped into a plurality of groups of contact plugs according to respective distances between the contact plugs and the second side,

wherein a first group of the plurality of groups includes contact plugs having a distance to the second side that is less than a first predetermined value,

wherein a second group of the plurality of groups includes contact plugs having a distance to the second side that is greater than a second predetermined value, the second predetermined value being greater than or equal to the first predetermined value,

wherein the first contact plug is in the first group,

wherein the second contact plug is in the second group, and

wherein each contact plug in the first group has the same resistance as that of the first contact plug.

10. The electronic device of claim 9, wherein a third group of the plurality of groups includes contact plugs having a distance to the second side that is greater than the first predetermined value and less than the second predetermined value, and

wherein each contact plug in the third group has a respective resistance that is less than the resistance of the first contact plug and greater than the resistance of the second contact plug.

11. An electronic device including a semiconductor memory, the semiconductor memory comprising:

a plurality of conductive lines including word lines and bit lines;

a plurality of contact plugs including word line contact plugs and bit line contact plugs, the word line contact plugs respectively coupled to the word lines, the bit line contact plugs respectively coupled to the bit lines; and

a plurality of memory cells provided in a cell region, each memory cell having a current path coupled to a word line contact plug and a bit line contact plug, the current path including a portion of a bit line coupled between a corresponding memory cell and the bit line contact plug and a portion of a word line coupled between the corresponding memory cell and the word line contact plug,

wherein a first memory cell has a first current path coupled to a first contact plug, the first current path having a first resistance,

wherein a second memory cell has a second current path coupled to a second contact plug, the second current path having a second

resistance, the second resistance being higher than the first resistance, and

wherein the first contact plug is configured to have a higher resistance than that of the second contact plug to compensate for a difference between the first and second resistances.

12. The electronic device of claim 11,

wherein the plurality of contact plugs is disposed in a periphery of the cell region and include a third contact plug and a fourth contact plug,

wherein the first current path including a portion of a first conductive line coupled between the first memory cell and the third contact plug,

wherein the second current path including a portion of a second conductive line coupled between the second memory cell and the fourth contact plug, and

wherein the portion of the first conductive line is shorter than and has a lower resistance than the portion of the second conductive line.

13. The electronic device of claim 12, wherein the cell region comprises a first area adjacent to the first and second contact plugs and a second area adjacent to the first area,

wherein the first conductive line is disposed in the first area and not disposed in the second area, and

wherein the second conductive line is disposed in the second area.

14. The electronic device of claim 12,

wherein the cell region comprises:

a first area adjacent to a first side of the cell region, the first side being adjacent to the first and second contact plugs, and

a second area adjacent to a second side of the cell region, the second side being opposite the first side;

wherein the first conductive line is disposed in the first area and not disposed in the second area, and

wherein the second conductive line is disposed in the second area.

15. The electronic device of claim 11, wherein the first contact plug includes a region having an oxygen concentration higher than oxygen concentration of a corresponding region of the second contact plug to increase the resistance of the first contact plug.

16. The electronic device of claim 11, wherein the first contact plug includes an oxide pattern disposed on a surface of the first contact plug to increase the resistance of the first contact plug.

17. The electronic device of claim 16, wherein the first contact plug includes a first conductive portion and a second conductive portion disposed on top of the first conductive portion, and the oxide pattern is disposed on a top surface of the first conductive portion.

18. The electronic device of claim 11, wherein the first contact plug and the second contact plug are each disposed along a first side of the semiconductor memory.

19. The electronic device of claim 18, wherein at least one contact plug is disposed along a second side of the semiconductor memory, the second side being orthogonal to the first side,

wherein the first contact plug is closer to the second side than the second contact plug,

wherein contact plugs disposed along the first side are grouped into a plurality of groups of contact plugs according to respective distances between the contact plugs and the second side,

wherein a first group of the plurality of groups includes contact plugs having a distance to the second side that is less than a first predetermined value,

wherein a second group of the plurality of groups includes contact plugs having a distance to the second side that is greater than a second predetermined value, the second predetermined value being greater than or equal to the first predetermined value,

wherein the first contact plug is in the first group,

wherein the second contact plug is in the second group, and

wherein each contact plug in the first group has the same resistance as that of the first contact plug.

20. The electronic device of claim 19,

wherein a third group of the plurality of groups includes contact plugs having a distance to the second side that is greater than the first predetermined value and less than the second predetermined value, and

wherein each contact plug in the third group has a respective resistance that is less than the resistance of the first contact plug and greater than the resistance of the second contact plug.