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(54) IMPROVEMENTS IN OR RELATING TO SEMICONDUCTOR DEVICES

(71) We, HITACHI LIMITED, a body corporate organised according to the laws of Japan, of 1-5-1 Marunouchi, Chiyoda-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed, to be particularly described in and by the following statement:

This invention relates to semiconductor devices, more particularly but not necessarily exclusively large scale integrated circuits (LSI), which employ insulated gate field-effect transistors (MIS FET's).

Semiconductor devices in the field of information processing require a high density of integration for such reasons as the reliability and reduction of costs. As an effective expedient to satisfy this requirement, there is the LSI which is constructed using the MIS FET as the fundamental element and in which the respective elements are integrated on a single semiconductor substrate.

The MIS LSI constructed with the MIS FET as the fundamental element has a structure in which isolation of the elements is unnecessary and the density of integration becomes higher to that extent. Moreover, when the elements are the MIS FET's of the enhancement type, there are the merits that the manufacturing techniques are relatively easy and the production yield is high.

However, in the multilayer wiring technique indispensable to conventional MIS LSI's, aluminium wiring is used for the electrical interconnection among the electrodes of the respective elements of the MIS LSI. In connecting the aluminium conductors and the electrodes of the respective elements, the area occupied by the contact holes is large due to the difficulty of the dimensional precision of a mask even when the contact holes are formed by an accurate mask registration and an elaborate photo resist technique. In consequence, the density of integration of the MIS LSI is reduced.

For example, an insulated gate type read only memory (MIS ROM) used as one of the constituent blocks of an MIS LSI has been constructed in an array as schematically shown in Figure 1 of the accompanying drawings. Figures 2 and 3 illustrate the pattern of the MIS ROM which is formed on a single semiconductor substrate. In Figure 1, $Q_1 - Q_5$ denote MIS FETs of the enhancement type, $A_1 - A_3$ address connections, and $B_1 - B_3$ connections for output signals. Figure 3 is a sectional view on the line III–III of Figure 2. In Figures 2 and 3, numeral 1 designates an N-type silicon substrate, 2 and 3 P^+-type regions which are source or drain regions, 4 an insulating film, 5 polycrystal silicon layers for silicon gates, 6 aluminium conductors, and 7 contact holes which electrically connect the aluminium conductors to their associated P^+-type regions for the drains, wherein only the insulating films under gate electrodes of enhancement mode transistors are made thin so as to form these transistors as actual elements and the other insulating films under address input connections crossing with output connections are made thick so as not to form the positions as actual elements.

As is apparent from Figures 1 to 3, the MIS ROM which is constructed using the plurality of MIS FET's of the enhancement type needs to employ the aluminium conductors as a multilayer arrangement in order to connect the drain P^+-type regions of the respective MIS FET's to the output lines, and also need to be formed with the contact holes on the drain P^+-type regions of the respective MIS FET's in order to establish electrical connection between the aluminium conductors and the drain P^+-type regions. Moreover, the MIS ROM which is constructed from the memory array body as shown in Figure 3 includes huge numbers of MIS FET's and interconnections. Besides,

when the peripheral circuits of the MIS ROM are added, the numbers of the elements and interconnections increase more. An extremely large number of contact holes are accordingly required for connecting the multilayer arrangement of aluminium conductors and the drain P^+–type regions. For this reason, the density of integration of the prior-art MIS LSI including the MIS ROM has to be reduced.

According to one aspect of the present invention there is provided a semiconductor integrated circuit device including: a plurality of enhancement and depletion type field-effect transistors each having source and drain regions of a first conductivity type located in a substrate of a second conductivity type, opposite to said first conductivity type, and a gate electrode overlying a region between the source and drain regions, said plurality of transistors being arranged in the form of a matrix of rows and columns of transistors, the transistors of each row being connected in series through their source and drain paths; and a plurality of electrical connections corresponding to said columns of transistors, the gate electrodes of the transistors of each column being connected to the corresponding electrical connections in common.

According to another aspect of the present invention there is provided a semiconductor integrated circuit device including: a plurality of conductive layers electrically separated from each other and being substantially arranged in parallel with each other on an insulating layer lying on a semiconductor substrate of a first conductivity type; and a plurality of diffused regions of a second conductivity type opposite to said first conductivity type being arranged in parallel with each other in said semiconductor substrate and extending so that each of the conductive layers cross respective said diffused regions; each of the crossed portions of the conductive layers and the diffused regions act as field effect transistors, some of said transistors being of the depletion type whilst others are of the enhancement type.

The present invention will be described in greater detail with reference to Figures 4, 5 and 6*a* and 6*b* of the remaining figures of the accompanying drawings, wherein:

Figure 4 is a schematic diagram showing a part of a complex electric circuit in which a MIS ROM is assembled into a MIS LSI being a semiconductor device in accordance with the invention,

Figure 5 is a plan view in the case where the electric circuit is formed on a single silicon substrate, and

Figures 6*a* and *b* are schematic sectional views on the line VI–VI in Figure 5, Figure 6*b* illustrating a possible modification of the structure in Figure 6*a*.

In Figures 4 A_1 – A_3 denote address connections, B_1 – B_3 connections for output signals, Q_{E1} – Q_{E5} MIS FETs of the enhancement type, and Q_{D1} – Q_{D4} MIS FETs of the depletion type. The numeral 1 (Figures 6*a* and *b*) designates an N-type silicon substrate, 2 a P^+–type region for a source or drain, 3 or 3′ a P–type region for a channel in a MIS FET of the depletion type, 4 an insulating film, and 5 polycrystal silicon layers for silicon gates.

A MIS ROM at a very high density of integration can be constructed on a single semiconductor substrate in such way that the plurality of actual MIS FET's are arrayed in the shape of a matrix as illustrated in Figure 4 and that Q_{E1} – Q_{E5} are made MIS FETs of the enhancement type, while Q_{D1} – Q_{D4} are made the MIS FETs of the depletion type.

More specifically, the MIS ROM in this embodiment is composed of MIS FETs of the enhancement type which operate the bits of the MIS ROM (elements of the so-called normally off type in which, at a zero gate voltage the connection between the source and drain is cut off and when a certain threshold voltage is applied to the gate electrode, the channel is formed for the first time and the connection between the source and drain falls into the conductive state), and MIS FETs of the depletion type in which the surface of the N–type silicon substrate as underlies the gate electrode becomes a P^+–type region by thermal diffusion or ion implantation (elements of the so-called on type in which, even at zero gate voltage the channel is formed and the connection between the source and the drain is in the conductive state). The MIS FETs of the depletion type are always in the "on" state, while the MIS FETs of the enhancement type can detect two levels of the "on" state and the "off" state. Accordingly, "1" and "0" are distinguishable, and the operation of the MIS ROM is possible in such manner that an output signal current is produced at a point where a MIS FET of the enhancement type is connected, when that point is addressed.

Where polycrystalline layers are to be used as the gate electrodes and interconnection layers, it is much more preferable to provide the thin or shallow channel layers 3′ of the depletion type MOS FETs as shown in Figure 6*b* by ion-implantation of an impurity such as boron rather than to provide the thick or deep channel layers 3 shown in Figure 6*a* by thermal diffusion of boron. Such a MOS FET matrix is fabricated by forming a thin SiO_2 film of 500 to 1500 angstroms on the N–type silicon substrate surface position where the MOS FETs are required, introducing boron ions partially through the

thin SiOz film into the substrate so as to form P type channel regions for depletion type transistors, forming polycrystalline silicone bands on the thin SiOz film by depositing silicon material, selectively removing the thin SiOz film to form openings for source and drain regions of the MOS FETs, and then diffusing or introducing a P type impurity such as boron into the substrate surface through the openings using the silicon bands as the diffusion mask thereof. Thus, at each crossing portion between the polycrystalline silicon input bands 5 and the outputs 2 of P^+-type semiconductor regions an actual MOS FET of enhancement or depletion mode can be provided, wherein all of the MOS FETs have thin gate insulating films of substantially the same thickness of 500 to 1500 angstroms as shown in Figures 4, 5 and 6*b*.

Furthermore, since the MIS ROM described has the MIS FETs of the depletion type and of the enhancement type arranged in the shape of the matrix, it is unnecessary to employ the aluminium conductors as a multilayer arrangement and it is unnecessary to provide a multilayer wiring even in places where the P^+-type regions 2 of the source or drain regions and the polycrystal silicon 5 forming the silicon gate electrodes intersect. Furthermore, since the MIS ROM of this embodiment has the drain P^+-type region of each depletion MIS FET connected with the adjacent source P^+-type region by a P^+-type regions, it is not necessary to provide the prior arrangement in which the drain is connected to the earth line or to the aluminium conductor forming part of a multilayer arrangement by providing the contact hole and the total number of contact holes is considerably reduced.

The MIS ROM described with reference to Figures 4 to 6 can give a MIS LSI with an extraordinarily high density of integration. Moreover, it is possible to obtain a high production yield and high reliability because the manufacturing method is relatively simple and easy.

As will be apparent from the foregoing embodiment, the invention can readily be embodied without employing any multilayer wiring in an MIS LSI having a circuit arrangement in which the polycrystal silicon layer for the silicon gates and the P^+-type regions for the sources or drains intersect. It is therefore possible to obtain the MIS LSI at a very high density of integration.

This invention is not restricted to the embodiment described above, but it is applicable to semiconductor devices of various forms where, by use of the invention, combining MIS FETs of the enhancement type and those of the depletion type in the shape of the matrix on the single semiconductor substrate, such semiconductor devices can be produced with a very high density of integration and by a relatively simple and easy manufacturing technique.

WHAT WE CLAIM IS:—

1. A semiconductor integrated circuit device including: a plurality of enhancement and depletion type field-effect transistors each having source and drain regions of a first conductivity type located in a substrate of a second conductivity type, opposite to said first conductivity type, and a gate electrode overlying a region between the source and drain regions, said plurality of transistors being arranged in the form of a matrix of rows and columns of transistors, the transistors of each row being connected in series through their source and drain paths; and a plurality of electrical connections corresponding to said columns of transistors, the gate electrodes of the transistors of each column being connected to the corresponding electrical connections in common.

2. A semiconductor integrated circuit device according to claim 1, wherein each of said gate electrodes is formed of polycrystalline silicon.

3. A semiconductor integrated circuit device according to claim 2, wherein the polycrystalline silicon gate electrodes of the transistors of each column are formed of the same continuous polycrystalline silicon electrode.

4. A semiconductor integrated circuit device according to any one of the preceding claims, wherein channel regions of the first conductivity type are formed at said regions between the source and drain regions of said depletion type transistors by ion implantation, so as to form conductive paths between said source and drain regions.

5. A semiconductor integrated circuit device according to claim 4, wherein each ion-implanted channel region extends from the surface of the substrate to a depth greater than that of the source and drain regions and overlaps the source and drain regions.

6. A semiconductor integrated circuit device according to claim 4, wherein each ion-planted channel region extends from the surface of the substrate to a depth less than that of the source and drain regions and overlaps the source and drain regions.

7. A semiconductor integrated circuit device including: a plurality of conductive layers electrically separated from each other and being substantially arranged in parallel with each other on an insulating layer lying on a semiconductor substrate of a first conductivity type; and a plurality of diffused regions of a second conductivity type opposite to said first conductivity type being arranged in parallel with each other in said semiconductor substrate and extending so

thin SiOz film into the substrate so as to form P type channel regions for depletion type transistors, forming polycrystalline silicone bands on the thin SiOz film by depositing silicon material, selectively removing the thin SiOz film to form openings for source and drain regions of the MOS FETs, and then diffusing or introducing a P type impurity such as boron into the substrate surface through the openings using the silicon bands as the diffusion mask thereof. Thus, at each crossing portion between the polycrystalline silicon input bands 5 and the outputs 2 of P^+–type semiconductor regions an actual MOS FET of enhancement or depletion mode can be provided, wherein all of the MOS FETs have thin gate insulating films of substantially the same thickness of 500 to 1500 angstroms as shown in Figures 4, 5 and 6*b*.

Furthermore, since the MIS ROM described has the MIS FETs of the depletion type and of the enhancement type arranged in the shape of the matrix, it is unnecessary to employ the aluminium conductors as a multilayer arrangement and it is unnecessary to provide a multilayer wiring even in places where the P^+–type regions 2 of the source or drain regions and the polycrystal silicon 5 forming the silicon gate electrodes intersect. Furthermore, since the MIS ROM of this embodiment has the drain P^+–type region of each depletion MIS FET connected with the adjacent source P^+–type region by a P^+–type regions, it is not necessary to provide the prior arrangement in which the drain is connected to the earth line or to the aluminium conductor forming part of a multilayer arrangement by providing the contact hole and the total number of contact holes is considerably reduced.

The MIS ROM described with reference to Figures 4 to 6 can give a MIS LSI with an extraordinarily high density of integration. Moreover, it is possible to obtain a high production yield and high reliability because the manufacturing method is relatively simple and easy.

As will be apparent from the foregoing embodiment, the invention can readily be embodied without employing any multilayer wiring in an MIS LSI having a circuit arrangement in which the polycrystal silicon layer for the silicon gates and the P^+–type regions for the sources or drains intersect. It is therefore possible to obtain the MIS LSI at a very high density of integration.

This invention is not restricted to the embodiment described above, but it is applicable to semiconductor devices of various forms where, by use of the invention, combining MIS FETs of the enhancement type and those of the depletion type in the shape of the matrix on the single semiconductor substrate, such semiconductor devices can be produced with a very high density of integration and by a relatively simple and easy manufacturing technique.

WHAT WE CLAIM IS:—

1. A semiconductor integrated circuit device including: a plurality of enhancement and depletion type field-effect transistors each having source and drain regions of a first conductivity type located in a substrate of a second conductivity type, opposite to said first conductivity type, and a gate electrode overlying a region between the source and drain regions, said plurality of transistors being arranged in the form of a matrix of rows and columns of transistors, the transistors of each row being connected in series through their source and drain paths; and a plurality of electrical connections corresponding to said columns of transistors, the gate electrodes of the transistors of each column being connected to the corresponding electrical connections in common.

2. A semiconductor integrated circuit device according to claim 1, wherein each of said gate electrodes is formed of polycrystalline silicon.

3. A semiconductor integrated circuit device according to claim 2, wherein the polycrystalline silicon gate electrodes of the transistors of each column are formed of the same continuous polycrystalline silicon electrode.

4. A semiconductor integrated circuit device according to any one of the preceding claims, wherein channel regions of the first conductivity type are formed at said regions between the source and drain regions of said depletion type transistors by ion implantation, so as to form conductive paths between said source and drain regions.

5. A semiconductor integrated circuit device according to claim 4, wherein each ion-implanted channel region extends from the surface of the substrate to a depth greater than that of the source and drain regions and overlaps the source and drain regions.

6. A semiconductor integrated circuit device according to claim 4, wherein each ion-planted channel region extends from the surface of the substrate to a depth less than that of the source and drain regions and overlaps the source and drain regions.

7. A semiconductor integrated circuit device including: a plurality of conductive layers electrically separated from each other and being substantially arranged in parallel with each other on an insulating layer lying on a semiconductor substrate of a first conductivity type; and a plurality of diffused regions of a second conductivity type opposite to said first conductivity type being arranged in parallel with each other in said semiconductor substrate and extending so

that each of the conductive layers cross respective said diffused regions; each of the crossed portions of the conductive layers and the diffused regions act as field effect transistors, some of said transistors being of the depletion type whilst others are of the enhancement type.

8. A semiconductor integrated circuit device according to any one of the preceding claims, wherein said transistors are MIS FETs.

9. A semiconductor device constructed and arranged substantially as described herein with reference to Figures 4 and 5 together with Figure 6*a* or Figure 6*b* of the accompanying drawings.

10. A method of producing a semiconductor device substantially as described herein with reference to Figures 4 and 5 together with Figure 6*a* or Figure 6*b* of the accompanying drawings.

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