

CONTROL OF MULTIPLE EQUIVALENT FUNCTIONAL UNITS FOR POWER REDUCTION

Abstract

A processor (10) with multiple equivalent functional units for power reduction, which includes a mechanism (18) for controlling the selection of functional units. Specifically, the processor (10) comprises a first circuit performing a predetermined function at a first speed, a second circuit for performing the same predetermined function at a second speed, and a control system for selecting either the first or second circuit to perform the function. The control system further includes a mechanism for controlling the rate of execution of the processor instructions in the pipeline (12) in order to compensate for the speed at which the first or second circuit was performing the predetermined function.

Fig 1